Si-Based Interband Tunneling Devices For High-Speed Logic and Low Power Memory Applications

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Tunnel diode/transistor logic (TDTL), realized to date in III-V material systems only, enhances any transistor technology [1]. Memory circuits incorporating low current density double barrier resonant tunneling diodes (DBRTDs) [2] and resonant interband tunneling diodes (RITDs) [3] have been demonstrated with fewer transistors and lower power dissipation than conventional CMOS SRAM or DRAM circuitry. High current density DBRTDs, in contrast, have been shown to successfully improve the speed and power of logic circuitry such as multiplexers [4] and analog-to-digital converters [5]. However, such technology will never reach mainstream CMOS or SiGe HBT technology unless a suitable Si-based negative differential resistance (NDR) device can be developed.

This study extends the preliminary work of the authors [6], presenting improved epitaxially grown $Si/Si_{0.5}Ge_{0.5}/Si$ resonant interband tunnel diodes (RITDs) with current densities which exceed any previously reported [7] for a Si-based NDR device. For the first time, the needs of Si-based TDTL circuits are beginning to be addressed. Two new classes of Si-based NDR devices are also reported here: *Si-only* RITDs and $Si/Si_{0.5}Ge_{0.5}$ heterojunction Esaki tunnel diodes with a digitally graded superlattice (DG-SL). The key to achieving room temperature NDR is developing tight control of dopant profiles during epitaxial growth. The structures presented here make use of δ-doping planes of B and Sb to reduce the doping requirements of the bulk regions and also to define the tunnel barrier. The use of a low substrate temperature (370°C) during molecular beam epitaxial (MBE) growth leads to higher dopant incorporation and minimizes the segregation of dopants, such as Sb, during growth [8]. Post growth rapid thermal anneals (RTA) were employed to activate dopants and reduce point defect density. An intrinsic tunnel barrier was incorporated in all designs to reduce gap states and band tails in order to reduce the excess valley current. As will be shown in this study, precise control of the dopant profile, the material content of the tunnel barrier, and the device geometry are all critical to engineering the desired current density.

Fig. 1 presents a schematic diagram of a design for a high current density RITD. The intrinsic tunnel region consists of a 2 nm layer of strained, pseudomorphic $Si_{0.5}Ge_{0.5}$ cladded on either side with 1 nm of Si to separate the δ-doped layers from the heterointerface. The narrow bandgap $Si_{0.5}Ge_{0.5}$ is used to enhance the current density. The depletion region and tunnel barrier are confined between the two δ-doped planes. Fig. 2 shows the calculated band diagram and resonant states of the device assuming 1 nm diffusive broadening of the δ-doped regions. The quantum charge was calculated for each band from the effective mass Schrödinger equation and iterated to convergence with Poisson's equation. Secondary ion mass spectrometry (SIMS) depth profiling was performed on this structure after a 700°C 1 minute RTA which indicated significant segregation of the Sb during growth. A second band diagram of this structure was generated using the SIMS data, and is shown in Fig. 3. The later band diagram suggests that the quantum confinement of the Sb δ-doping spike is lost due to dopant segregation during growth. As SIMS depth resolution is known to suffer from knock-on effects, possibly exaggerating the degree of dopant segregation, an interpolation between the two band diagrams of Figs. 2 and 3 would be reasonable. If in fact there is quantum confinement due to the Sb δ-doping, the well is certainly more shallow than indicated by the ideal band diagram of Fig. 2. Fig. 4 shows a curve tracer plot of the I-V characteristics from a representative $Si/Si_{0.5}Ge_{0.5}/Si$ RITD which exhibited a peak-to-valley current ratio (PVCR) up to 2.05 with a peak current density of 22 kA/cm^2. To the knowledge of the authors, this current density exceeds any previously reported for a Si-based NDR structure.

A *Si-only* version of the above device resulted in an order of magnitude decrease in the current density which is still large for a *Si-only* tunnel diode. A schematic of the *Si-only* device is shown in Fig. 5 and a calculated band diagram using the expected dopant profile is shown in Fig. 6. Optimal device performance was found to occur for a 625°C 1 minute RTA for the *Si-only* RITDs. Fig. 7 shows representative I-V characteristics of these RITDs captured by a Hewlett-Packard 4142 Semiconductor Parameter Analyzer. A PVCR up to 1.39 with a current density of 3.1 kA/cm^2 was observed.

Due to the Sb segregation, the depletion region and tunnel barrier of both the $Si/Si_{0.5}Ge_{0.5}/Si$ and the *Si-only* RITD widen several nm beyond that of the design. The authors have reason to believe that greater control over the Sb segregation can be obtained by a lower growth temperature. Furthermore, simulations show that the δ-doped planes can be placed closer and still maintain the built in voltage between them. Since tunnel current depends exponentially on barrier width, there is room for one to two orders of magnitude increase in the current density for both the $Si/Si_{0.5}Ge_{0.5}/Si$ and the *Si-only* RITD.

A final structure, a $Si/Si_{0.5}Ge_{0.5}$ heterojunction Esaki diode with a DG-SL, is shown in Fig. 8. The structure was designed to take advantage of the natural band offsets between Si and $Si_{0.5}Ge_{0.5}$, which lowers the doping requirements on the P^+ side of the junction. A 10 nm DG-SL was incorporated on the P^+ side of the junction to reduce the barrier for holes to populate the valence band well. In order to *lower* the current density, a 4 nm intrinsic Si spacer was placed between the P^{++} and N^{++} layers. The band diagram of this structure is shown in Fig. 9. Fig. 10 shows the I-V characteristics of representative tunnel diodes which had a PVCR up to 1.2 with a peak current density of 7.5 A/cm^2, almost 4 orders of magnitude smaller than the $Si/Si_{0.5}Ge_{0.5}/Si$ RITDs. The low current density of this structure makes it a potential design to optimize for memory applications.

In conclusion, the authors have demonstrated a family of epitaxially fabricated Si-based NDR devices operating at room temperature. The precise control of dopant profiles as a result of the low temperature growth and post growth heat treatments enables the engineering of current densities, something previously unattainable for Si-based NDR structures. The authors have further demonstrated devices which have current densities exceeding any previously reported in Si-based NDR structures. With further adjustments to the growth conditions and device geometries, this value is expected to exceed 10^5 A/cm^2. Low current density devices suitable for memory applications have also been demonstrated. With this new fabrication technology, Si-based TDTL circuitry may become a reality.

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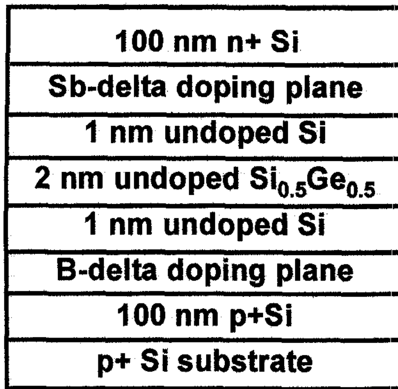

Fig. 1. Schematic diagram of the $Si/Si_{0.5}Ge_{0.5}/Si$ RITD structure.

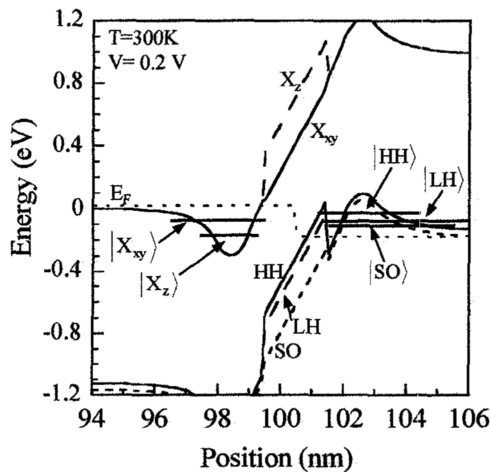

Fig. 2. Calculated band diagram and resonant states of the high current density $Si/Si_{0.5}Ge_{0.5}/Si$ RITD. 1 nm diffusive broadening of the δ-doped profiles were assumed for this calculation.

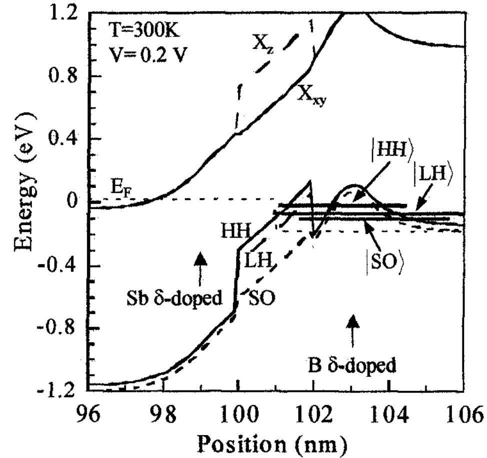

Fig. 3. Calculated band diagram of the high current density $Si/Si_{0.5}Ge_{0.5}/Si$ RITD using the SIMS Sb profile. Note that confinement on the Sb side of the junction has lost confinement because of segregation during growth.

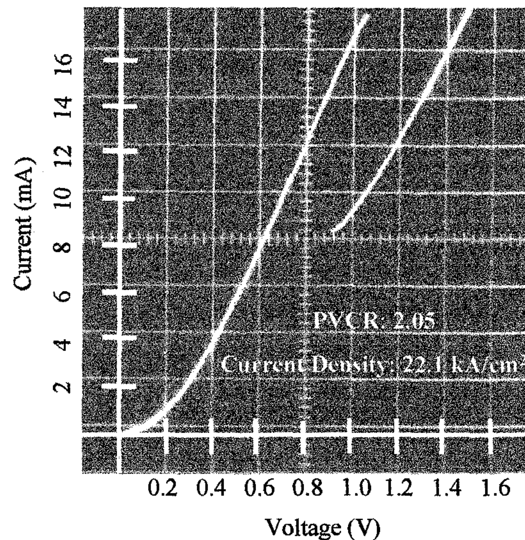

Fig. 4. I-V characteristics of the high current density $Si/Si_{0.5}Ge_{0.5}/Si$ RITD structure annealed at 700°C having an 18 μm diameter which exhibits room temperature NDR (PVCR $\sim$ 2.05 at a peak current density of 22 kA/cm^2).

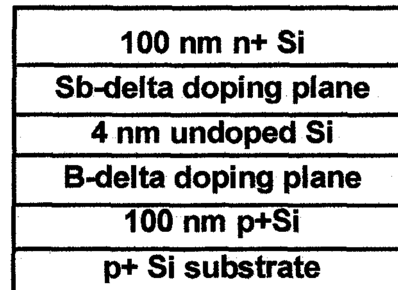

Fig. 5. Schematic diagram of the *Si-only* RITD structure.

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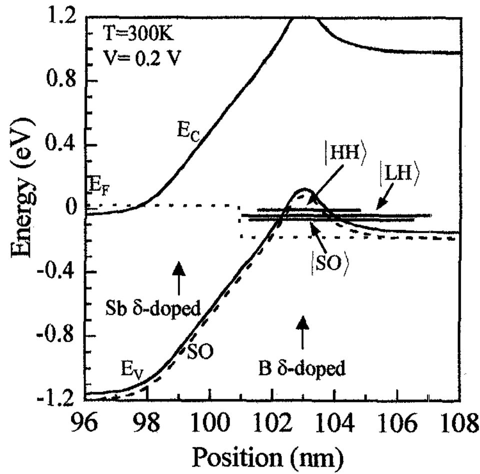

Fig. 6. Calculated band diagram and resonant states of the *Si-only* RITD of Fig. 5 using the expected Sb doping profile.

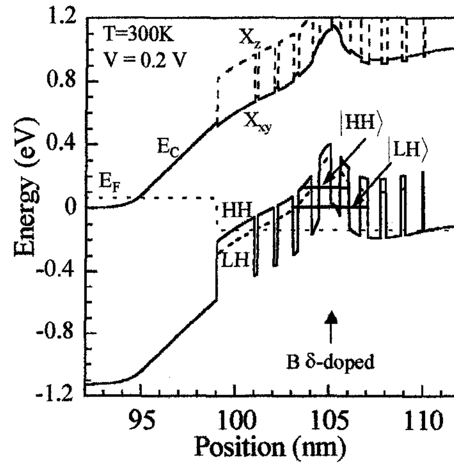

Fig. 9. Calculated band diagram and resonant states of the low current density DG-SL heterojunction Esaki diode.

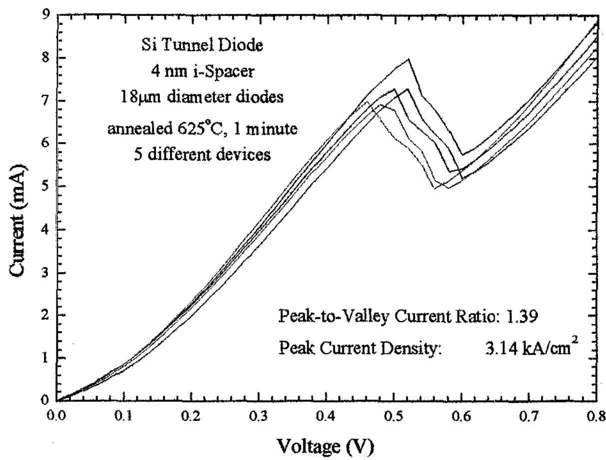

Fig. 7. I-V characteristics of six representative *Si-only* RITDs annealed at 625°C having 18 μm diameters which exhibit room temperature NDR (PVCR ~ 1.4 at a peak current density of 3.14 kA/cm^2).

~50 nm n+ Si
20 nm n++ Si
4 nm undoped Si
5 nm $p^+Si/Si_{0.5}Ge_{0.5}$ DG-SL 5 periods
B-delta doping plane
5 nm $p^+Si/Si_{0.5}Ge_{0.5}$ DG-SL 5 periods
100 nm p+Si
p+ Si substrate

Fig. 8. Schematic diagram of the $Si/Si_{0.5}Ge_{0.5}$ heterojunction Esaki diode with a DG-SL structure.

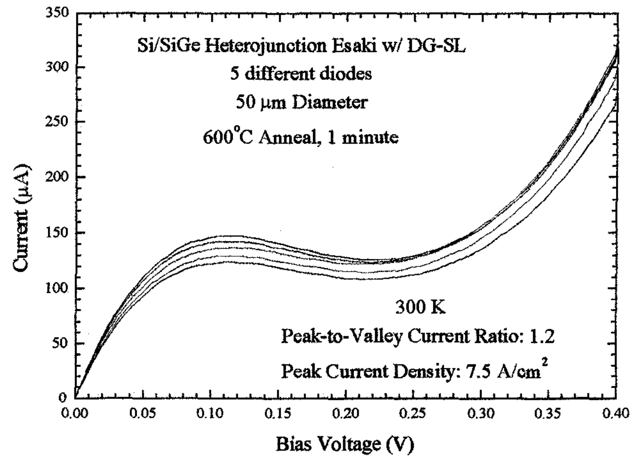

Fig. 10. I-V characteristics of five representative DG-SL heterojunction Esaki diodes annealed at 600°C having 50 μm diameters which exhibit room temperature NDR (PVCR ~ 1.2 at a peak current density of 7.5 A/cm^2).

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