Epitaxially Grown Si Resonant Interband Tunnel Diodes Exhibiting High Current Densities

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***Abstract*— This study presents the room-temperature operation of δ-doped Si resonant interband tunneling diodes which were fabricated by low-temperature molecular beam epitaxy. Post growth rapid thermal annealing of the samples was found to improve the current–voltage (I–V) characteristics. Optimal performance was observed for a 600 °C 1 min anneal, yielding a peak-to-valley current ratio (PVCR) as high as 1.38 with a peak current density (J_p) as high as 1.42 kA/cm^2 for a device with a 4-nm intrinsic Si tunnel barrier. When the tunnel barrier was reduced to 2 nm, a PVCR of 1.41 with a J_p as high as 10.8 kA/cm^2 was observed. The devices withstood a series of burn-in measurements without noticeable degradation in either the J_p or PVCR. The structures presented are strain-free, and are compatible with a standard CMOS or HBT process.**

***Index Terms*—CMOS compatability, molecular beam epitaxy, negative differential resistance, rapid thermal annealing, resonant interband tunneling diodes, silicon.**

I. Introduction

TUNNEL diodes are undergoing a rebirth particularly in the III–V material systems where integrated tunnel diode/transistor circuits are showing promise for mixed signal [1], [2] and memory [3], [4] applications. However, the lack of a Si-based process compatible with CMOS or SiGe heterojunction bipolar transistor (HBT) technology has impeded similar efforts in Si. Many of the earliest Si-based tunnel diodes, including the Si Esaki diode with the highest reported peak-to-valley current ratio (PVCR) of 4.0 [5], were fabricated via an alloying process. While this technique was adept at fabricating discrete devices, it was not suited for integrated circuit processing [6]. Valient attempts were made in the early 1990's to fabricate Si/SiGe resonant tunneling diodes (RTD's), but the lack of a material capable of achieving a conduction band offset prevented the realization of RTD's with PVCR's much greater than 1.2 [7]. A recent letter by the authors presented the room-temperature operation of δ-doped Si/$Si_{0.5}Ge_{0.5}$/Si resonant interband tunneling diodes (RITD's) which were fabricated epitaxially by low-temperature molecular beam epitaxy (LT-MBE) [8]. As-grown samples showed no evidence of negative differential resistance (NDR). However, heat treatments in a rapid thermal annealing (RTA) furnace used for dopant activation and point defect reduction resulted in NDR behavior. PVCR's as high as 1.5 at a peak current density of 3.2 kA/cm^2 were reported for a 1-min anneal at 700 °C. Beyond this temperature, the current density was found to abruptly decrease by an order of magnitude. This letter builds upon the previous study, presenting epitaxially fabricated δ-doped RITD structures consisting purely of Si which exhibit NDR at room temperature.

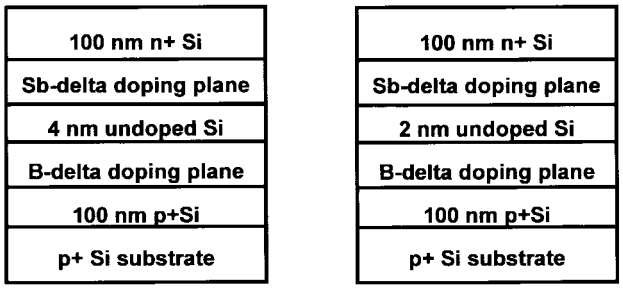

Fig. 1. Schematic diagrams of the Si RITD structures. (a) The tunnel barrier of SiTD1 is 4 nm of undoped Si. (b) The tunnel barrier of SiTD2 is 2 nm of undoped Si.

The key differences between the RITD's studied here and the previously reported Si/SiGe/Si RITD's are 1) a purely Si tunnel barrier eliminates critical thickness issues and strain associated with SiGe alloys, 2) strain relaxation during the RTA heat treatments is avoided, and 3) quantum confinement is not aided by the presence of a heterojunction discontinuity. The two structures presented, which will be referred to as SiTD1 and SiTD2, are shown in Fig. 1. The only variation between the two structures is the tunnel barrier thickness, which is 4 nm of undoped Si for SiTD1 and 2 nm of undoped Si for SiTD2. As with the previously reported Si/$Si_{0.5}Ge_{0.5}$/Si RITD's, B and Sb δ-doped injectors are used to create confined states in the valence and conduction bands, respectively. Fig. 2 shows a calculated band diagram for SiTD1. The δ-doped regions are assumed broadened over 1 nm with a dopant activation of 50%. The diagram was generated by solving the effective-mass Schrödinger equation and corresponding quantum charge for each band and iterating to convergence with Poisson's equation. As evidenced in this diagram, the built-in voltage drops across the intrinisic region. This region,

Manuscript received December 18, 1998; revised April 5, 1999. This work was supported by DARPA/AFOSR (F49620-96-C-0006) and by the National Science Foundation (ECS-9624160 and ECS-9622134).

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Publisher Item Identifier S 0741-3106(99)05665-7.

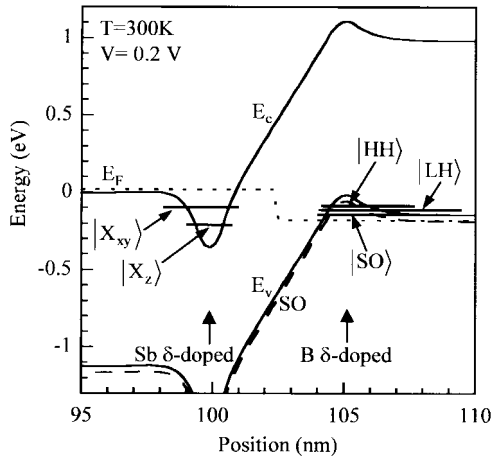

Fig. 2. Calculated energy band diagram and resonant states of SiTD1. The Sb and B activation of the δ-doped regions is assumed to be 50%. X_z denotes the conduction band minimums along the k_z axis of the Brillouin zone, and X_{xy} denotes the conduction band minimums along the k_x and k_y axes where z is the growth direction. SO denotes the split-off valence band-edge.

therefore, is also treated as the tunnel barrier. As Si has an indirect bandgap, the peak current in this structure is attributed to phonon assisted tunneling between the X_{xy} electron and light hole states [9]. The NDR in this structure results from a decrease in the tunneling probability with applied bias as these bands uncross.

II. Experimental Setup

Epitaxial growth was achieved with a specially designed MBE growth system [10] using elemental Si and Ge in e-beam sources, elemental Sb in a standard Knudsen cell and elemental B in a high-temperature Knudsen cell. The structures were grown on 75-mm B-doped ($\rho = 0.015$–$0.04\ \Omega$·cm) Si(100) wafers. Prior to growth, the substrates were prepared using a cleaning technique previously described [11]. The growths were initiated with a 2-nm undoped Si buffer layer grown at 700 °C. The substrate temperature was then lowered to 540 °C for the growth of a 70-nm B-doped p^+-Si (2×10^{19}/cm^3) layer. The substrate temperature was further reduced to 370 °C for the remainder of the sample growth. This included a B δ-doped layer (7×10^{13}/cm^2), an undoped tunneling barrier (see Fig. 1), an Sb δ-doped layer (3×10^{14}/cm^2), and a 100-nm Sb-doped n^+-Si (4×10^{19}/cm^3) contact layer. All regions of the sample were grown at a rate of 0.1 nm/s. Furthermore, with the exception of the lack of Ge in SiTD1 and SiTD2, their growth and doping was essentially identical to that of the previously reported $Si/Si_{0.5}Ge_{0.5}/Si$ RITD's.

A series of samples were annealed under a 15% H_2 85% N_2 ambient in an AG Associates Heatpulse 610 Rapid Thermal Annealing Furnace. The anneal time of all samples was fixed at one minute. Anneal temperatures of 500, 550, 600, 650, and 700 °C were employed in this study. Control samples without heat treatment were also fabricated for SiTD1 and SiTD2.

Al dots with diameters of 5, 10, 18, 50, and 75 μm were patterned on the surface of the wafer via a standard contact lithography/liftoff process. The samples were dipped in a buffered oxide etch prior to metallization to remove the native oxide. The Al dots served as a mask when the samples were etched in a CF_4/O_2 plasma for mesa isolation. Finally, an Al backside contact was thermally evaporated to complete the device fabrication.

TABLE I
Summary of the Room Temperature $I-V$ Characteristics of the Si RITD's for SiTD1 and SiTD2. Results From 18 μm Diameters Diodes From Substrates Annealed at 1 min are Shown. A PVCR Entry of 1.00 Indicates that the Device Exhibited a Plateau in the Forward Direction Rather than NDR Behavior

	T (°C)	500	550	600	650	700
SiTD1	J_p (kA/cm^2)	1.60	0.61	1.36	0.87	0.17
	J_v (kA/cm^2)	——	0.52	0.98	0.65	0.15
	PVCR	1.00	1.15	1.38	1.35	1.15
SiTD2	J_p (kA/cm^2)	32.00	15.8	9.40	1.40	0.46
	J_v (kA/cm^2)	27.0	14.8	6.28	1.28	0.41
	PVCR	1.17	1.07	1.45	1.1	1.1

III. Results and Discussion

Room temperature current–voltage (I–V) chacteristics were measured both with an HP 4142 Semiconductor Parameter Analyzer and a Textronix curve tracer. In contrast to the previous study, NDR behavior was observed in the control samples which were not heat treated. However, NDR was only evident in the 5- and 10-μm diameter diodes of the control samples, and the observed PVCR from these samples was barely greater than one. Post-growth heat treatments substantially improved the device performance.

Table I summarizes the peak current density (J_p), valley current density (J_v), and PVCR of 18 μm diameter diodes resulting from each anneal temperature employed on SiTD1 and SiTD2. The largest combination of J_p and PVCR occurred after a 600 °C, 1-min anneal for both SiTD1 and SiTD2; a PVCR of 1.38 with a J_p of 1.36 kA/cm^2, and a PVCR of 1.45 with a J_p of 9.4 kA/cm^2 were observed for SiTD1 and SiTD2, respectively. Anneal temperatures above this optimal value led to lower values of J_p. It should also be noted that the degradation of Si RITD's occurred at an anneal temperature 100 °C below that of the $Si/Si_{0.5}Ge_{0.5}/Si$ RITD study [8], possibly because the diffusion of B is more rapid in bulk Si than in $Si_{1-x}Ge_x$ alloys [12].

Spacer thickness had a significant influence on J_p and v. Fig. 3 shows an overlay of the I–V characteristics of 10 μm diameter diodes from SiTD1 and SiTD2, both annealed at a temperature of 600 °C for 1 min. The current density of SiTD2 (10.8 kA/cm^2) is almost an order of magnitude larger than that of SiTD1 (1.42 kA/cm^2). Since the devices were grown under identical conditions with the exception of spacer thickness, the elevated current density of SiTD2 must be due to its thinner spacer. The fact that all entries from SiTD1 in Table I have smaller J_p and J_v values than corresponding entries from SiTD2 reinforces this conclusion. However, a reduction in spacer thickness did not yield as sharp of an increase in current density as the authors originally suspected. The may suggest that the depletion region for these structures extends beyond the δ-doping planes. With proper adjustments to the doping levels and to growth parameters, this problem may be avoided.

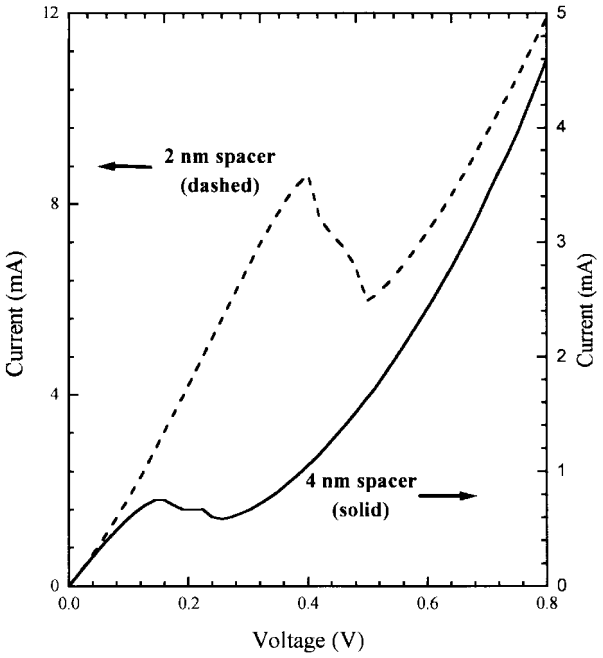

Fig. 3. $I-V$ characteristics of Si RITD's with 4-nm (SiTD1) and 2-nm (SiTD2) tunnel barriers. The current from the 2-nm structure and 4-nm structures are plotted on the left and right axes, respectively. The diodes shown have a 10-μm diameter and were annealed at 600 °C for 1 min. The 4-nm device had a PVCR of 1.42 with a J_p of 1.42 kA/cm^2. The 2-nm device had a PVCR of 1.41 with a J_p of 10.8 kA/cm^2.

The variation in peak voltage evident in Fig. 3 is attributed to the series resistance of the Al contacts.

A burn-in study was performed on a portion of SiTD2 annealed at 600 °C. The devices on this sample were cycled between -1.5 and 1.5 V at a rate of 18 cycles/s for the first 20 500 cycles. The rate was then increased to 42 cycles/s for the duration of the measurements. A 0.47% reduction in J_p and J_v was observed over the first 20 500 cycles. The $I-V$ charactertistics then remained essentially unchanged after 83 800 cycles.

IV. Conclusion

In conclusion, Si RITD's were fabricated epitaxially and found to exhibit NDR behavior at room temperature. PVCR's up to 1.42 with a J_p as high as 1.42 kA/cm^2 and up to 1.41 with a J_p as high as 10.8 kA/cm^2 were observed after a 1-min 600 °C anneal for 4- and 2-nm undoped Si spacers, respectively. The current density of the RITD's was found to depend on the thickness of the undoped Si spacer, allowing for engineering of the peak current density for specific device applications. Optimal anneal conditions may be affected by the interdiffusion of dopants, as device degradation occurred 100 °C below the 700 °C, 1-min optimal anneal previously reported for Si/SiGe/Si RITD's. The devices withstood a burn-in study which demonstrated their reliability for circuit operation. The device structure, as well its low temperature fabrication process makes it a strong candidate for integration in a CMOS or HBT fabrication line.

Acknowledgment

The authors would like to thank C. Guedj (University of Delaware) for X-ray diffraction, D. S. Simons (NIST) for secondary ion mass spectrometry, M. Twigg (NRL) for high-resolution transmission electron microscopy, and Astropower Inc. for help in device fabrication. NEMO software was used to calculate the structure of the band diagrams. In addition, the authors wish to recognize J. Kolodzey (University of Delaware) and G. Pomerenke (DARPA/ETO) for their guidance and support.

References

[1] T. P. E. Broekaert, B. Brar, J. P. A. van der Wagt, A. C. Seabaugh, T. S. Moise, F. J. Morris, E. A. Beam, III, and G. A. Frazier, "A monolithic 4-bit 2-Gsps resonant tunneling analog-to-digital converter," *IEEE J. Solid State Circuits*, vol. 33, pp. 1342–1349, 1998.

[2] A. C. Seabaugh, B. Brar, T. Broekaert, F. Morris, and G. Frazier, "Resonant tunneling analog/mixed signal circuit technology," *Top. Workshop Heterostructure Microelectronics for Information Systems Applications*, 1998, pp. 14–15.

[3] J. P. A. van der Wagt, A. C. Seabaugh, and E. A. Beam, III, "RTD/HFET low standby power SRAM gain cell," *IEEE Electron Device Lett.*, vol. 19, pp. 7–9, 1998.

[4] J. P. A. van der Wagt, "Tunneling-based SRAM," *Proc. IEEE*, vol. 87, pp. 571–595, 1999.

[5] V. M. Franks, K. F. Hulme, and J. R. Morgan, "An alloy process for making high current density Si tunnel diode junctions," *Solid State Electron.*, vol. 8, pp. 343–344, 1965.

[6] R. G. Swartz, "In perspective: The tunnel diode," in *1986 IEEE Int. Solid-State Circuits Symp.*, pp. 278–280.

[7] K. Ismail, B. S. Meyerson, and P. J. Wang, "Electron resonant tunneling in Si/SiGe double barrier diodes," *Appl. Phys. Lett.*, vol. 59, pp. 973–975, 1991.

[8] S. L. Rommel, T. E. Dillon, III, M. W. Dashiell, H. Feng, J. Kolodzey, P. R. Berger, P. E. Thompson, K. D. Hobart, R. Lake, A. C. Seabaugh, G. Klimeck, and D. K. Blanks, "Room temperature operation of epitaxially grown Si/$Si_{0.5}Ge_{0.5}$/Si resonant interband tunneling diodes," *Appl. Phys. Lett.*, vol. 73, pp. 2191–2193, 1998.

[9] N. Holonyak, I. A. Lesk, R. N. Hall, J. J. Tiemann, and H. Ehrenreich, "Direct observation of phonons during tunneling in narrow junction diodes," *Phys. Rev. Lett.*, vol. 3, pp. 167–168, 1959.

[10] E. D. Richmond, J. G. Pellegrino, M. E. Twigg, S. Qadri, and M. T. Duffy, "Unique properties of molecular beam epitaxy on sapphire using *in-situ* high temperature substrate annealing compared with chemically vapor deposited silicon on sapphire," *Thin Solid Films*, vol. 192, pp. 287–294, 1990.

[11] P. E. Thompson, M. E. Twigg, D. J. Godbey, K. D. Hobart, and D. S. Simons, "Low-temperature cleaning processes for Si molecular beam epitaxy," *J. Vac. Sci. Technol. B*, vol. 11, pp. 1077–1082, 1993.

[12] P. Kuo, J. L. Hoyt, J. F. Gibbons, J. E. Turner, and D. Lefforge, "Effects of strain on boron diffusion in Si and $Si_{1-x}Ge_x$," *Appl. Phys. Lett.*, vol. 66, pp. 580–582, 1995.