Development of δB/i-Si/δSb and δB/i-Si/δSb/i-Si/δB Resonant Interband Tunnel Diodes For Integrated Circuit Applications

Sean L. Rommel, Niu Jin, T. E. Dillon, Sandro J. Di Giacomo, Joel Banyai, Bryan M. Cord, C. D'Imperio, D. J. Hancock, N. Kirpalani, V. Emanuele, Paul R. Berger, Phillip E. Thompson,[a] Karl D. Hobart,[a] and Roger Lake[b]

University of Delaware, Department of Electrical and Computer Engineering, Newark, DE 19716-3130

[a]Naval Research Laboratory, Washington, D.C. 20375, [b]Raytheon Systems, Dallas, TX 75243

Recent developments in Si based tunnel diode technologies have made the realization of circuits incorporating both tunnel diodes and transistors feasible [1-2]. Memory circuits incorporating low current density double barrier resonant tunneling diodes (DBRTDs) [3] have been demonstrated with fewer transistors and lower power dissipation than conventional CMOS SRAM or DRAM circuitry. High current density DBRTDs, in contrast, have been shown to improve the speed and power of logic circuitry such as multiplexers [4] and analog-to-digital converters [5]. However, such technology will never reach mainstream CMOS or SiGe HBT technology unless a suitable Si-based negative differential resistance (NDR) device can be developed.

A recent study by the authors presented the design of an n-on-p Si RITD layer with a peak-to-valley current ratio (PVCR) of 2.15 at a current density of 3 kA/cm^2 which was grown by molecular beam epitaxy (MBE) [6]. The schematic diagram of this structure, which is used as the base sample in the present study, is shown in Fig. 1, and the current-voltage (I-V) characteristics of this layer are shown in Fig. 2. Follow-up studies on this structure investigated additional tunnel barrier thicknesses of 4 nm, 8 nm, and 10 nm. In all samples, room temperature NDR was observed comparable to that of the baseline 6 nm RITD. Fig. 3 illustrates the exponential dependence of the current density on the tunnel barrier thickness. This figure clearly shows that simple adjustments to the tunnel barrier thickness can be made to tailor the performance for a particular circuit application.

However, growth of a complimentary p-on-n tunnel diode is problematic due to Sb segregation through the intrinsic tunneling spacer. This would result in unintentional incorporation and increased compensation by the segregated Sb and hence lower PVCR. A study, which will be published elsewhere, details a growth technique which overcomes these difficulties. The solution is to control the Sb segregation by employing multiple substrate temperatures during MBE growth. The Sb δ-doping plane is first deposited at 320°C. This will minimize the degree of segregation, and ensure that a large percentage of dopants incorporate into the lattice during the growth of the Sb δ-doping plane. The Sb flux will then terminate, and a fixed length of Si (referred to as L1) will be grown at 320°C. The Si flux will then be terminated for a stop growth. At this point, the substrate temperature is then *elevated* for the remainder of the sample growth, including the deposition of the B δ-doping plane. Thus, rather than dropping the substrate temperature to suppress Sb segregation, the substrate temperature is elevated to promote segregation while simultaneously minimizing Sb incorporation. Fig. 6 illustrates this process for the case which yielded the best results, an L1 length of 5 nm, and a length of 3 nm after the stop growth and prior to the B δ-doping plane. Fig. 5 shows the I-V characteristics of the p-on-n sample annealed at 575°C, 1 min. Note that the resulting PVCR of 2.1 and peak current density of 1.1 kA/cm^2 are comparable to that of the n-on-p 6 nm RITD shown in Fig. 1.

Following the success of the complementary p-on-n growth strategy, it was now possible to demonstrate the integration of two tunnel diodes in a single growth. The basic flow and design presented here follow that of III-V RITDs [7], presenting a symmetric pnp RITD structure. The motivation for developing this structure was to mimic the I-V characteristic of III-V RTDs which have NDR regions under forward and reverse bias. A Si-based structure with these properties would facilitate the development of a Goto-type memory cell [8]. Ideally, the PVCR and peak current density of the forward and reverse NDR regions should be nearly identical if the structure grown is symmetrical.

Fig. 6 shows the ideal structure which in essence consists of two 6 nm Si RITD layers. As Fig. 6 illustrates, the growth of this sample combines the growth procedures for the devices shown in Figs. 1 and 4. Fig. 7 shows the I-V characteristics resulting from a 600°C, 1 min anneal for the pnp RITD. Note that when a forward bias is applied, the device nearer the surface (the top diode) will be under forward bias, and when a reverse bias is applied with respect to the layers, the device nearer the substrate (the bottom diode) will be under forward bias. As theorized, NDR is clearly present in the forward and reverse directions with a PVCR of 1.67 for the top diode and 1.37 for the bottom diode. An asymmetry is clearly present in the layer as the current density of the bottom diode (5.7 kA/cm^2) is over double that of the top diode (2.6 kA/cm^2). With growth modifications it should be possible to achieve a symmetric I-V characteristic.

This simple example of integration has demonstrated that it is relatively straightforward to combine two growth templates in a single epitaxial run. An obvious extension to this study would be the growth of a Si/SiGe heterojunction bipolar transistor with a tunnel diode placed on the emitter for high frequency mixed signal applications. Relatively few changes to the growth template would be required to make the structure work. In conclusion, a variety of Si-based tunnel diode structures configured to meet the needs of a CMOS environment have been demonstrated.

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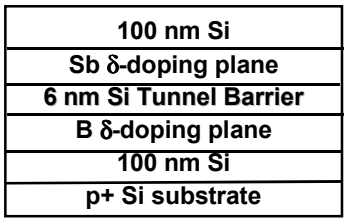

Fig. 1. Device schematic of a Si RITD structure. This device lacks bulk doping to enhance quantum confinement. A family of devices with this structure were grown with spacers of 4 nm, 6 nm, 8 nm, and 10 nm.

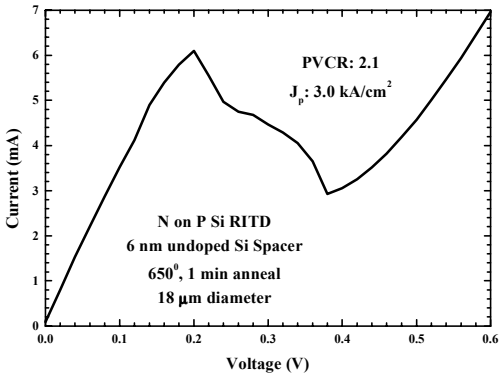

Fig. 2. I-V Characteristics of the 6 nm n on p Si RITD annealed at 650°C, 1 min. At this temperature, a PVCR of 2.05 at a peak current density of 3.0 kA/cm^2 was observed.

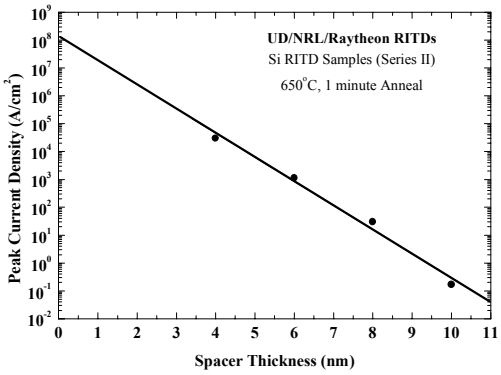

Fig. 3. Semilog plot of the peak current density resulting from various barrier thickness. Four orders of magnitude in current density are represented in this plot.

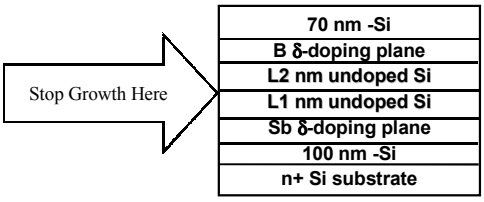

Fig. 4. Schematic diagram of the structure examined in the complimentary growth study. 3 nm of Si were grown at 320°C, and 5 nm of Si were grown at 550°C. Because of segregation, the resulting device is comparable to the 6 nm Si RITD in Fig. 1.

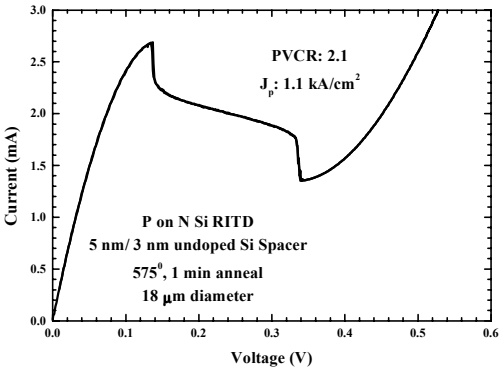

Fig. 5. I-V characteristics of an 18 μm diameter diode from the p on n sample with L1=5 nm, L2=3 nm. A PVCR of 2.1 at a peak current density of 1.1 kA/cm^2 is observed. The diode was annealed at 575°C for 1 min.

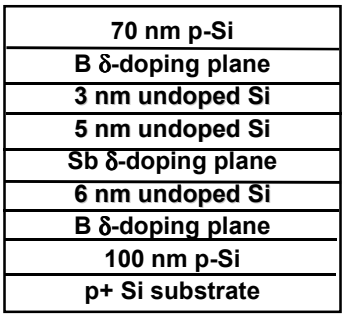

Fig. 6. Schematic diagram of the PNP RITD layer. Ideally this layer consists of a pair of back-to-back 6 nm Si RITDs.

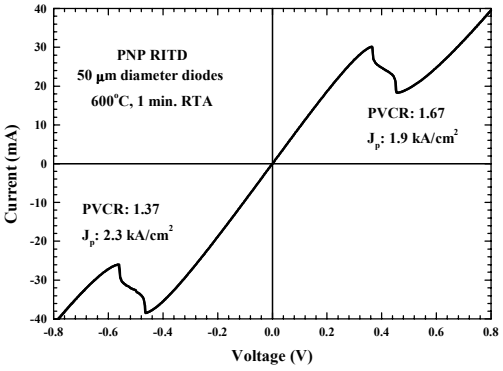

Fig. 7. I-V characteristic of the PNP RITD layer. Two NDR regions are observed. Under forward bias, a PVCR of 1.67 at a peak current density of 2.6 kA/cm^2 is observed. Under reverse bias, a PVCR of 1.37 at a peak current density of 5.7 kA/cm^2 is observed. The asymmetry in the current density is attributed to growth variations. The diodes presented were annealed at 600°C, 1 min.