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Integration of Si/SiGe HBT and Si-based RITD demonstrating controllable negative differential resistance for wireless applications

Sung-Yong Chung [a], Si-Young Park [a], Jeffrey W. Daulton [a], Ronghua Yu [b], Paul R. Berger [a,b,*], Phillip E. Thompson [c]

[a] *The Ohio State University, 205 Dreese Laboratory, Department of Electrical and Computer Engineering, 2015 Neil Avenue, Columbus, OH 43210, USA*
[b] *The Ohio State University, Department of Physics, Columbus, OH 43210, USA*
[c] *Naval Research Laboratory, Code 6812, Washington, DC 20375, USA*

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Abstract

Si-based resonant interband tunnel diodes (RITD) were monolithically integrated with Si/SiGe heterojunction bipolar transistors (HBT) on silicon substrates effectively creating a 3-terminal negative differential resistance (NDR) device. We demonstrate that the room temperature NDR in the I_C–V_{EC} characteristics under common emitter configuration can be controlled by a third terminal which is the basis of the integrated circuit. The estimated NDR values from the DC *I*–*V* characteristics, assuming that the NDR is linear, can be varied from about −27.5 Ω to −180 Ω with respect to V_{CE} in the range of 0.96 V–1.16 V.
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1. Introduction

Low power consumption concurrently with high-speed performance is a key for next generation portable wireless applications including satellite communications. Devices such as tunnel diodes that exhibit negative differential resistance (NDR) in their current–voltage characteristics are very useful for circuit applications such as high-speed mixed signal and ultra-fast logic/memory with low power consumption. To date, applications using tunnel diodes that have been demonstrated include voltage-controlled oscillators [1,2], A/D converters [3,4], frequency dividers [5,6], sampling [7], memory [3,8], logic circuitry [5,9], etc. All these applications derive benefit from the intrinsic negative resistance of NDR devices which can also reduce power consumption by the reduction of circuit complexity and therefore device count. Furthermore, since the tunneling phenomenon is a majority carrier effect, the speed of circuits incorporating NDR devices can be much faster.

The most representative NDR devices are tunnel diodes. However, the utility of two terminal tunnel diodes themselves in circuits has several drawbacks such as input/output isolation, poor controllability, and vulnerability to the growth and fabrication procedure. Therefore, the use of transistors in conjunction with tunnel diodes by providing a third terminal with NDR devices will overcome the drawbacks described above and extend the useful range of NDR device based circuit applications. These types of

* Corresponding author. Address: The Ohio State University, 205 Dreese Laboratory, Department of Electrical and Computer Engineering, 2015 Neil Avenue, Columbus, OH 43210, USA. Tel.: +1 614 247 6235; fax: +1 614 292 7596.
E-mail address: pberger@ieee.org (P.R. Berger).

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hybrid circuits have already been demonstrated in many III–V compound semiconductor material systems mostly by the integration of unipolar resonant tunnel diodes (RTDs) with HBTs [1,5,10] or high electron mobility transistors (HEMT) [2–4,6]. However, despite the better performance of III–V-based NDR devices stemming from their different material properties such as a direct band gap, or large heterojunction band offsets, etc., such technology is not readily compatible with the mainstream platforms of complementary metal oxide semiconductor (CMOS) and Si/SiGe heterojunction bipolar transistor (HBT) technologies unless a suitable Si-based NDR device and compatible integration technology with existing Si-based CMOS or HBT devices is available.

The first Si-based tunnel diode integration was demonstrated using a Si/SiGe resonant interband tunnel diodes (RITDs) with a Si/SiGe HBT [11]. The resulting circuits showed the distinguishing characteristics of adjustable PVCR and PCD corresponding to the NDR by the control of the HBT base current. This enabled a 3-terminal NDR device and was the first report of a monolithic Si-based resonant bipolar tunneling transistor (RBT). This embodiment utilized interband tunneling versus the intraband tunneling via resonant tunneling diodes (RTD) utilized by III–V resonant tunneling transistors (RTT) [1,5,10].

This study extends the preliminary work of the authors [11], presenting an improved Si/SiGe-based RITD–HBT integration. The RITD–HBT integration discussed here shows the capability to adjust the NDR values by the control of the base current which is a third terminal of the integration as well as a greatly reduced series resistance. The estimated NDR values of the integrated RITD–HBT from DC I–V characteristics, assuming that NDR is linear, varies from about $-27.5\ \Omega$ to $-180\ \Omega$ with respect to V_{CE} in the range of 0.96 V–1.16 V. Two issues related to the improvement of the integration will be discussed: (1) reducing a large non-linear series resistance originating from the backward diode that is necessary to connect two bipolar devices in series without also introducing a reverse biased parasitic rectifying diode in between; (2) improving the gain of the SiGe HBTs. Included in this study is the load line analysis of the RITD–HBT integration for better understanding.

2. Structure design and process

The overall RITD–HBT structure, as shown in Fig. 1(a), consists of three intrinsic devices that are vertically stacked such that an n-on-p RITD is placed on top, an n–p–n HBT on bottom, and a p-on-n backward diode between the two devices.

A tandem of an n-on-p RITD on an n–p–n HBT is necessary for the RITD to modulate the current transport across the HBT emitter under forward active operation in the common emitter configuration (refer to Fig. 1: $V_{BE} > 0$, $V_{EC} > 0$, $V_{BC} > 0$) where the n-on-p RITD needs to be forward-based to make the NDR region appear. However, since both the RITD and HBT are bipolar devices, placing an n-on-p RITD directly atop the n-type of HBT emitter creates a parasitic diode between the two bipolar devices, which blocks current flow as it is reverse-biased under forward active operation. Therefore, inserted between the RITD and the emitter of the HBT was a backward diode which will be reverse-biased under HBT forward bias active operation in the common emitter configuration. The backwards diode effectively connects the top RITD and the bottom HBT appearing as a small series resistance for the vertically integrated RITD–HBT circuit.

The entire vertically integrated RITD–HBT structures were grown by low temperature molecular beam epitaxy (LT-MBE) using elemental Si and Ge in electron-beam sources on Sb-doped ($\rho = 0.008$–$0.018\ \Omega\,$cm) Si(100) substrates. Two different n-type dopants, P and Sb were

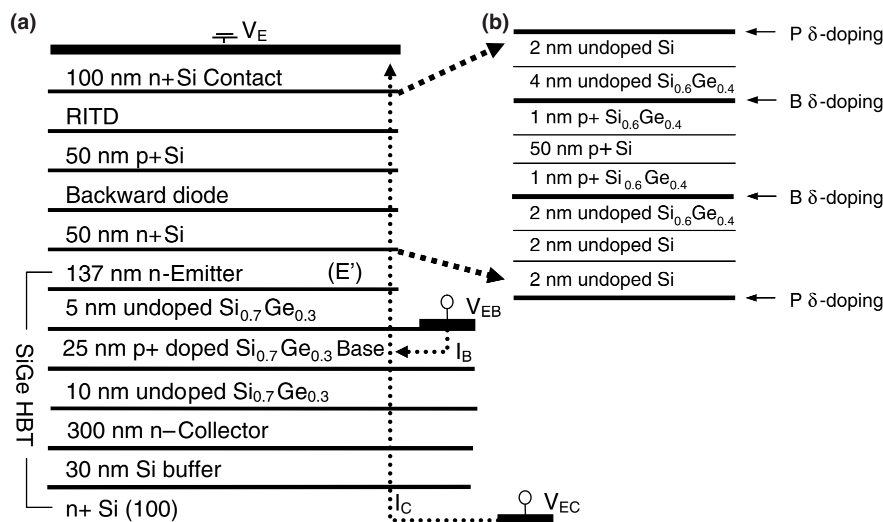

Fig. 1. The schematic of the RITD–HBT layer structure consisting of three intrinsic devices such that the n-on-p RITD is placed on top, the n–p–n HBT on bottom, and the p-on-n backward diode between the two devices. The detailed structure for the RITD and the backward diode is shown separately.

chosen for this study such that Sb was the n-type dopant for the n–p–n HBT layer growth and P was the n-type dopant for the remaining backward diode and the RITD layers, which also require δ-doping concentrations. B was used as the p-type dopant.

The generic structure of the n–p–n HBT is shown in Fig. 1 [12]. Using the highly Sb-doped substrate as the sub-collector (its doping level is in the range of $1.5\times10^{18}\,cm^{-3}$–$5\times10^{18}\,cm^{-3}$), more than 300 nm including Si buffer layers of n-collector doped by Sb at $5\times10^{16}\,cm^{-3}$ was grown. The total 40 nm of SiGe base layer including undoped SiGe cladding layers was grown using a box shape Ge profile with 30% of Ge. The resulting SiGe layer is biaxially tensially-strained which should create about 0.22 eV of band offset in the valence band at both the emitter–base and the base–collector heterojunctions. Sandwiched by undoped SiGe spacer layers to suppress B outdiffusion during the growth and subsequent processing was the 25 nm B-highly doped ($2\times10^{19}\,cm^{-3}$) base layer. The Si emitter layer was grown atop the SiGe base layer using Sb with a doping level of $1.0\times10^{18}\,cm^{-3}$.

The backward diode in the previous study [11] was formed directly between the p+ injector layer of the top RITD and the n+ emitter layer of the n–p–n HBT, which is essentially a p–n junction with doping levels of $5\times10^{19}\,cm^{-3}$ each and with no intrinsic spacer between the p and n sides. The relatively low doping density on both sides, plus inevitable dopant diffusion during the 800 °C 1-min post-growth rapid thermal annealing (RTA), resulted in a wide tunneling barrier and therefore a large non-linear resistance. This unfavorably shifted the peak voltage and created hysteresis in the current–voltage measurements under the common emitter configuration. In this study, a δ-doped backward diode is instead inserted to obtain a significantly higher doping density with a thinner tunneling barrier, as shown in Fig. 1. Both the B and P δ-doping layers have a sheet carrier concentration of $2.5\times10^{13}\,cm^{-2}$. A 6 nm intrinsic spacer is inserted between the δ-doping layers to prevent dopant interdiffusion and compensation [13]. However, it is problematic to grow B-doped layers directly on top of a P δ-doping layer due to P segregation. Segregated P atoms will incorporate into the overlayer and lead to unintentional doping and a compensated B doped layer which will result in a smaller effective carrier density. To minimize the effect of P segregation on both the backward diode and the upper RITD, a stop growth technique associated with a substrate temperature reduction to 320 °C to control the P segregation [14] was employed.

A SiGe RITD was grown atop the backward diode. The structure of the Si-based RITD was designed based on previous work [15,16] developed by the authors. For this state-of-the-art Si-based RITD, several key points employed are: (i) δ-doped injectors to create defined quantum wells, (ii) a composite intrinsic tunneling barrier to effectively clad the δ-doped spike, (iii) low temperature MBE (LT-MBE) growth to suppress segregation and diffusion, and (iv) post-growth rapid thermal anneal (RTA) heat treatment to reduce point defects created during the LT-MBE process [17]. Details on RITD growth are reported elsewhere [15,16]. It is noted that only one post-growth RTA treatment at 800 °C for 1 min was performed after the completion of the entire RITD–HBT growth.

The fabricated RITD–HBTs employed a double mesa structure. They were fabricated using conventional photolithography and a self-aligned emitter process. Initially, the emitter metal (Cr/Au), which also acts as the anode metal for the RITD, was defined by a lift-off process. It acts as an etch mask for the emitter and RITD mesa etching. Two different wet chemical etches are required to form the emitter and RITD mesa. For a conventional SiGe HBT using a double mesa, a KOH wet echant has been commonly used to selectively etch the Si emitter and stop etching at the SiGe base layer. However, due to the SiGe spacer layers incorporated into the RITD structure, the RITD active region was first etched using the non-selective $HF/HNO_3/H_2O$ (1:100:100) wet etchant. Then, the etching was switched back to the selective KOH wet etchant below the RITD to effectively stop at the SiGe base region. The undercut of the emitter and RITD mesa etching procedure is sufficient to provide a self-aligned base metal (Pt/Au) to the emitter mesa by shadow masking. Using photo-lithographically defined photoresist as an etch mask to protect the self-aligned emitter–base region, the base mesa etching was performed using an $HF/HNO_3/H_2O$ (1:100:100) wet etchant for the active device isolation. The collector ohmic contact (Ti/Au) was made on the backside of the substrate.

3. Results and discussion

Fig. 2 shows the base/emitter *I–V* characteristics of the RITD–HBT measured at room temperature with the collector open. Shown in the inset of Fig. 2 are the *I–V* characteristics of a representative RITD having the same layer structure which was grown under the same conditions and experienced the same post-growth thermal budget as utilized in this RITD–HBT integration study. The measured emitter–base junction size in Fig. 2 is $6\times40\,\mu m^2$. The NDR modulation at around 1.0 V is the result of resonant interband tunneling of electrons through the forward-biased RITD, serially with the reverse-biased backward diode, and the forward-biased intrinsic emitter–base junction of the HBT (Here, the emitter is referred to as the top of the RITD–HBT while the intrinsic emitter is referred to as the emitter of the HBT only, E' in Fig. 1). The peak current density is about $1.7\,kA/cm^2$, which is similar to the RITD in the inset of Fig. 2. The slight discrepancy is possibly due to non-identical growth and/or fabrication conditions. Unlike the discrete RITD shown in the inset of Fig. 2, when the emitter–base junction of the integration is reverse-biased, the *I–V* characteristics are saturated because the reverse-biased intrinsic emitter–base junction of the HBT blocks current flow. The high peak voltage, 1.8 V, previously observed [11] in the *I–V* characteristics is now greatly reduced to 1.0 V as a result of the revised backward diode structure.

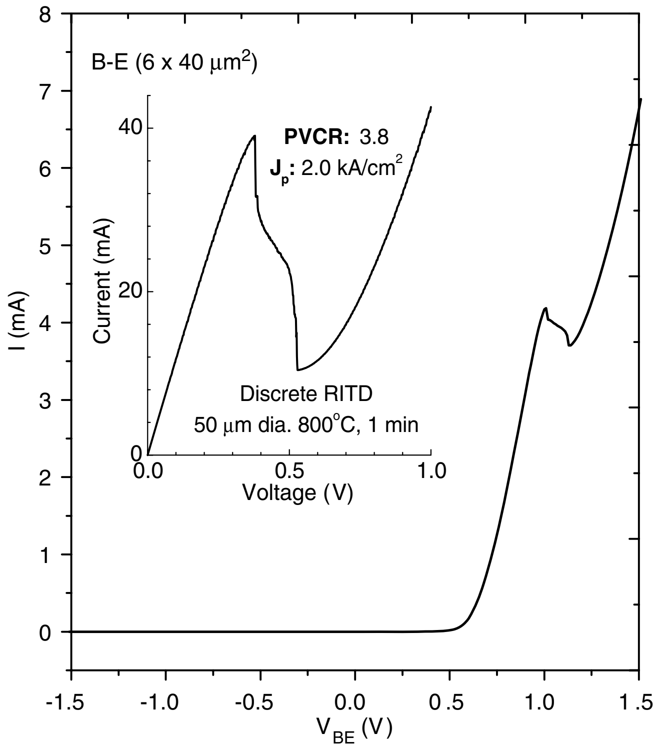

Fig. 2. The base–emitter junction *I*–*V* characteristics of the RITD–HBT with the collector open measured at room temperature in which the RITD and backward diode are coupled between the base and emitter. Shown in the inset are the *I*–*V* characteristics of a representative discrete RITD having the same structure.

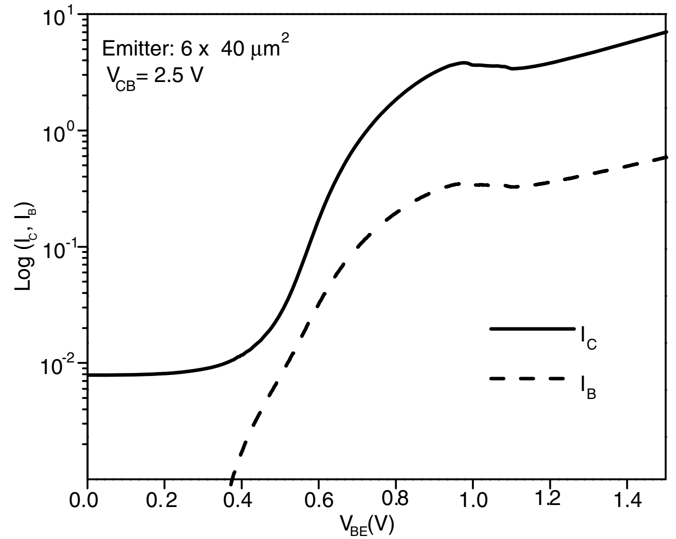

Fig. 4. The Gummel plot displaying the measured I_B and I_C in logarithmic scale with the base–emitter junction reverse-biased at $V_{BC} = 2.5$ V. It shows that both I_B and I_C are modulated by the NDR property of the RITD.

Fig. 3 shows that the collector current (I_C) versus voltage (V_{CE}) characteristics as measured at room temperature for the common emitter configuration (see the inset) as a function of the base current, I_B. When I_B is less than 400 μA, the characteristics are similar to those of a conventional bipolar transistor. With I_B larger than 400 μA, it is observed that the NDR characteristics which are due to the combined effects of the RITD current limiter coupled with the emitter of the HBT and the control of the HBT through the base current. The Gummel plot, shown in Fig. 4, displays the measured I_B and I_C in logarithmic scale with the base–emitter junction reverse-biased at $V_{BC} = 2.5$ V. It clearly shows that both I_B and I_C are modulated by the NDR property of the RITD. The maximum current gain of 15 obtained from the Gummel plot is nearly 10 times higher than the HBT in the previous report. Compared to Chung et al. [11], this improvement is due to (1) the reduced defect densities by switching n-type dopants from P to Sb and by increasing the substrate growth tem-

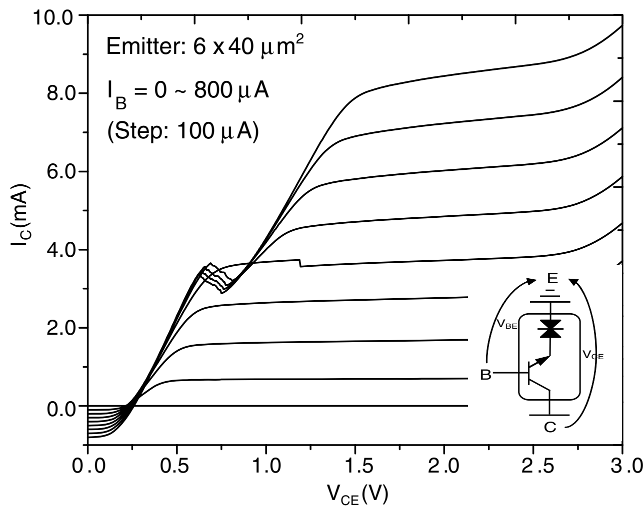

Fig. 3. I_C–V_{CE} characteristics as measured at room temperature for the common emitter configuration (see the inset) with base current, I_B, as a parameter. (Emitter size of 6×40 μm^2).

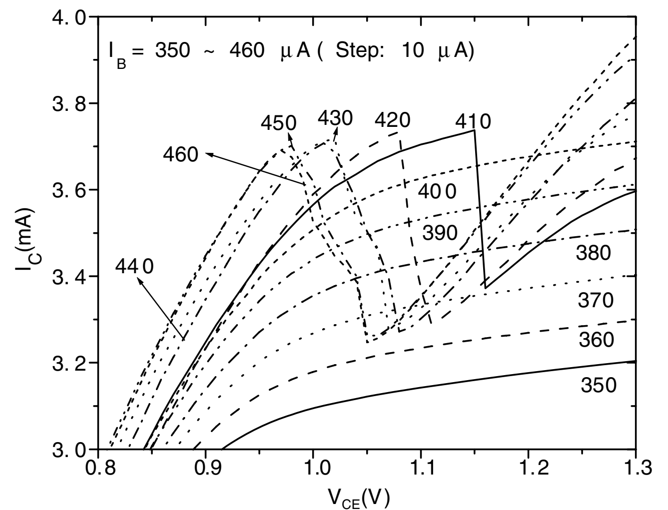

Fig. 5. Measured common emitter *I*–*V* characteristics showing the monolithically integrated RITD/HBT enables a direct adjustment of the NDR values by the control of I_B.

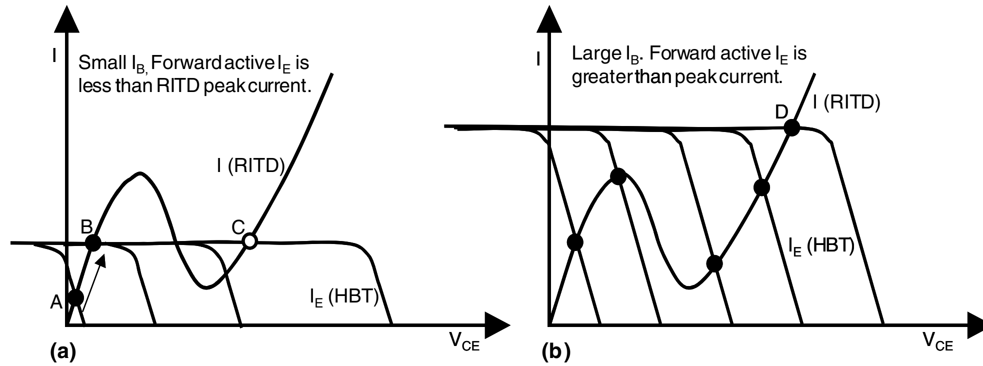

Fig. 6. RITD and HBT emitter current load lines for fixed base current, I_B: (a) low I_B showing bistable latching behavior and (b) large I_B showing the NDR appearance in I_C.

perature for the base layer growth [18], and (2) the revised SiGe base layer design from a trapezoidal Ge profile to a box shape Ge profile which results in suppression of the holes back injected into the emitter due to the greater band offset at the emitter–base heterojunction.

Fig. 5 shows that the monolithically integrated RITD/HBT circuit enables direct adjustment of the NDR magnitude by the control of I_B. When I_B varies from 410 μA to 460 μA (in steps of 10 μA), the NDR characteristics are observed for V_{CE} in the range of 0.96 V–1.16 V. The NDR region shifts toward lower V_{CE} and the magnitude of the NDR increases as I_B increases. The estimated NDR values from DC I–V characteristics shown in Fig. 5, assuming that NDR is linear, varies from about −27.5 Ω to −180 Ω. NDR modulation is due to the series resistance added by the HBT that is in series with the RITD [6]. The HBT stays in the saturation region if I_E of the HBT is larger than I_{peak} of the RITD resulting in the addition of a small series resistance to the RITD. But when I_E of the HBT is less than I_{peak}, it results in a large series resistance. No NDR would be observed for I_E less than I_{peak} unless the Early effect of the HBT is considered.

As a three-terminal NDR device, the applications of this RBT device can greatly extend SiGe HBTs from their conventional domain of high-end analog circuits in the forward active mode operation to additionally quantum functional circuits based on their NDR characteristics in the saturation mode operation, depending on its terminals' bias conditions.

4. Load line analysis and switching operation

The integrated RITD–HBT device behavior is properly explained by a load line analysis as shown in Fig. 6. This figure shows the load lines of the RITD and the emitter current, I_E, for a fixed base current, I_B. The collector current is then obtained from $I_C = I_E - I_B$. For small I_B, as shown in Fig. 6(a), the maximum forward active I_E is less than the RITD peak current. Initially, at Point A the HBT is in saturation. As V_{CE} increases, the HBT enters the forward active region and the operating point becomes fixed at B. The voltage across the RITD stays fixed and a further increase in V_{CE} is dropped across the HBT because I_B is fixed. Thus, no NDR is seen in the I_C–V_{CE} curves for small I_B as seen in Fig. 5.

For large I_B, as shown in Fig. 6(b), the maximum forward active emitter current, I_E, is greater than the RITD peak current. The HBT stays in saturation tracing out the RITD I–V, again as shown in Fig. 5. The HBT only enters the forward biased active region at Point D when the diffusion current turns on the RITD. At this point the voltage across the RITD becomes fixed and a further increase in V_{CE} is dropped across the HBT. Since the differential resistance of the HBT in saturation varies depending on the bias condition, I_B can control the NDR magnitude for the RITD–HBT. The vertical NDR observed with I_B of 410 μA in Fig. 5 is due to the base width modulation effect that leads to the gradual increase of I_E in active mode operation as V_{CE} increases.

5. Conclusion

Si-based RITDs were monolithically integrated with Si/SiGe heterojunction bipolar transistors (HBT) on silicon substrates. The NDR modulation in the I_C–V_{EC} characteristics under common emitter configuration was demonstrated by the control of the base current, a third terminal at the room temperature. The integrated RITD–HBT device behavior was analyzed by a load line analysis.

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