Fabrication of nanowires with high aspect ratios utilized by dry etching with $SF_6:C_4F_8$ and self-limiting thermal oxidation on Si substrate

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Si-based nanowires with high aspect ratios have been fabricated using an inductively coupled plasma reactive ion etching (ICP-RIE) with a continuous processing gas mixture of fluorine-based $SF_6:C_4F_8$ combined with a thermal oxidation technique. The subsequent thermal oxidation further reduced the nanowire diameter utilizing the self-limiting oxidation effect below the lithographic dimensions. Transmission electron microscopy analysis of the completed nanostructures revealed the total oxide thickness and the consumption of the Si core which determines the inner nanowire diameter. The final dimensions of the inner Si nanowire are about 600 nm tall and less than 25 nm wide using top-down processing techniques. © *2010 American Vacuum Society.*
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I. INTRODUCTION

Both top-down and bottom-up techniques are well known approaches to fabricate nanostructures for low-dimensional devices, which show tremendous promise in the emerging technological field of high performance nanoelectronics and nano-optical devices, including nanolasers,[1] nanosensors,[2] nanowires,[3,4] vertical transistors,[5] quantum dots,[6] and nanorods,[7] and tunnel field effect transistors (FETs).[8] Each methodology has its merits, with top-down being the conventional brute force approach, however with bottom-up offering an elegant self-assembly method but which struggles with yield and uniformity.

For vertical configurations, a top-down method, using precision engineering of dry etching and lithography provides accurate size, shape and placement control, is the currently preferred manufacturing route for the microelectronics industry for massive production of reliably scaled devices with extreme packing densities of computer chips. The bottom-up technique using the self-assembly or direct chemical synthesis atom-by-atom or molecule-by-molecule or even particle-by-particle shows great promise for the future. However, incorporation of the Au catalyst into the bottom-up nanowire using techniques such as the standard vapor-liquid-solid growth process is highly probable, and recent reports in the literature are indeed suggesting trace amounts of Au catalyst that are housed within the Si nanowires.[9,10] The direct detection of trace amounts of Au is quite challenging, however, given the small volume of each nanowire. But, even a small amount of Au manifests as a deep-level in Si nanowires which can severely degrade electrical performance. Furthermore, the bottom-up technique of nanowire synthesis involves uncontrollable growth mechanisms leading to many practical drawbacks such as crystallographic faceting, imprecise size and chirality, varied orientations, and even sometimes random placement[11] Therefore, a top-down process is currently more attractive for commercial nanostructure synthesis where registration and yield are demanded.

A challenge for top-down methodologies, however, is creating a plasma etching process to synthesize high aspect-ratio submicron and nanoscale dimensions, following patterning technologies such as optical and electron-beam lithographies, without concurrent sidewall damage that can compromise nanoscale device operation. The precise control of various parameters including etch chemistries, pressure, and bias power in dry plasma etching systems determines etch rate, surface morphology, and sidewall profiles.

In this article, we demonstrate a plasma etching study for nanostructures using the processing gas mixture of fluorine-based sulfur hexafluoride: ocatfluorocyclobutane ($SF_6:C_4F_8$) which contains both etch and passivation chemistries like the Bosch process.[12] However, the Bosch process utilizes a multiplexed and complicated valving recipe to etch/passivate each cycle. The Bosch process is known to create a scalloped sidewall profile which is tolerable for microstructure sized microelectro mechanical systems (MEMS) but detrimental to nanostructures.[13] Here we report on the continuous etching of nanostructures using $SF_6:C_4F_8$. Subsequent self-limiting

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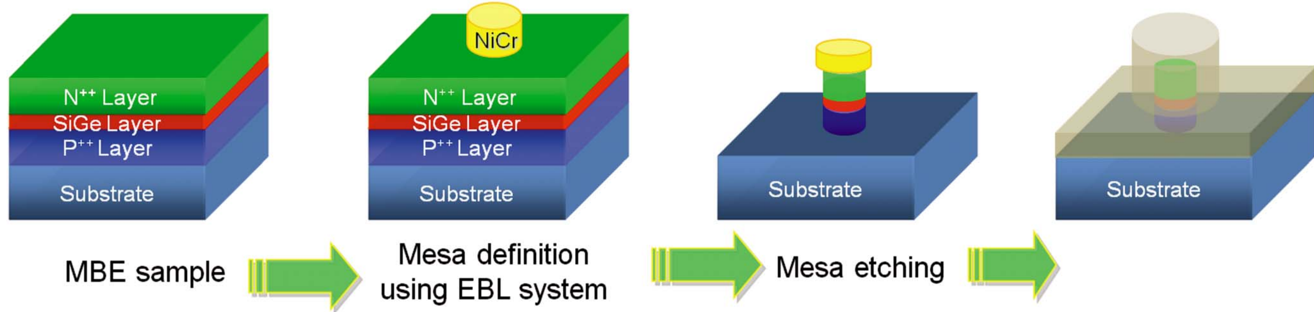

FIG. 1. (Color online) Schematic illustration of the overall process flow for the creation and inspection of the Si-based nanowires.

oxidation is provided for greater aspect ratios and is expected to greatly suppress sidewall damage by moving the interface away from the surface while providing natural passivation. This study presents silicon based vertical nanowire structures which have numerous applications, including tunnel FETs, and potential market opportunities in the future due to attractiveness to device engineers for compatibility with existing silicon processes and superior circuit potential.

II. EXPERIMENT

The multilayer nanowire material of Si and SiGe layers is epitaxially grown over the full wafer surface using molecular beam epitaxy (MBE) with elemental Si and Ge sources atop Si (100) wafers. The MBE growth was initiated with a 4 nm undoped Si buffer layer followed by a 38 nm n^{++} Si layer. Then the next layer consists of a 30 nm undoped Si buffer followed by two thin quantum wells (QWs) of $Si_{1-x}Ge_x$ as markers, each separated by 12 nm of intrinsic Si in between. The whole QW stack was then capped with an additional 30 nm undoped Si layer and finally topped with 10 nm of n^{++} Si. The QWs were nominally 1 nm thick and used a Ge percentage of 1% for the wafer reported here. The wires were then defined using a Jeol-6000 electron-beam lithography (EBL) system. A 25 nm thick layer of NiCr dots was patterned using lift-off of a bilayer stack of positive polymethylmethacrylate (PMMA) resists of different molecular weights, a 1.2% 495 000 PMMA in chlorobenzene layer was spin coated first and then a less-sensitive 2% 950 000 PMMA in anisole was applied. Subsequently, the resist was developed in a solution of methylisobutylketone (MIBK):isopropanol (IPA), followed by the electron-beam evaporation of the NiCr to define the nanowire etch masks via lift-off.

To create the desired nanowire structures, an Oxford Plasmalab 100 with ICP 180, inductively coupled plasma reactive ion etching (ICP-RIE) system was used. The ICP 180 ICP-RIE system used the $SF_6:C_4F_8$ process gases at flow rates of 20:30, respectively, where each gas flow is given in SCCM (SCCM denotes cubic centimeter per minute at STP). Other parameters included 500 W ICP power, 20 W rf power, 30 mTorr strike pressure, 10 mTorr process pressure, 10 mTorr/s ramp rate, and 20 °C stage temperature, resulting in a roughly 220 nm/min etching rate. After the etch is complete, the residual NiCr was removed in a heated HCl:DI (de-ionized) H_2O (3:1) solution for 15 min. The samples were cleaned in base-peroxide, $NH_4OH:H_2O_2:DI\ H_2O$ (1:1:5), for 10 min following another 10 min in acid-peroxide solutions, $HCl:H_2O_2:DI\ H_2O$ (1:1:5), to remove any organic contaminants and metal residues following a buffered oxide etch just prior to final oxidation.

The thermal oxidation process effectively reduced the nanowire diameter size further utilizing the self-limiting effect previously reported for three-dimensional (3D) structures.[14] The oxidation was performed in a quartz tube furnace at 1100 °C in dry O_2 ambient for 1 h that is an appropriately selected oxidation temperature and time to reach the self-limiting regime. Previous oxidations had revealed that for even lower furnace temperatures (800 °C), the nanopillar diameter increased by only $5\% \pm 10\%$ for 4 h, based on inspection with scanning electron microscopy. Thus, it is concluded that the dry 3D oxidation has entered the self-limiting oxidation regime. Figure 1 shows the schematic illustration of the overall processing flow for Si nanowire fabrication.

For transmission electron microscopy (TEM) specimen preparation, a combined method was used that began with a diamond dicing saw followed by tripod polishing to further reduce the beam shadowing created by the bulk Si substrate in the region of interest, resulting in a thin electron-transparent TEM specimen that was mounted on a Cu grid. Figure 2 shows a diagram illustrating the combined method using a dicing saw followed by tripod polishing. For the first step, the oxidized nanowires are blanket coated with 1.6 μm thick photoresist that effectively protects the wires from damage during the sawing process. The second step is dicing to separate the nanopillars from the rest of the substrate with

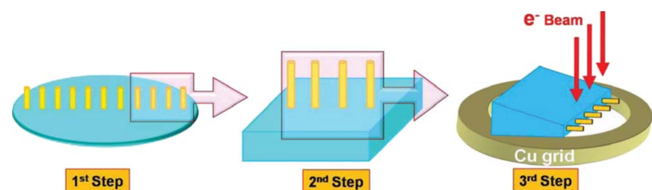

FIG. 2. (Color online) Overall process flow used combing dicing saw with tripod polishing. The first step shows the initial oxidized nanowires atop the substrate. The second step shows the dicing saw cutting and making a small reticular piece of substrate containing the nanowires on top. The last step shows the method of tripod polishing to remove shadowing.

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TABLE I. Process parameters used for this study showing the gas mixture, pressure, ICP power, rf power, stage temperature, and etching rate of materials.

Processing gas (sccm)	ICP power (W)	rf power (W)	Pressure (mTorr)	Stage temp. (°C)	Etching rate (nm/min)
$SF_6:C_4F_8=20:30$	500	20	30/10	20	~220

a diamond blade having a 3 mil wide curf and 408 μm grit sizes running at a 30 krpm spin speed. By performing two successive passes, a slice of only about 100 μm wide can be realized, and with proper control, the pillars are contained within this slice. The last step shows the tripod polishing method consisting of three verniers and a Pyrex rod to which the sample is affixed with an adhesive. Tripod polishing is able to thin the sample substrate at an oblique angle creating a wedge-shaped TEM specimen incorporated with a grinding wheel and successively finer grits.[15] Thinning the region of interest is a critical step which prevents electron-beam shadowing effects, allowing the nanopillars to be inspected clearly.

TEM was used to further inspect the internal structure of the nanowire, which revealed a crystalline Si core (dark) surrounded by amorphous SiO_2 (bright), and those results are presented here. High-angle annular dark field (HAADF) imaging, also known as the *Z*-contrast imaging technique, which depends on the atomic nucleus of different atomic numbers creating different scattering angle of the scattered incident electrons from the electron gun, was also used to characterize and analyze the nanowire composition.

III. RESULTS AND DISCUSSION

A top-down approach is the most advantageous for providing adequate placement and registry of nanostructures suitable for electronics applications, unlike many optoelectronics' applications, such as quantum dot lasers, where self-assembled quantum dots housed anywhere within the optical cavity can suffice.[11,16] Each electrical switching node must be precisely placed to enable device interconnect wiring. But, top-down approaches often have a challenge to create low-dimensional structures equivalent to bottom-up approaches due to the limitations of processing equipment and techniques. Highly anisotropic structures and localized semiconductor alloy composition variations in the wafer's x and y dimensions that differ from other adjacent regions formed during the initially epitaxy step are extremely challenging to realize. This article provides a few avenues that have not been combined before and that may guide future investigations, plasma etching, self-limiting oxidation, and potentially Ge-pileup.

To achieve anisotropic profiles with high aspect ratios for nanoscale wires and pillars, dry etching is the preferred technique that can precisely control etching depth and profile with various controllable parameters, such as incident ion energy and selection of gas, pressure, compared to traditional wet etching governed by isotropic etching. However, there are very complicated interactions between these parameters making process development quite challenging to realize a vertical etch profile suitable for a nanowire. In this study, an Oxford Plasmalab System 100 provided ICP-RIE processing, which combines remote high density plasma with low incident ion energy and therefore reduced surface damage.[17]

One way to create highly anisotropic profiles is by including a passivation gas, which covers the entire sample surface with nonreactive polymers, particularly recently etched (and exposed) sidewalls. However, the kinetics of the etch gas's ion energy can effectively remove the polymer film created on the planer surface through the large kinetic energy normal to the surface plane, while the deposited polymer on the vertical sidewalls effectively protects and prevents further etching from the incident ion bombardment due to the tangential angles.[18] Therefore, the selected gases in this study for etching and passivation in order to synthesize anisotropic profiles are the combined sulfur hexafluoride and octafluorocyclobutane process gasses (SF_6/C_4F_8), which together create very smooth sidewall surfaces unlike the Bosch process that makes undesirable rough sidewalls due to a cyclic etch/passivate process.[18,19] Table I shows the final parameters that were used in this study, including rf powers selected. To first order, the processing pressure mainly controls the etched sidewall profile by altering the ion mean free path length, while the ICP and rf powers determine the etching rate of the material that must be etched away. ICP power is the power delivered to create the remote high-density plasma, and the rf power controls the amount this remote plasma couples to the sample surface and thus permits almost direct control of incident ion energy, unlike standard RIE. Therefore, ICP-RIE improves the control and ion directionality for greater anisotropy etching profiles.

The pressure inside the ICP-RIE chamber is another important factor in order to control the sidewall profile precisely. The great advantage of the ICP-RIE technique is that the plasma can be maintained even at low pressures and low substrate bias voltages that effectively reduce ion collision damage. In fact, the pressure is so low that a pressure of 30 mTorr is required just to ignite the plasma. The preferred processing pressure in this study is maintained around 10 mTorr, which reduces the ion mean free path to create the desired etching rate and profile. Scanning electron microscopy (SEM) imaging of the nanowires using higher processing pressures revealed reduced anisotropy resulting in smaller diameter wires that were often not free standing and likely to topple over. The nanowire profiles become more anisotropic as the chamber pressure is reduced, as confirmed by the SEM inspection. At a chamber pressure of 10 mTorr, the mean free path is now long enough to significantly re-

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duce lateral etching and thus obtain nearly vertical etching profiles. To minimize isotropic etching, the chamber pressure is reduced from 30 mTorr immediately to the desired 10 mTorr pressure following plasma ignition. For the selected process flow rates and rf powers chosen, a 10 mTorr pressure provided the most vertical sidewall profiles.

The preferred ratio here was $SF_6:C_4F_8$ (20:30 SCCM) for the structures shown here. This ratio provides a preferred balance between the SF_6 etching and the C_4F_8 passivation. Since the reaction of the C_4F_8 plasma forms the carbon-based passivating polymer layer while the SF_6 plasma etches Si-based materials, a high C_4F_8 gas flow rate will reduce the chance that SF_6 will react chemically with the Si sidewall thereby enabling a highly, anisotropic profile to be both thin and tall, suitable for vertical nanowires. Therefore, a higher quantity of the C_4F_8 process gas is preferred.

Samples were attached to a 4 in. Si carrier wafer using high temperature vacuum grease (Apiezon H), which fosters better thermal contact between the sample and Si carrier wafer helping heat dissipate evenly while providing enhanced heat sinking, permitting higher etch rates without thermal damage or risk to the passivation polymer. To further control the undercut, a closed-loop liquid cooling system kept the stage temperature nominally at 20 °C under the carrier wafer.

Figure 3 shows SEM images of wires etched in the $SF_6:C_4F_8$ chemistry at a pressure of 10 mTorr. These images clearly demonstrate no sloping and a vertical profile of wires including NiCr etch mask on top, which was later removed prior to the oxidation process in the high temperature furnace. Undercutting of the metal mask and its translation into nanowires provided for greater lateral dimensional control than originally defined lithographically. However, structures shown in Fig. 3 remain difficult to analyze by TEM inspection in terms of their modest height relative to the substrate thickness, which significantly shadows the diffracted electron beam, especially for subsequent large angle collection for HAADF analysis. Focused ion beam (FIB) technologies to locally extract the nanowires have led to damage to the fragile nanostructures, and efforts to protect the region of interest using resist with another lithographic step is nonoptimal due to the extra processing overhead involved. Other hybrid techniques were developed here instead, which will be revealed later, to properly characterize the nanowires without harvesting from the substrate in batch mode common to carbon nanotubes. The nanowires shown in Fig. 3(b) were etched even further to a taller height with the same parameters of the earlier process. These SEM images reveal that they are very tall and thin enough to be electron transparent for TEM inspection, as the undercutting of the mask provides for even narrower diameter nanowires with the deeper etch depth. Figure 3(c) reveals an even deeper etch, by increasing the etch time in 2 min, resulting in nanopillars 25 nm wide and over 550 nm tall.

The effective diameter of the wires is further reduced during a thermal oxidation process utilizing the self-limiting technique,[14] and the final structures house a crystalline Si inner wire core covered by an amorphous SiO_2 layer. The self-limiting technique occurs when a three-dimensional structure is oxidized and two separate oxidation fronts approach each other. The tremendous strain energy involved as the two advancing Si/SiO_2 interfaces influences the oxidation rate as the two fronts come in close proximity. Eventually, the two strain fields effectively repel each other and prevent further oxidation, as long as the oxidation temperature is not high enough to permit plastic flow of the SiO_2, thereby releasing the strain energy triggering the self-limiting oxidation. Using a constant furnace temperature and a fixed oxidation time, the limitations of directly patterned feature sizes with EBL systems and dry etching enable extremely narrow dimensional wires with high yields and uniformity concurrently with precise placement.[14,20]

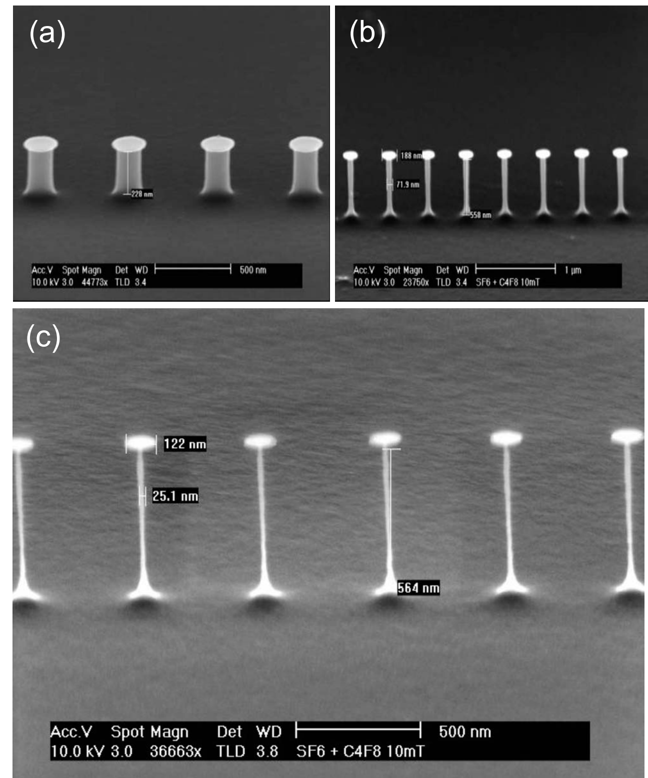

FIG. 3. SEM images of nanowires following ICP-RIE etching in a $SF_6:C_4F_8$ (20:30 SCCM) mixture at a pressure of 10 mTorr. These images clearly demonstrate no sloping and a nearly vertical profile of wires including the NiCr metal etch mask on top, although erosion below the NiCr mask has narrowed the nanopillars beyond that defined lithographically. (c) shows the highest aspect ratio that reveals pillars ~25 nm in diameter and more than 550 nm tall.

Figure 4 shows the top view SEM images of nanowires after the thermal oxidation process is performed in a quartz tube furnace at 1100 °C in dry O_2 ambient for 1 h. Note that some charging on the silicon dioxide surface has caused some of the diameter dimensions to be misrepresented and care must be given to its interpretation from the top view.

TEM analysis provides structure information of this wire directly. However, TEM preparation must be suitable for electron transparency in order to form images, and the dimensions realized here are suitable as is. However, a dicing

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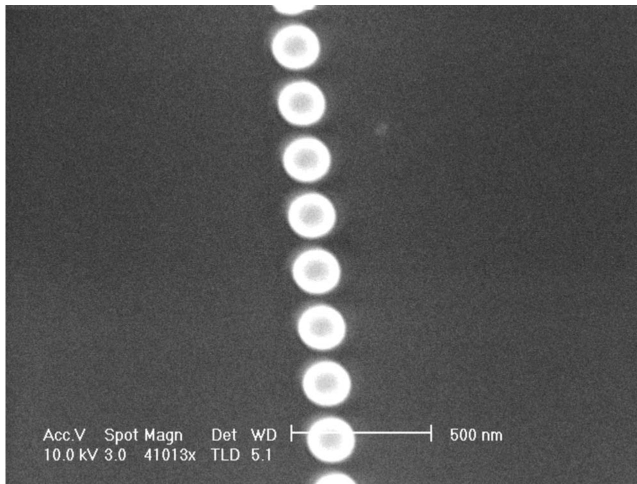

FIG. 4. Top view SEM images of nanowires after the thermal oxidation process is performed in a quartz tube furnace at 1100 °C in dry O_2 ambient for 1 h. Electrical charging of the SiO_2 exterior by the incident electron beam falsely represents the swelling of the nanowire diameter.

saw following tripod polish method is used instead of FIB,[21] which uses high energetic ions generating surface heating and sputtered material redeposition that severely damaged the fragile wires in earlier attempts. Usage of strategically placed resist atop only the region of interest also proved problematic, as the extra electron-beam lithography costs and labor were prohibitive.

In Fig. 5, several TEM images of a selected silicon nanowire are shown that was obtained with a Tecnai F20 field emission TEM at 200 kV with an X-twin lens. According to TEM analysis, the diameter of the inner Si core surrounded by the SiO_2 layer is slightly smaller than 40 nm, which is much smaller in diameter than the wires prior to oxidation and immediately following plasma etching. For the image shown here, the initial NiCr etch mask was nominally 190 nm in diameter, and after plasma etching this diameter reduced to about 70 nm. The oxidation process caused the nanopillars to swell to 110 nm (outside diameter), with 70 nm of this attributed to the oxide and the inner core now effectively only 40 nm in diameter. Also, the height of the nanowires was determined to be about ~600 nm based on the TEM micrographs. Thus, this combined ICP-RIE etching and self-limiting oxidation technique reduced the observed nanostructures from nominally 190 nm in diameter to 40 nm, using this TEM example. Due to the self-limiting oxidation, this provides a robust process to generate high aspect nanostructures below the lithographic dimensions.

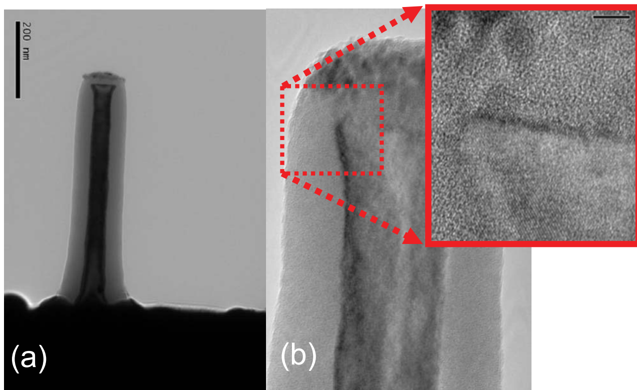

FIG. 5. (Color online) Here, cross sectional TEM analysis reveals the diameter of the inner Si core surrounded by SiO_2 layer has now reduced to about 40 nm. Also, the nanowire height is about 600 nm from the image. The TEM photomicrograph of the nanowire indicates a crystalline core and an amorphous cladding.

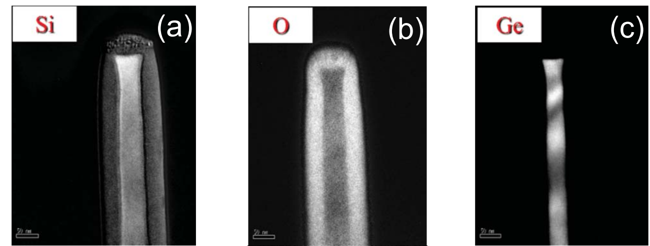

FIG. 6. (Color online) HAADF analysis of the Si nanowire shows the elemental analysis. The Si signal is fairly uniform, indicating a reasonable uniformity throughout the Si core and SiO_2 cladding and the right image shows the oxygen concentrated at the SiO_2 periphery. (c) shows the HAADF analysis of the nanopillar detecting Ge species.

TEM images of the nanowire indicate a crystalline core and amorphous oxide cladding. It is evident here that some residual NiCr used as a plasma etching mask is still present atop the nanowire, since plasma dry etching process always creates heat on samples during etching which is done by energetic ion bombardment on the surface according to reference.[22,23] We believe that heat during the etching process makes NiCr diffusion on Si substrate. Plus there is additional heating due to chemical effects during the etching reaction with various processing gases such as SF_6 and C_4F_8. That is why some residual NiCr on top of nanowire is revealed. However, NiCr residual remaining on SiO_2 layers, which covers Si nanowire, will be removed easily by HF dipping. Therefore, this is no problem at all in terms of device performance. Further reduction in the nanowire diameter is expected with different tailoring of the patterning, etching, and oxidation processes.

The high-angle annular dark field (HAADF) analysis of the Si nanowire reveals on the left of Fig. 6 that the Si signal is fairly uniform, indicating a reasonable uniformity throughout the Si core and SiO_2 cladding, and the middle image shows the oxygen concentrated at the SiO_2 periphery. It should be noted that since the structure is actually a cylinder, the HAADF oxygen signal is not zero at the center, since HAADF will indicate a cumulative signal for the front and back of the nanowire as well.

It is very interesting to note that the thin 1 nm Ge containing layers, 1% of Ge atoms in $Si_{1-x}Ge_x$, used as markers now are fully diffused into all surrounding regions of the Si nanowire, see Fig. 6(c), following the thermal oxidation process to reduce the nanowire diameter size further.[24,25] The high oxidation temperature of 1100 °C used for this specimen and for a 1 h duration is perceived as low enough to provide self-limiting oxidation[26] whereby the two strain

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fields that collide in the three-dimensional nanowire structure and repel each other. This occurs below the temperature for appreciable SiO_2 plastic flow to relieve the strain energy created at the Si/SiO_2 interface. However, this temperature is clearly too high a temperature to concurrently permit measurable Ge-pileup from the oxidation of a $Si_{1-x}Ge_x$,[27] where an oxidized Ge atom is consumed in the advancing oxidation front, and then exchanged with a Si atom, leading to a Si-rich oxide and an underlying unoxidized Ge-rich layer.[28] For Ge-pileup, as this underlying region becomes Ge-rich, the diffusivity of oxygen through the Ge-rich layer is reduced and the advancing oxidation front is halted, even for planar wafers. In these experiments, the furnace temperature was high enough to permit this Si–Ge exchange at the oxide interface, but then subsequently the high diffusivity of Ge in Si at that temperature permitted it to also be uniformly distributed throughout the unoxidized nanowire.[29] This could, however, be a future basis to synthesize three-dimensional Si/SiGe structures orthogonal to the epitaxial growth plane.

IV. CONCLUSION

Si-based nanowires with high aspect ratios and a high degree of registry have been fabricated with using an ICP-RIE process with a $SF_6:C_4F_8$ gas mixture using a top-down approach. An additional thermal oxidation step was performed to further reduce the nanowire dimensionality. TEM analysis illustrates that the inner Si-wire core is roughly 600 nm tall and 40 nm wide in diameter with a high aspect ratio for a top down nanostructure. These are excellent candidates for nanoscale computing where placement of low-dimensional structures is the key for successful interconnect wiring.

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[1] M. H. Huang, S. Mao, H. Feick, H. Yan, Y. Wu, H. Kind, E. Weber, R. Russo, and P. Yang, Science **292**, 1897 (2001).
[2] Y. Cui, Q. Q. Wei, H. K. Park, and C. M. Lieber, Science **293**, 1289 (2001).
[3] M. S. Gudiksen, L. J. Lauhon, J. Wang, D. C. Smith, and C. M. Lieber, Nature (London) **415**, 617 (2002).
[4] L. Vayssieres, Adv. Mater. **15**, 464 (2003).
[5] M. T. Björk, O. Hayden, H. Schmid, H. Riel, and W. Riess, Appl. Phys. Lett. **90**, 142110 (2007).
[6] L. P. Kouwenhoven, T. H. Oosterkamp, S. Tarucha, D. G. Austing, and T. Honda, Physica B **249–251**, 191 (1998).
[7] W. Wang, C. J. Summers, and Z. L. Wang, Nano Lett. **4**, 423 (2004).
[8] Krishna K. Bhuwalka, Jorg Schulze, and Ignaz Eisele, IEEE Trans. Electron Devices **52**, 909 (2005).
[9] J. E. Allen *et al.*, Nat. Nanotechnol. **3**, 168 (2008).
[10] S. H. Oh *et al.*, Nano Lett. **8**, 1016 (2008).
[11] P. R. Berger, K. Chang, P. Bhattacharya, J. Singh, and K. K. Bajaj, Appl. Phys. Lett. **53**, 684 (1988).
[12] F. Laermer and A. Schip, U.S. Patent No. 5,501,893.
[13] H. Rhee, H. Kwon, C.-K. Kim, H. Kim, J. Yoo, and Y. W. Kim, J. Vac. Sci. Technol. B **26**, 576 (2008).
[14] H. I. Liu, D. K. Biegelsem, N. M. Johnson, and R. F. W. Pease, J. Vac. Sci. Technol. B **11**, 2532 (1993).
[15] N. Kato, H. Maruyama, and H. Saka, J. Electron Microsc. **50**, 9 (2001).
[16] K. Kamath, P. Bhattacharya, T. Sosnowski, T. Norris, and J. Phillips, Electron. Lett. **32**, 1374 (1996).
[17] S.-Y. Park, S.-Y. Chung, R. Yu, P. R. Berger, and P. E. Thompson, Electron. Lett. **42**, 719 (2006).
[18] X. Li, X. Cao, H. Zhou, C. D. W. Wilkinson, S. Thoms, D. Macintyre, M. Holland, and I. G. Thayne, Microelectron. Eng. **83**, 1152 (2006).
[19] W. J. Park, J. H. Kim, S. M. Cho, S. G. Yoon, S. J. Suh, and D. H. Yoon, Surf. Coat. Technol. **171**, 290 (2002).
[20] H. Fukuda, J. L. Hoyt, M. A. McCord, and R. F. W. Pease, Appl. Phys. Lett. **70**, 333 (1997).
[21] N. I. Kato, J. Electron Microsc. **53**, 451 (2004).
[22] A. Durandet, O. Joubert, J. Pelietier, and M. Pichot, J. Appl. Phys. **67**, 3862 (1990).
[23] R. Dussart, A. L. Thomann, L. E. Pichon, L. Bedra, N. Semmar, P. Lefaucheux, J. Mathias, and Y. Tessier, Appl. Phys. Lett. **93**, 131502 (2008).
[24] Y. Bogumilowicz *et al.*, ECS Trans. **3**, 1099 (2006).
[25] N. E. B. Cowern, P. C. Zalm, P. van der Sluis, D. J. Gravesteijn, and W. B de Boer, Phys. Rev. Lett., **72**, 2585 (1994).
[26] A. N. Stepanova, V. I. Muratova, L. N. Obolenskaya, O. M. Zhigalina, N. A. Kiselev, and E. I. Givargizov, J. Phys.: Conf. Ser. **61**, 352 (2007).
[27] M. Hasanuzzaman and Y. M. Haddara, J. Mater. Sci. **19**, 569 (2008).
[28] P. E. Hellberg, S. L. Zhang, F. M. d'Heurle, and C. S. Petersson, J. Appl. Phys. **82**, 5773 (1997).
[29] G. F. A. van de Walle, L. J. van IJzendoorn, A. A. van Gorkum, R. A. van den Heuvel, and A. M. L. Theunissen, Semicond. Sci. Technol. **5**, 345 (1990).

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