# Extending CMOS: Quantum Functional Circuits Using Si-Based Resonant Interband Tunnel Diodes

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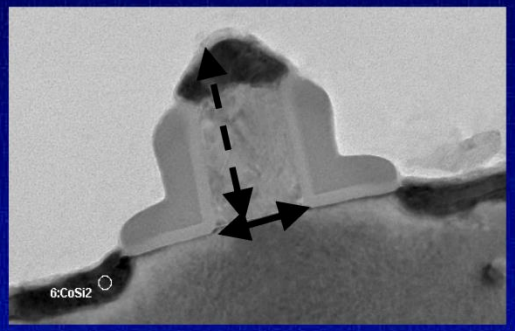
# Present Day CMOS Challenges

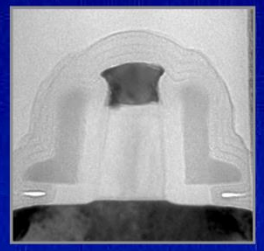
# Accelerated Scaling of Planar Transistors

130nm Node



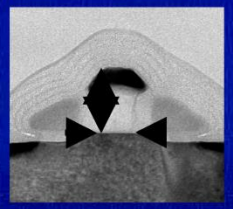

70nm Length
(Production2001)

90nm Node



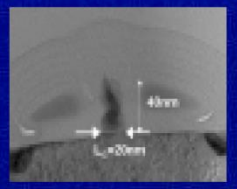
50nm Length
(Production in 2003)

65nm Node

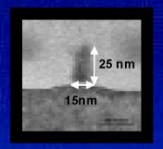


30nm Prototype
(Production in 2005)

45nm Node



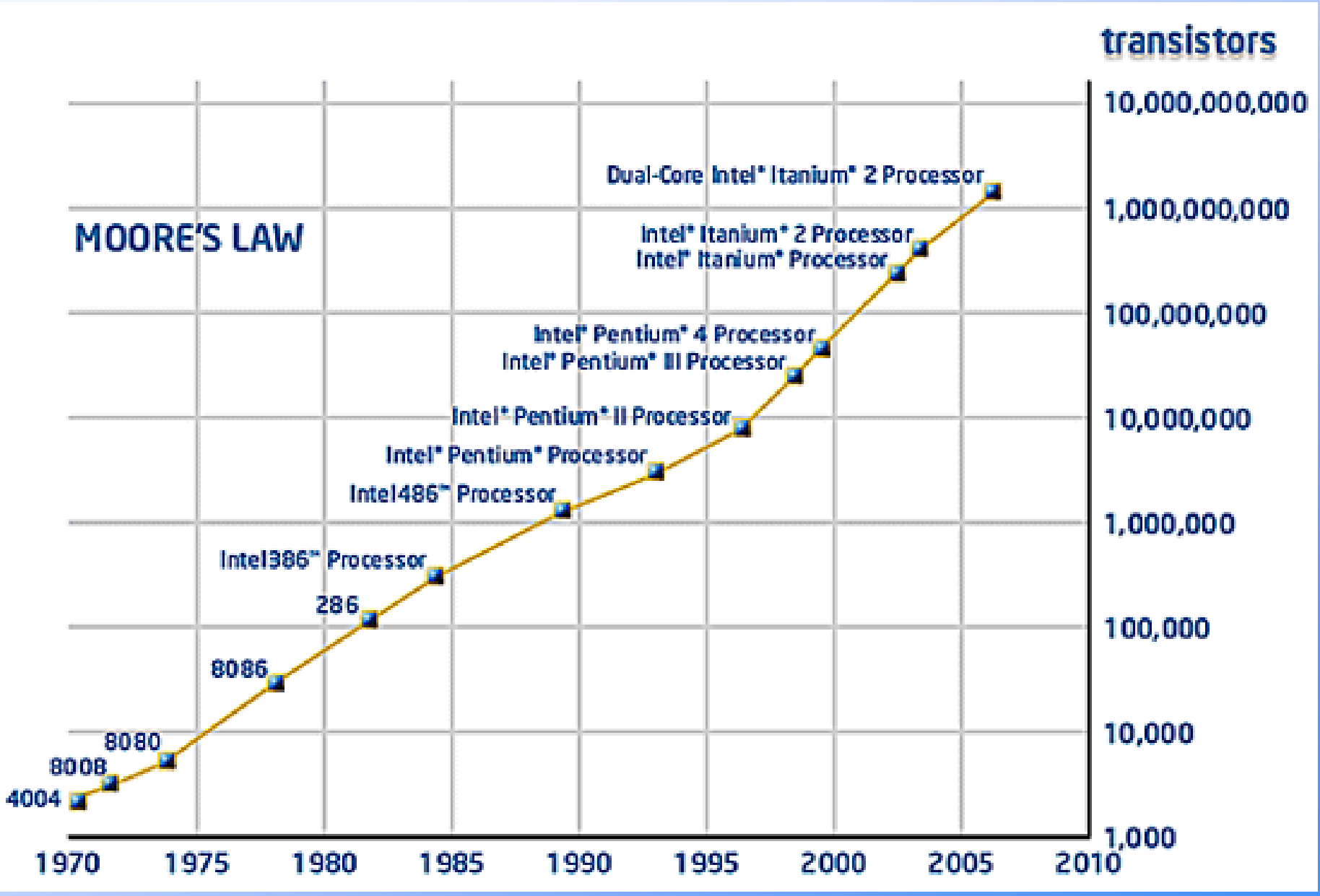

32nm Node




20nm Prototype
(Production in 2007)

15nm Prototype
(Production in 2009)

Intel


transistors
MOORE'S LAW
Dual-Core Intel® Itanium® 2 Processor
Intel® Itanium® 2 Processor
Intel® Itanium® Processor
Intel® Pentium® 4 Processor
Intel® Pentium® III Processor
Intel® Pentium® II Processor
Intel® Pentium® Processor
Intel486™ Processor
Intel386™ Processor
286
8086
8080
8008
4004
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100,000,000
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1970
1975
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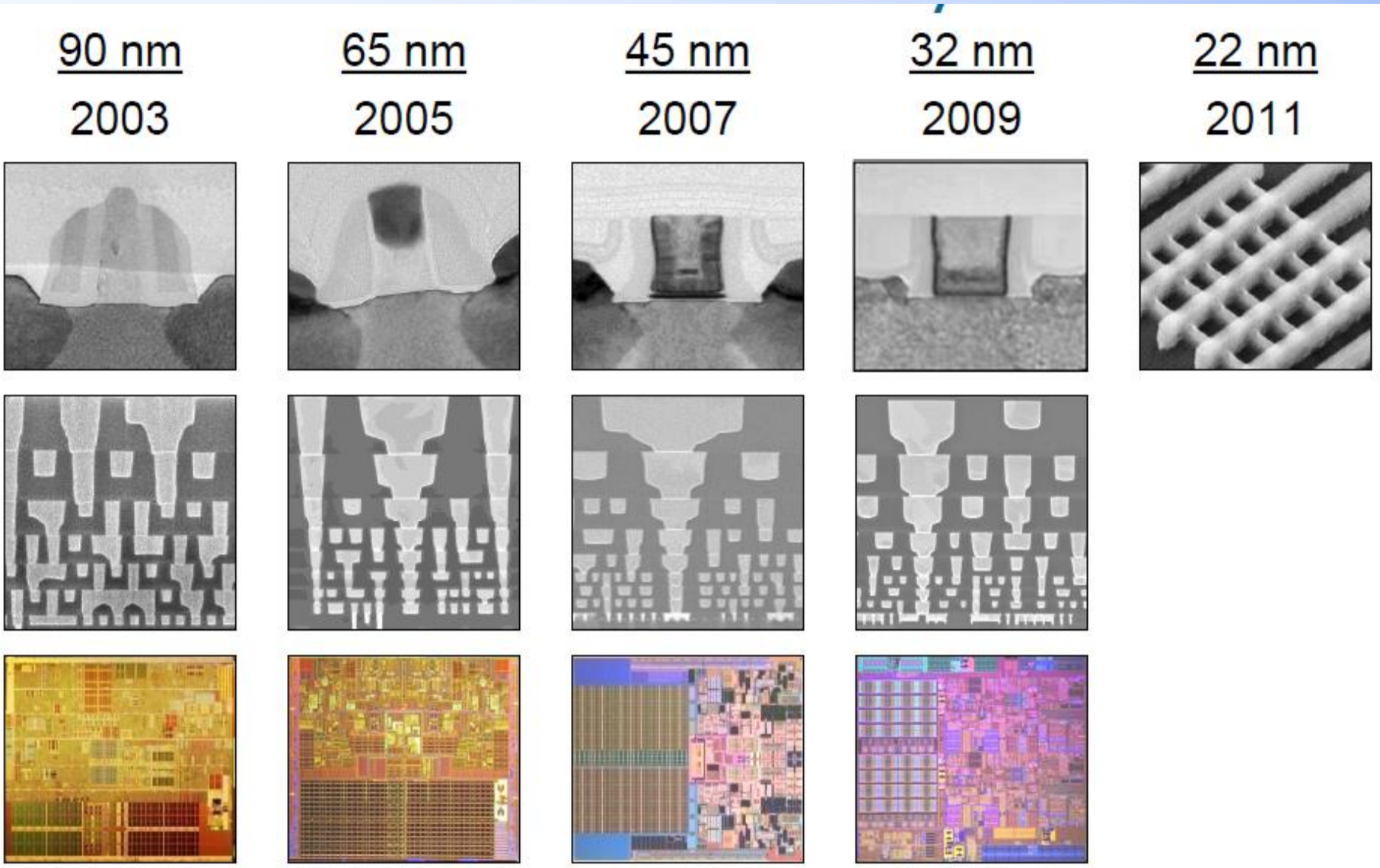
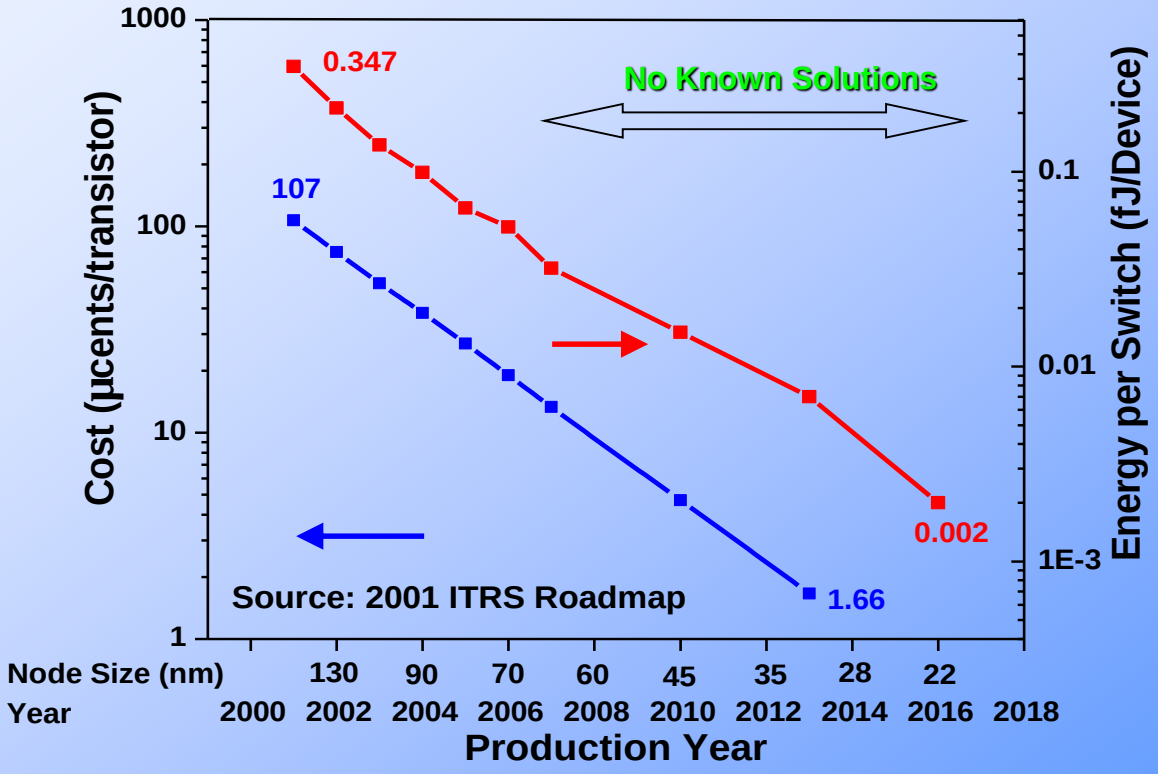
1995
2000
2005
2010

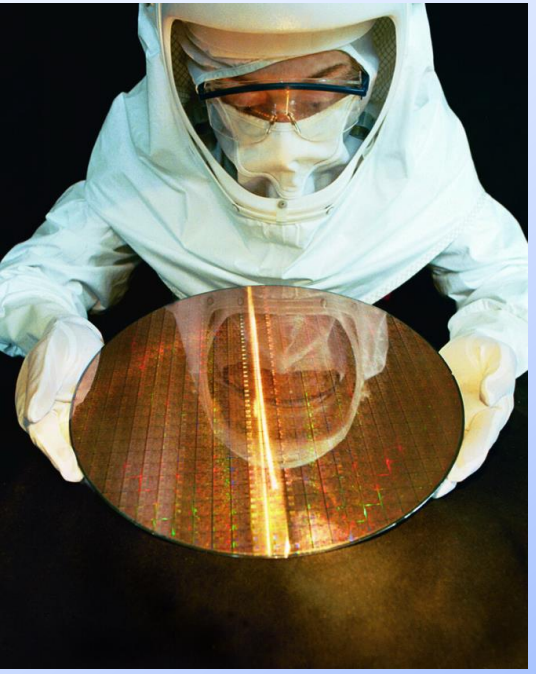
# Moore's law



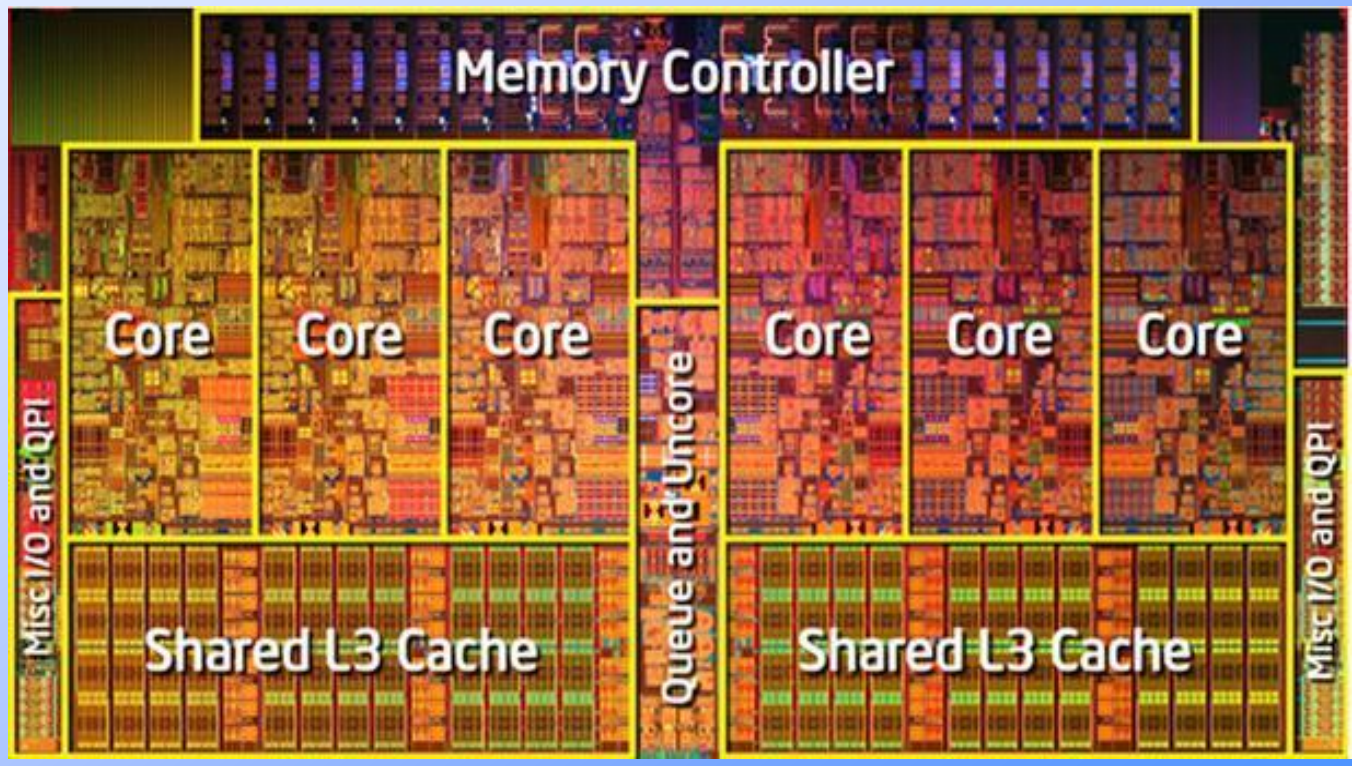
# Motivation: Extending CMOS?




- CMOS cannot be scaled indefinitely.
- Solutions: either replace or augment scaled CMOS
- Tunnel diodes married with CMOS offer enhancements

**6T SRAM cache memory dominates footprint and power consumption, operates about 1 volt**
**(→ 8T SRAM)**

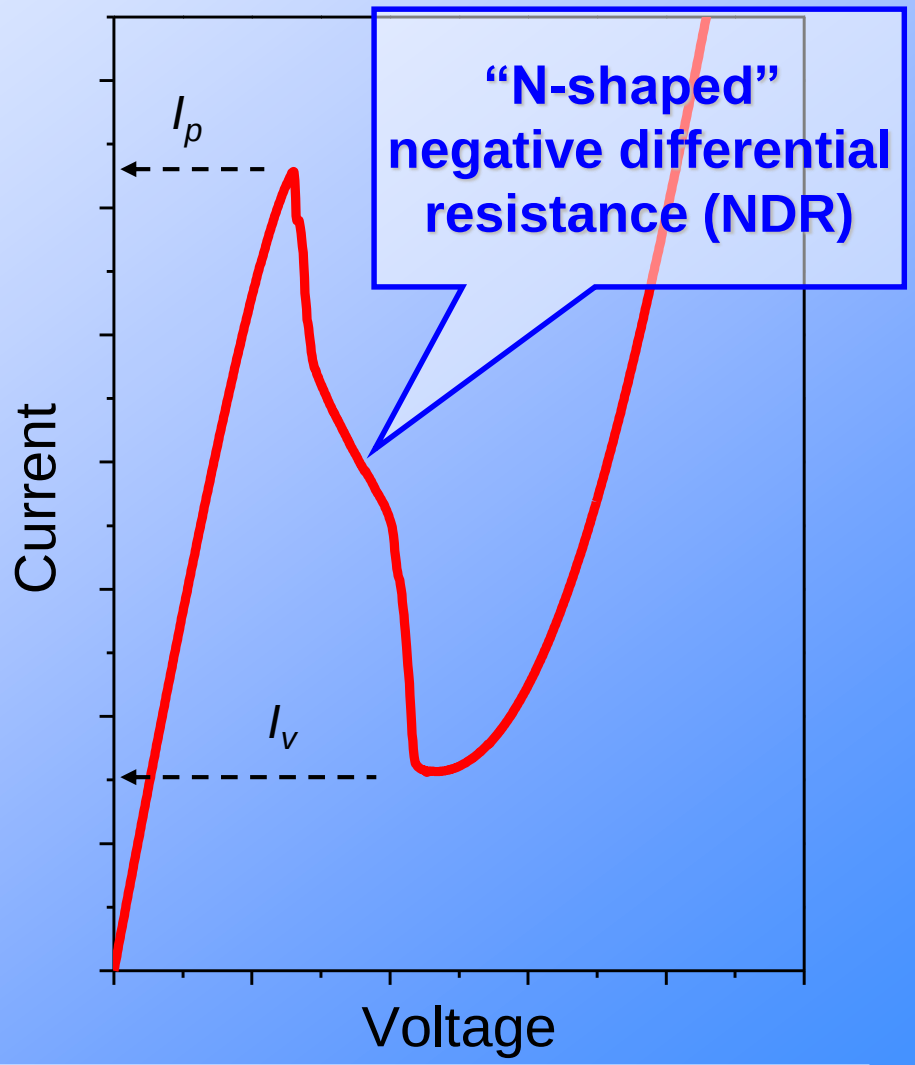



**Power consumption related to voltage squared**
**(~1 volt state-of-the-art)**

# Let's Enter the Quantum World

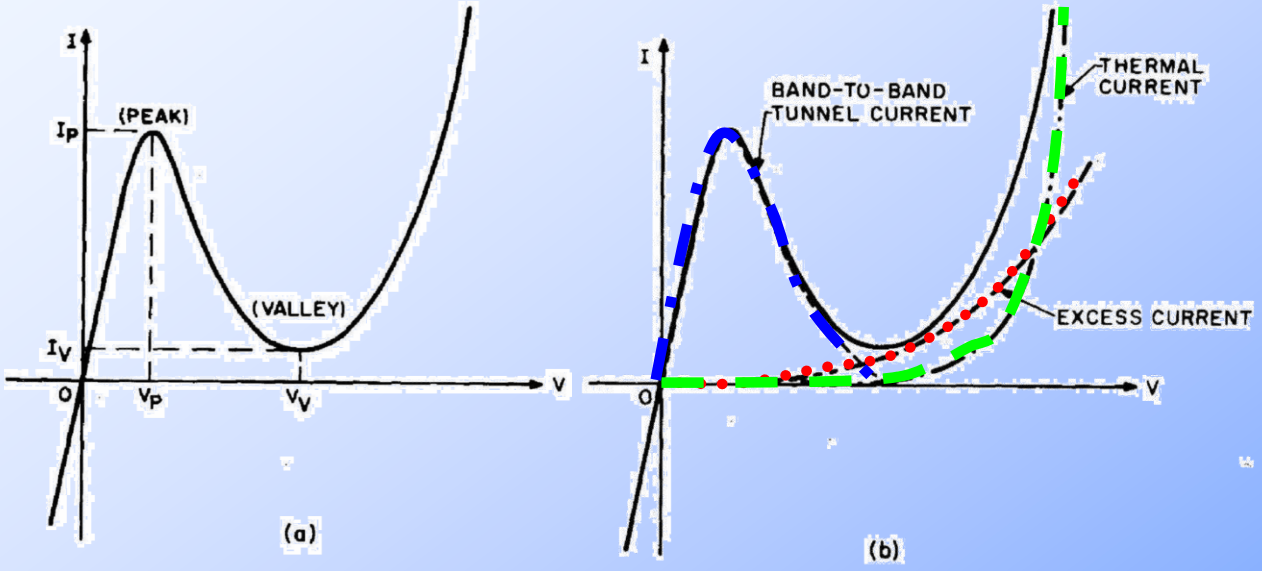
# Introduction to Advantages of Tunnel Diodes

- How to characterize tunnel diode?
  - **Peak-to-valley current ratio**
    $PVCR = I_p / I_v$
  - **Peak current density**
    $J_p = I_p / Area$
  - Speed index
    $s = J_p / C_j$
- Why use TD with transistors?
  - Increases circuit speed
  - Reduces circuit complexity
  - Lowers circuit power
  - Simple integration with transistor



# Three Interband TD Current Components

**From Sze, Physics of Semiconductor Devices, pg. 517 (1981).**

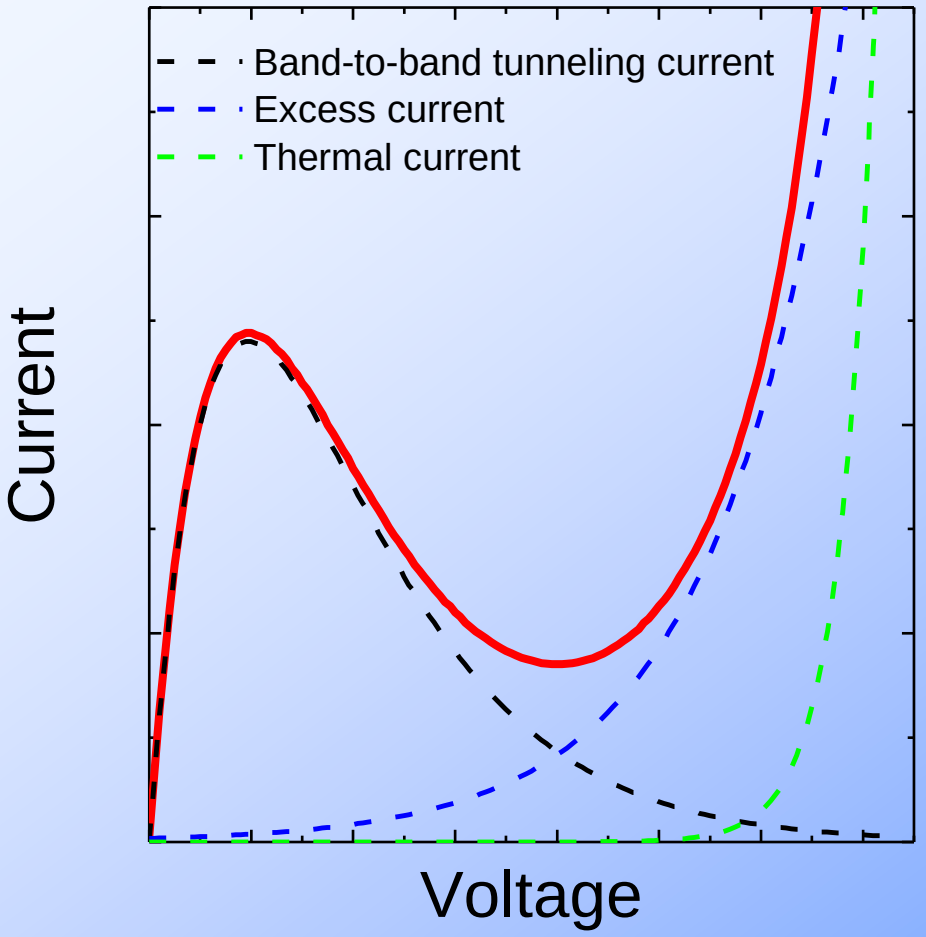



- Desired: optimize structure for efficient quantum mechanical tunneling
- Undesired: excess current comprised partially of defect related tunneling
- Thermal diffusion current eventually takes over at higher biases

## Basic TD Figure-of-Merit

- Peak-to-valley current ratio (PVCR) = $I_p/I_v$
- Peak current density (PCD or $J_p$ )= $I_p/A$, where A is the diode area

# Physics Based Model for RITDs




- Band-to-band tunneling current
  - PVCR, PCD, and speed

$$\exp\left[-\left(\pi \cdot W \cdot m^{*1/2} E_g^{\,3/2}\right)/\left(4\sqrt{2} q\hbar \cdot (V_{bi} - V)\right)\right]$$

- Excess tunneling current
  - PVCR and Standby power dissipation

$$D_x \exp\left[\left(\frac{-\alpha_x \cdot W \cdot e^{0.5}}{2}\right) \times \left(E_g - eV + 0.6 \cdot e \cdot (V_n - V_p\right)\right]$$

- Thermal diffusion current

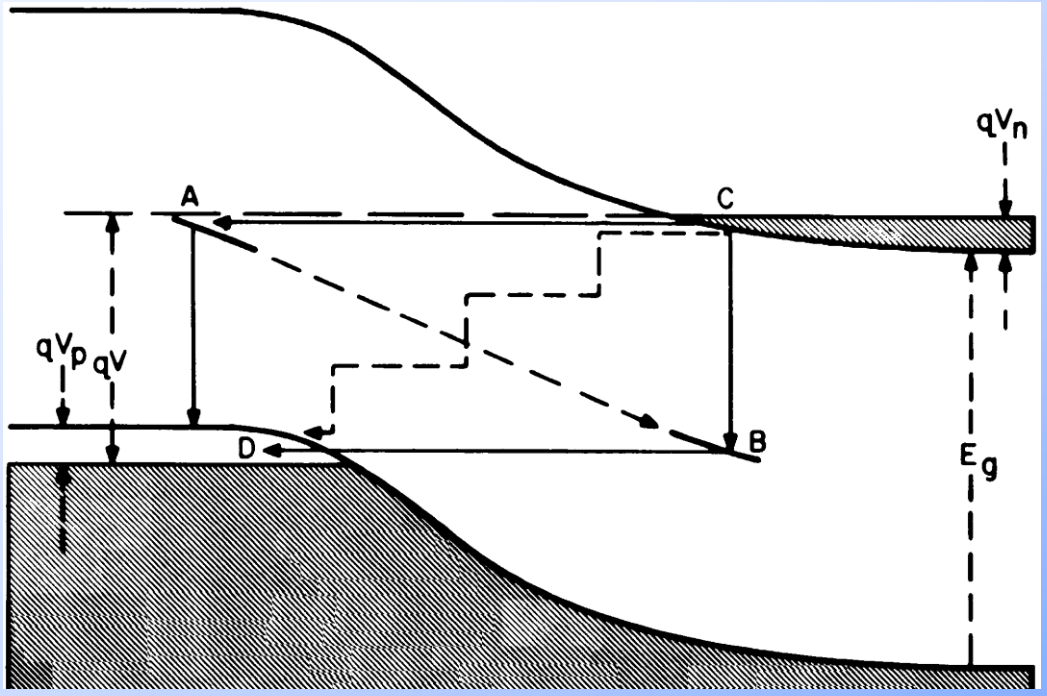
From Sze

$$J_{th} = J_o\left(e^{qV/kT} - 1\right)$$

Goal: Increase **band-to-band current** and minimize **excess current**.

# Excess Current of an Esaki Diode

**Figure adapted from Sze, Physics of Semiconductor Devices, pg. 528 (1981).**



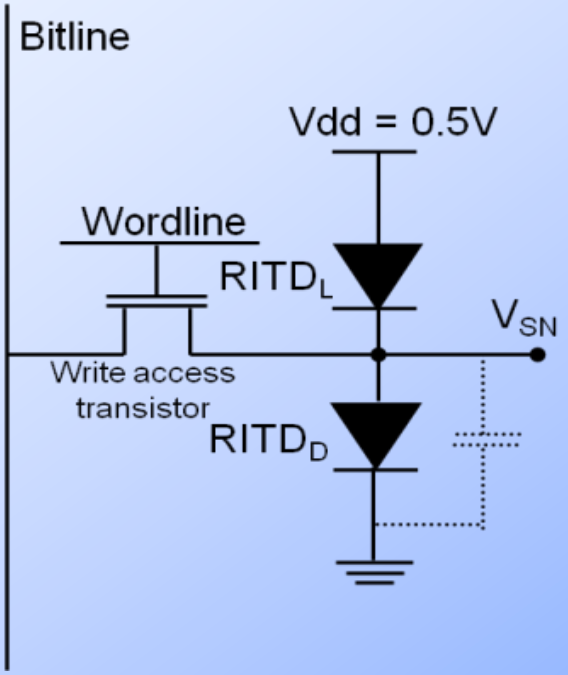

- **Excess current limits PVCR.**
- **Excess current is a tunneling phenomena via defect or midgap states**

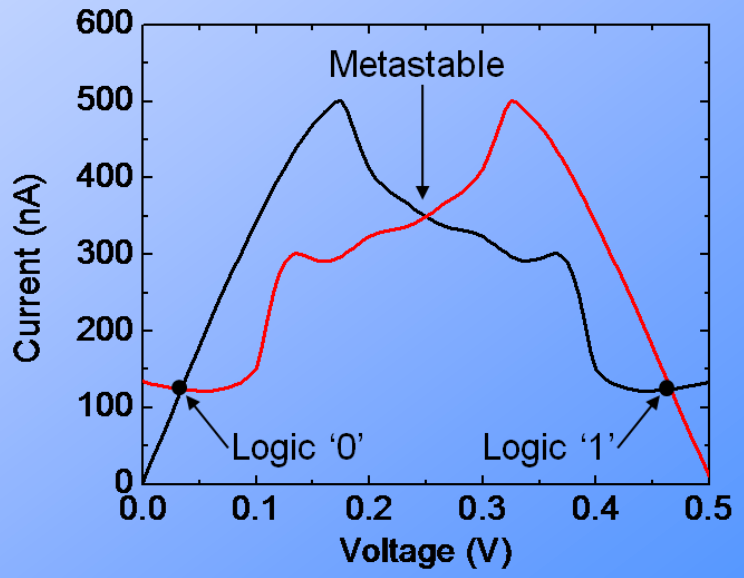
For more info see Chynoweth et al., Phys. Rev., vol. 121, p. 684, (1961).

# The Opportunity

# Opportunity: Tunnel Diode Memory

- One Transistor 2-Tunnel Diode SRAM (1T TSRAM)
- Robust operation at low voltages
- Refresh-free – Low active and standby power Consumption

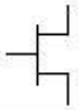
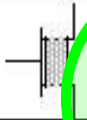
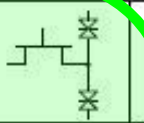
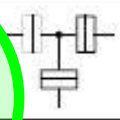
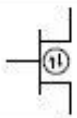




- J. P. A. van der Wagt, A. C. Seabaugh, and E. A. Beam, III, "RTD/HFET low standby power SRAM gain cell," *IEEE Electron Dev. Lett.* **19**, pp. 7-9 (1998).
- J. P. A. van der Wagt, "Tunneling-Based SRAM," *Proc. of IEEE*, 87, pp. 571-595 (1999).

- **Monolithic Integration of Si-based tunnel diodes with Si-based transistors**

| Device | |  |  |  |  |  |  |  |
|---|---|---|---|---|---|---|---|---|
| | | *FET [B]* | *1D structures* | *Resonant Tunneling Devices* | *SET* | *Molecular* | *Ferromagnetic logic* | *Spin transistor* |
| *Types* | | *Si CMOS* | *CNT FET*<br>*NW FET*<br>*NW hetero-structures*<br>*Crossbar nanostructure* | *RTD-FET*<br>*RIT* | *SET* | *Crossbar latch*<br>*Molecular transistor*<br>*Molecular QCA* | *Moving domain wall*<br>*M: QCA* | *Spin transistor* |
| *Supported Architectures* | | *Conventional* | *Conventional and Cross-bar* | *Conventional and CNN* | *CNN* | *Cross-bar and QCA* | *CNN Reconfigure logic and QCA* | *Conventional* |
| *Cell Size (spatial pitch)* | *Projected* | 100 nm | 100 nm [C] | 100 nm [C] | 40 nm [L] | 10 nm [Q] | 140 nm [U] | 100 nm [C] |
| | *Demonstrated* | 590 nm | ~1.5 μm [D] | 3μm [H] | ~700 nm [M] | ~2μm [R] | 250 nm [V, W] | 100 μm [X] |
| *Density (device/cm²)* | *Projected* | 1E10 | 4.5E9 | 4.5E9 | 6E10 | 1E12 | 5E9 | 4.5E9 |
| | *Demonstrated* | 2.8E8 | 4E7 | 1E7 | 2E8 | 2E7 | 1.6E9 | 1E4 |
| *Switch Speed* | *Projected* | 12 THz | 6.3 THz [E] | 16 THz [I] | 10 THz [M] | 1 THz [S] | 1 GHz [U] | 40 GHz [Y] |
| | *Demonstrated* | 1 THz | 200 MHz [F] | 700 GHz [J] | 2 THz [N] | 100 Hz [R] | 30 Hz [V, W] | Not known |
| *Circuit Speed* | *Projected* | 61 GHz | 61 GHz [C] | 61 GHz [C] | 1 GHz [L] | 1 GHz [Q] | 10 MHz [U] | Not known |
| | *Demonstrated* | 5.6 GHz | 220 Hz [G] | 10 GHz [Z] | 1 MHz [F] | 100 Hz [R] | 30 Hz [V] | Not known |
| *Switching Energy, J* | *Projected* | 3E-18 | 3E-18 | >3E-18 | $1\times10^{-18}$ [L] [$>1.5\times10^{-17}$] [O] | 5E-17 [T] | ~1E-17 [V] | 3E-18 |
| | *Demonstrated* | 1E-16 | 1E-11 [G] | 1E-13 [K] | $8\times10^{-17}$ [P] [$>1.3\times10^{-14}$] [O] | 3E-7 [R] | 6E-18 [W] | Not known |
| *Binary Throughput, GBit/ns/cm²* | *Projected* | 238 | 238 [C] | 238 [C] | 10 | 1000 | 5E-2 | Not known |
| | *Demonstrated* | 1.6 | 1E-8 | 0.1 | 2E-4 | 2E-9 | 5E-8 | Not known |
| *Operational Temperature* | | RT | RT | 4.2 – 300 K | 20 K [L] | RT | RT | RT |
| *Materials System* | | Si | CNT, Si, Ge, III-V, $In_2O_3$, ZnO, $TiO_2$, SiC, | III-V Si-Ge | III-V Si | Organic molecules | Ferromagnetic alloys | Si, III-V, complex metals oxides |
| *Research activity [A]* | | | 171 | 88 | 65 | 204 | 25 | 102 |

2005 ITRS – Emerging Research Devices

*Resonant tunneling devices*[51, 52]—Resonant tunneling devices for logic applications include resonant tunnel transistors (RTT) and hybrid devices incorporating resonant tunneling diodes and one or more FETs (RTD-FET). The RTDs are two terminal devices that intrinsically have a very high switching speed and exhibit a region of negative differential resistance in their I-V curves. These two characteristics make them potentially attractive as high speed switching devices. If two RTDs are connected in series, they have two stable operating points and can switch between the two stable points very quickly if a third terminal is added that can act as a gate. However, since the peak current through an RTD depends exponentially on the barrier thickness, it is inherently difficult to get reproducible device operation unless the gate also controls the peak current. Controlling the peak current is usually done by integrating a transistor with the series-connected double RTDs on a common substrate.[53] This approach results in complex, epitaxially grown structures requiring very good control of film thicknesses.

Integration of a transistor with a pair of RTDs introduces delays to the inherently fast bistable switching times associated with capacitive charging and discharging of the transistor gate stack. The operational speed of the integrated device can be an order of magnitude slower than the intrinsic switching speeds of the RTDs themselves. Additional challenges include a limited $I_{ON}/I_{OFF}$ ratio of 10 rather than the factor of $10^5$ that CMOS digital circuit designers require and the inherent complexity of the integrated structure, which limits the dimensional scaling of the devices. The complexity of the hybrid devices makes them large with experimental spatial pitch values of order 5 μm being reported. Another issue is fabrication of silicon or silicon-germanium tunnel diodes with high peak-to-valley ratios.

Adding a control terminal to RTDs extends their usability to a variety of applications. This approach has been used to build resonant tunneling transistors.[54] RTTs have a negative transconductance that can be used in several logic circuits, e.g., in XOR gate with only one transistor.[55]

Traditionally, RTDs have been fabricated in III-V material systems that has limited their widespread applicability. Recently, several papers have described fabrication of group IV devices with Si compatible materials. These include a tri-state logic device fabricated in SiGe[56] and a Si-based field-induced band-to-band tunneling transistor.[57] Although these devices continue to have all the issues outlined above, fabrication in a Si compatible material structure substantially reduces the integration challenges.

Multi-valued logic circuits based on Si resonant tunneling MOS transistors (SRTMOS) were theoretically explored.[58] This theoretical analysis assumed that the SRTMOS has an ON current density of the order of $10^6$ A/cm$^2$ and the $I_{ON}/I_{OFF}$ ratio larger than $10^4$. At this point, no experimental demonstration of resonant tunnel devices with both high current and high $I_{ON}/I_{OFF}$ ratio is known.

A number of recent works explore the spin-polarized resonant tunneling, which could be useful for application in spintronic devices.[59, 60, 61] Another potential niche application for RTDs is in photodetectors for detection of single photons with low dark count rates and high efficiency.[62]

Overall, the resonant tunneling devices may be useful for certain niche applications requiring high speed and low dynamic range and low peak currents provided the manufacturing issues associated with uniformity of the tunneling barrier can be resolved. The principle focus of recent research activity involving RTDs has been in the area of integration on the silicon platform.

# The Payoff: TDs Integrated with Transistors

More computational power per unit area

- ✓ Fewer devices required
- ✓ Faster circuits and systems
- ✓ Reduced power consumption

**Result: Extension of CMOS if a Si-Based TD is available that is compatible with CMOS!**

# Now Let's Apply Quantum Mechanics

**Figure 3–13** Energy band discontinuities for a thin layer of GaAs sandwiched between layers of wider band gap AIGaAs. In this case, the GaAs region is so thin that quantum states are formed in the valence and conduction bands. Electrons in the GaAs conduction band reside on "particle in a potential well" states such as $E_1$ shown here, rather than in the usual conduction band states. Holes in the quantum well occupy similar discrete states, such as $E_h$.

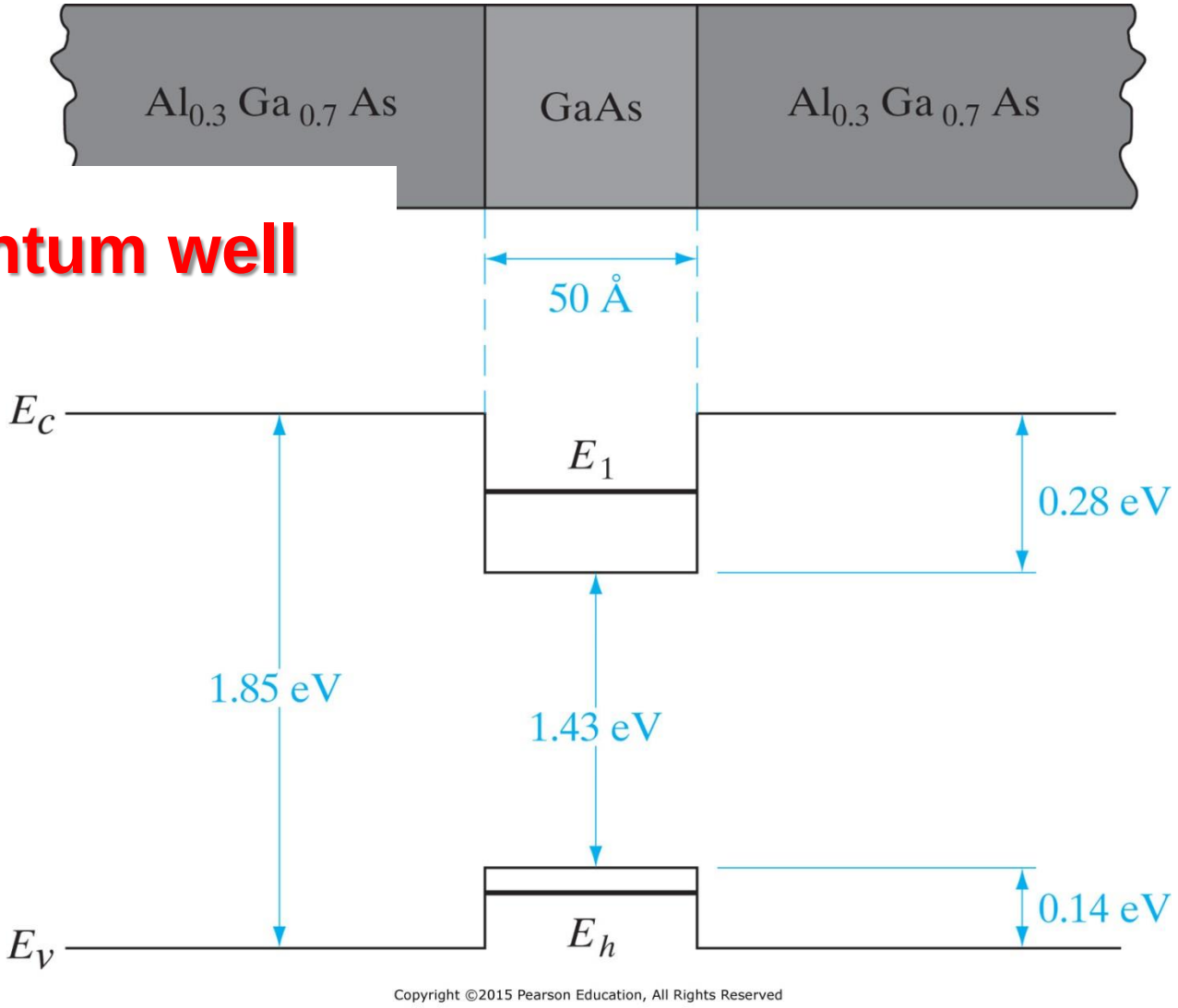
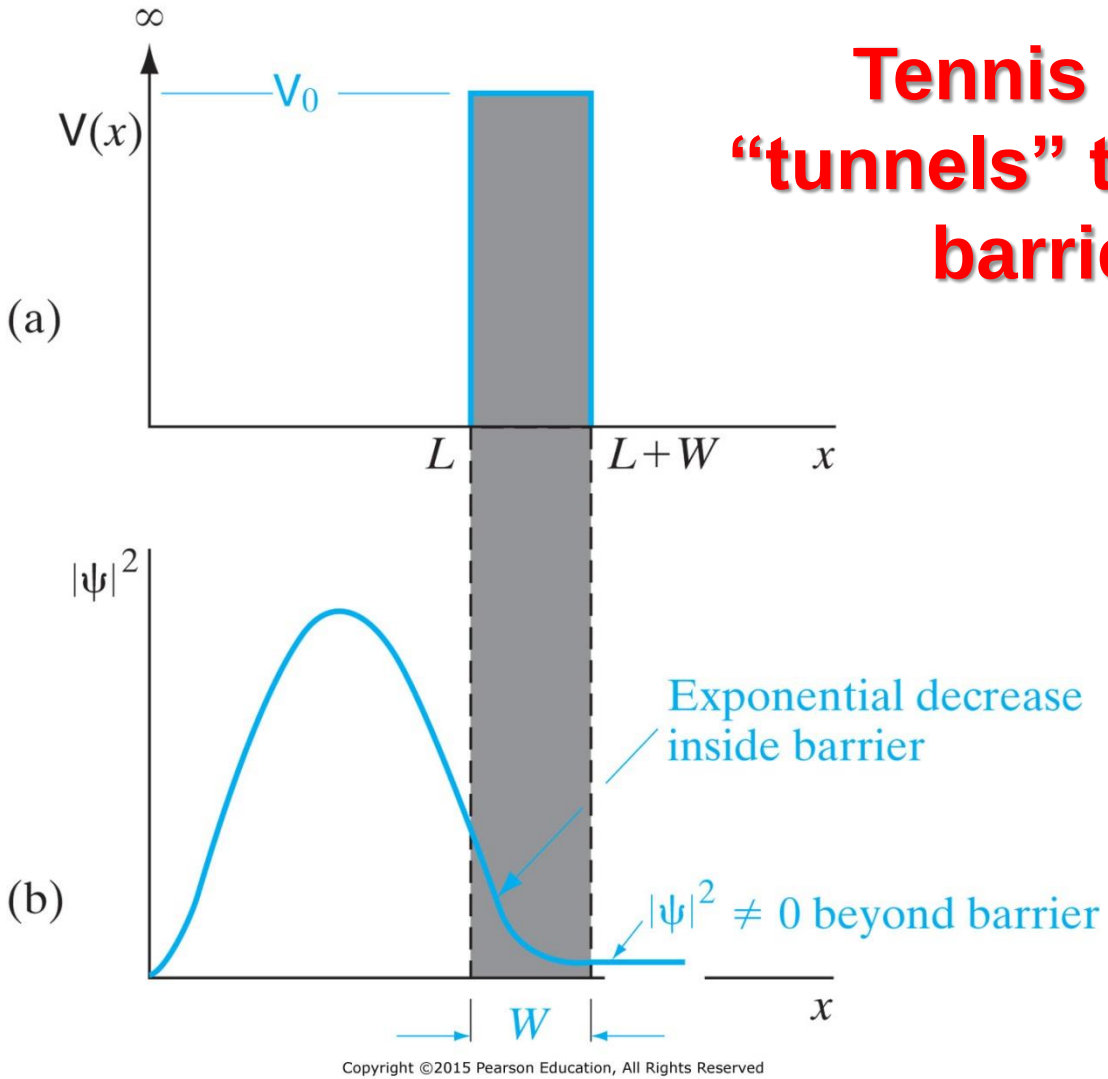
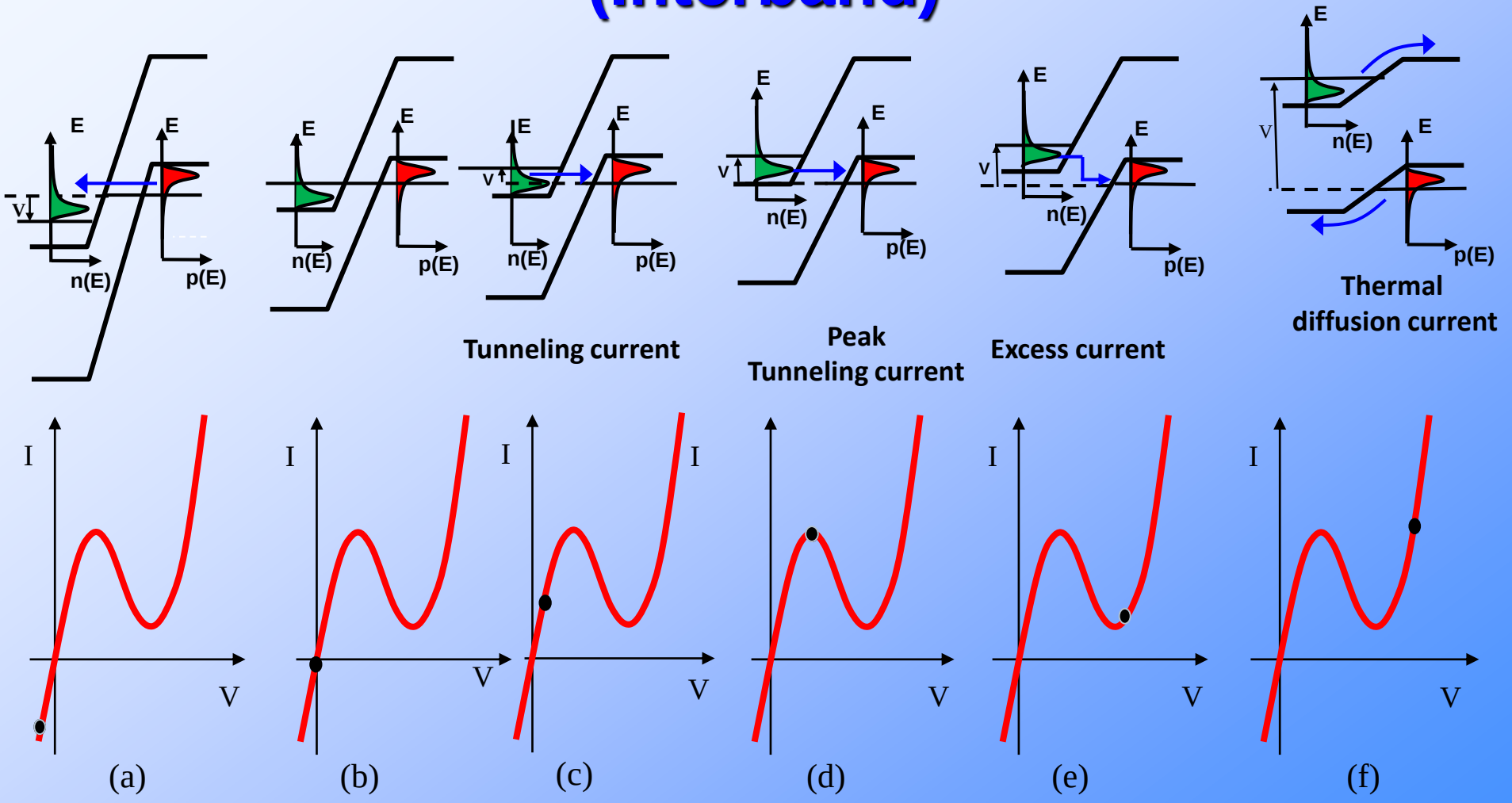


**Figure 2–6** Quantum mechanical tunneling: (a) potential barrier of height $V_0$ and thickness $W$; (b) probability density for an electron with energy $E < V_0$, indicating a nonzero value of the wavefunction beyond the barrier.




**Tennis Ball "tunnels" through barrier**

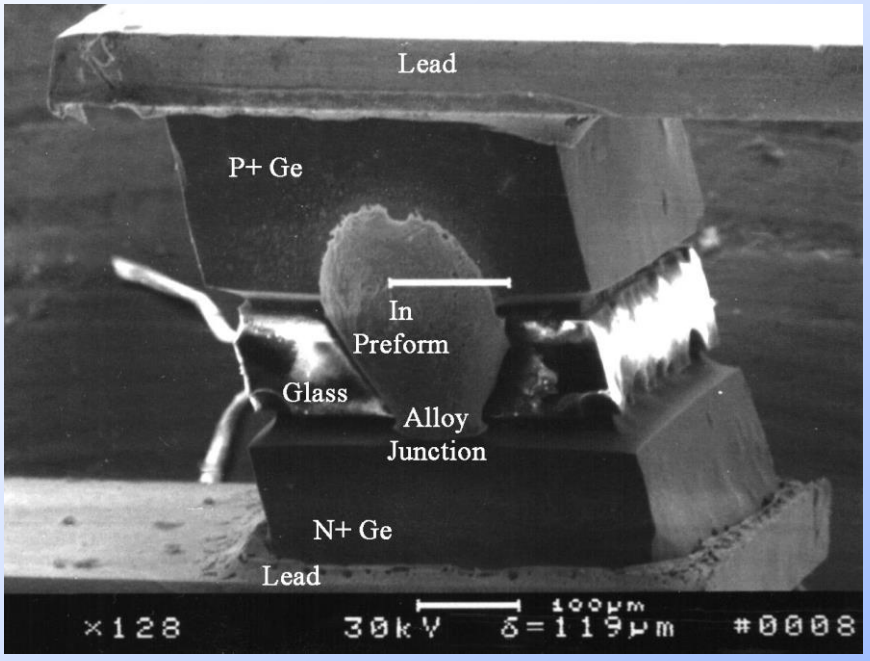
# Basic Physics: Esaki Tunnel Diode (Interband)

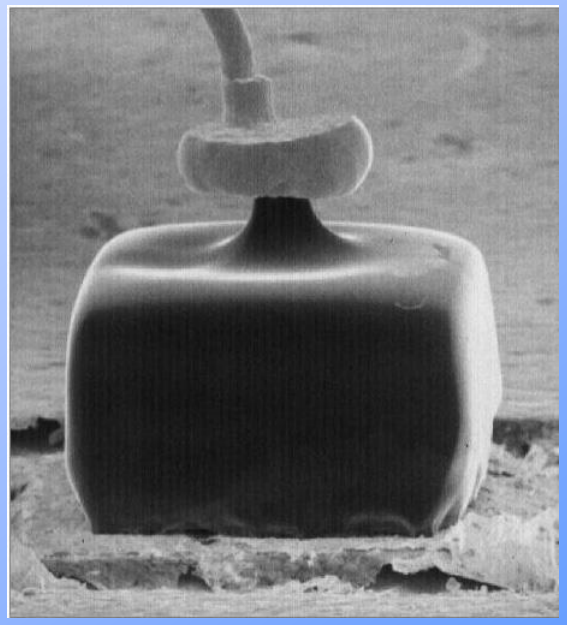



**Degenerate Doping Required – Difficult with conventional epitaxy**

For more info see L. Esaki, "New phenomenon in narrow Germanium p-n junctions," *Phys. Rev.*, vol. 109, p. 603, 1958.

# Prior Art: Lack of Si-Based TDs that can be Monolithically Integrated with Si transistors



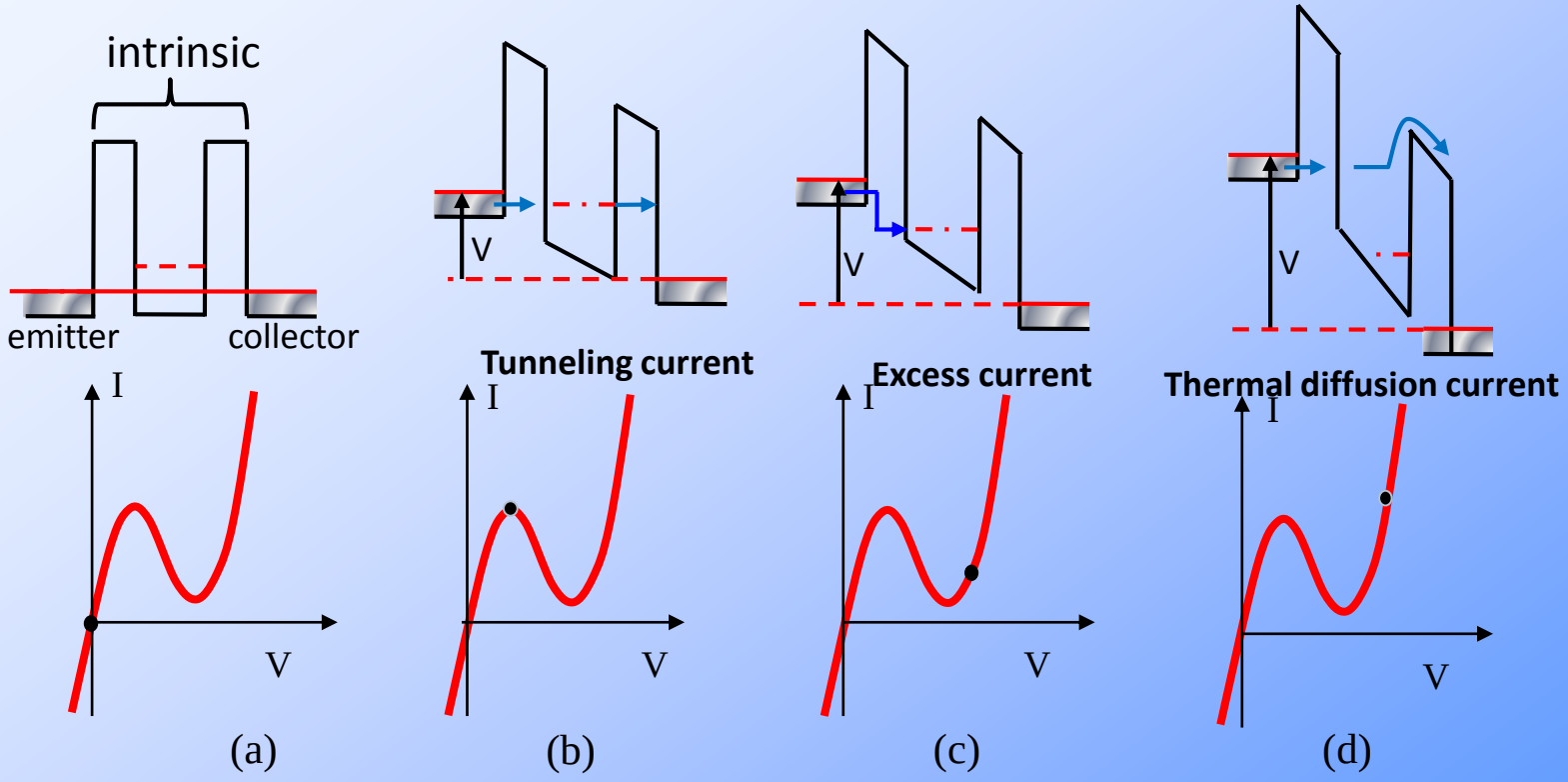



**Ge Esaki Diode**

**Si Esaki Diode**

- Vintage 1960's alloy technology prevents large-scale batch processing
- Discrete Esaki diodes are ideal for niche applications.
- However the alloy process does not lend itself to an integrated circuit.

# Basic Physics: Resonant Tunneling Diode (Intraband)



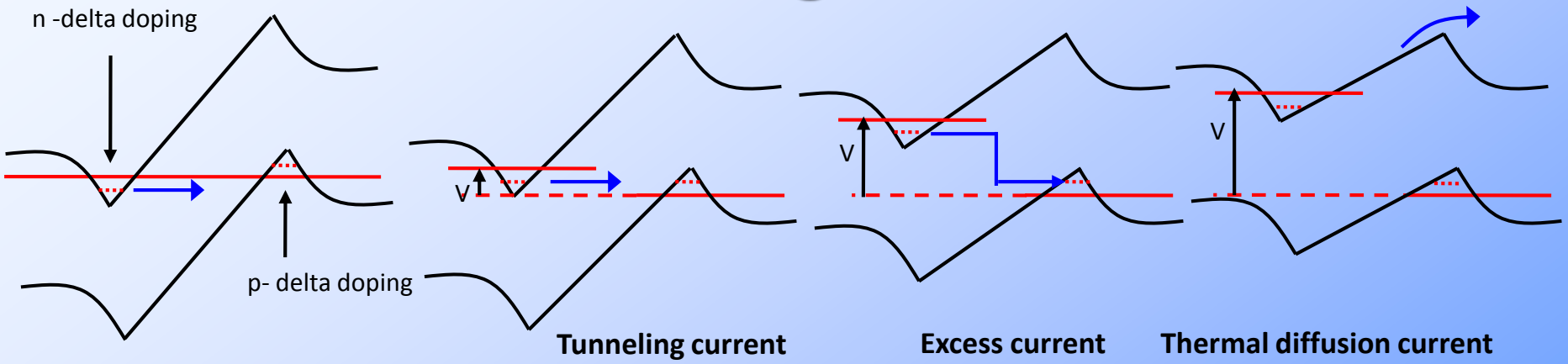

**Large Band Offset Required**

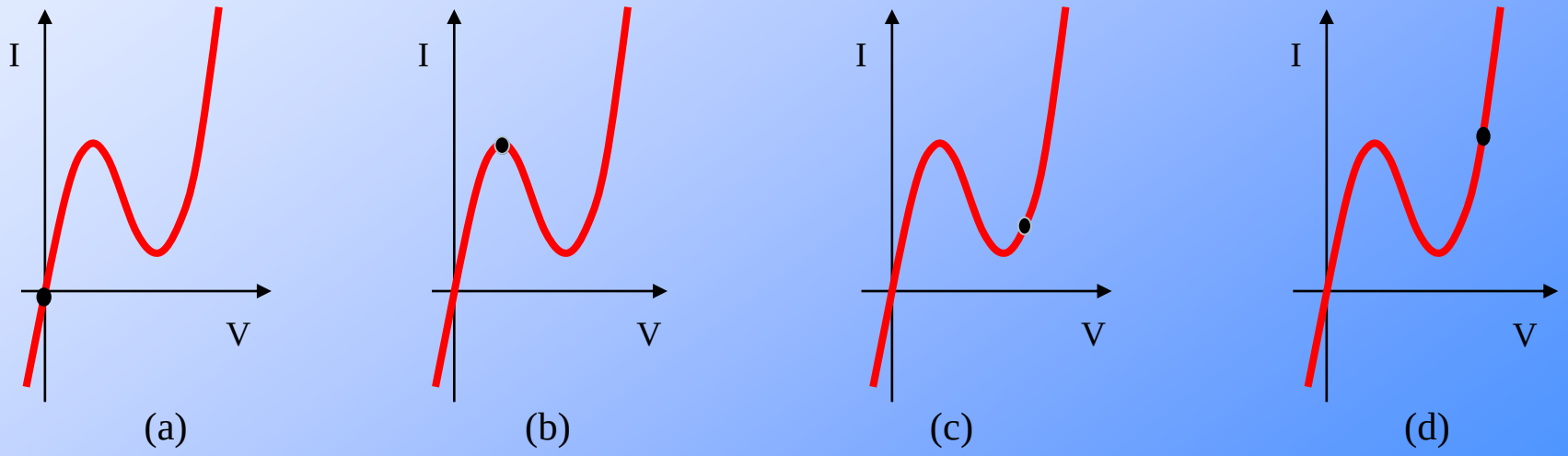
**Si/SiGe heterojunction has limited band offset without a thick relaxed buffer**

**Alternative barriers (i.e. $SiO_2$) present difficult heteroepitaxy of single crystal Si quantum well atop amorphous barrier**

For more info see L. L. Chang, L. Esaki and R. Tsu, "Resonant tunneling in semiconductor double barriers," *Appl. Phys. Lett.*, vol. 24, pp. 593-595, 1974.

# Basic Physics: Resonant Interband Tunneling Diode

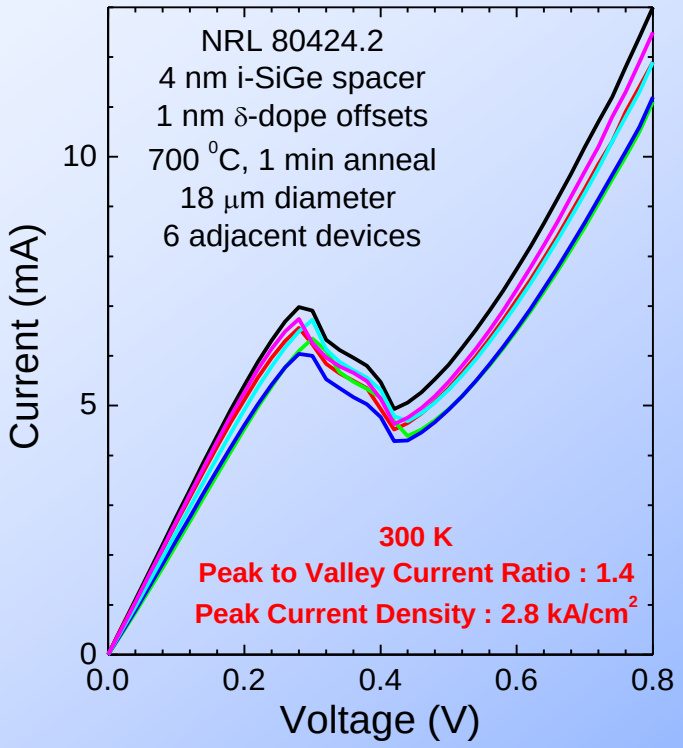



For more info see M. Sweeny and J. Xu, "Resonant interband tunnel diodes," *Appl. Phys. Lett.*, vol. 54, pp. 546-548, 1989.

**δ-doping to form quantum wells; eliminates need for degenerately doped junctions**

# World's First Si-Based Resonant Interband Tunnel Diode (1998)



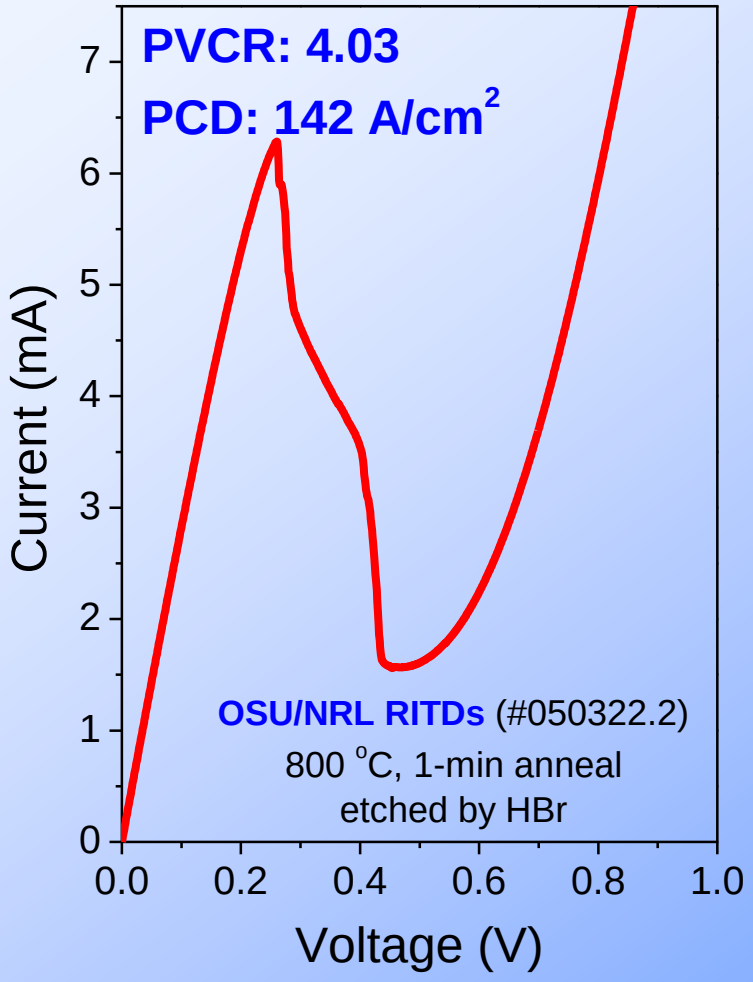

- Low growth temperature (320 °C)
- CMOS process compatibility

| |
|---|
| 100 nm n+ Si |
| Sb-delta doping plane |
| 1 nm undoped Si |
| 4 nm undoped $Si_{0.5}Ge_{0.5}$ |
| 1 nm undoped Si |
| B-delta doping plane |
| 100 nm p+Si |
| p+ Si substrate |

"Room Temperature Operation of Epitaxially Grown $Si/Si_{0.5}Ge_{0.5}/Si$ Resonant Interband Tunneling Diodes," Sean L. Rommel, Thomas E. Dillon, M. W. Dashiell, H. Feng, J. Kolodzey, Paul R. Berger, Phillip E. Thompson, Karl D. Hobart, Roger Lake, Alan C. Seabaugh, Gerhard Klimeck, and Daniel K. Blanks, *Appl. Phys. Lett.*, **73**, pp. 2191-2193 (1998).

**MBE Heterostructure**

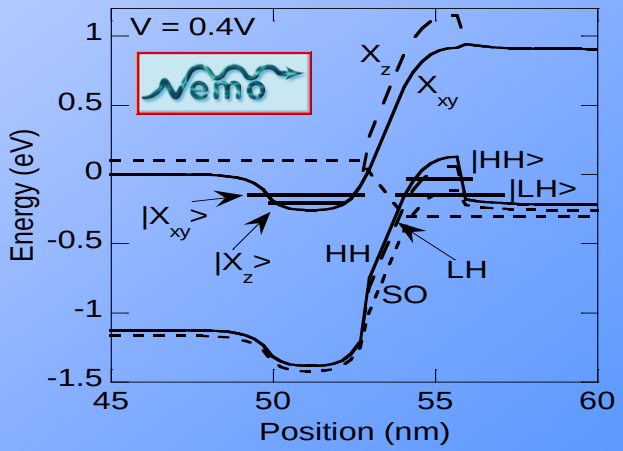
# High Peak-to-Valley Current Ratios




## MBE Heterostructure

Si/$Si_{0.6}Ge_{0.4}$/Si RITDs
Grown at 320 °C

| | |
|---|---|
| | 100 nm n+ Si |
| | P δ-doping plane |
| Tunnel Barrier | 4 nm undoped Si |
| Tunnel Barrier | 4 nm undoped $Si_{0.6}Ge_{0.4}$ |
| | B δ-doping plane |
| | 1 nm p+ $Si_{0.6}Ge_{0.4}$ |
| | 100 nm p+ Si |
| | p+ Si substrate |




Courtesy R. Lake (UC Riverside)

**Greater defect annihilation leads to less excess current in valley region and therefore higher PVCRs**




National Science Foundation
Celebrating 50 Years

# First Si-Based Resonant Interband Tunnel Diodes

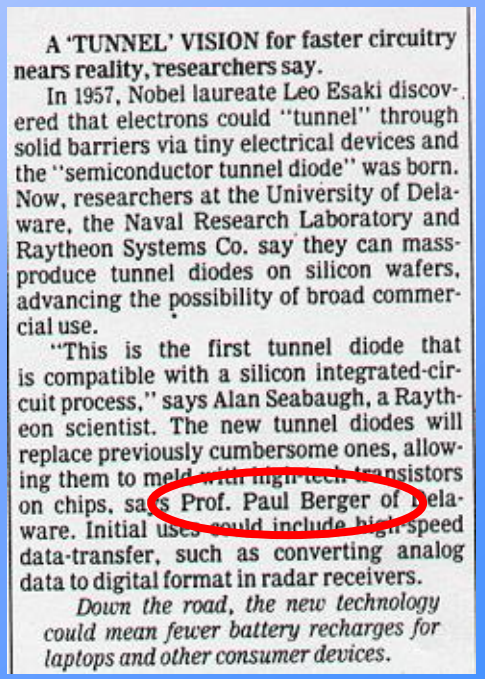
| Approach | $\Delta E_C$ (eV) | Upper Barrier Crystalline | Quantum Well Crystalline | Lower Barrier Crystalline | Production Potential | Status |
|---|---|---|---|---|---|---|
| $SiO_2$/a-Si/$SiO_2$ | 3.2 | No | No | No | High | Abandoned - High scattering in quantum, no room temperature PVR |
| $CaF_2$/Si/$CaF_2$ | 2 | Yes | Yes | Yes | Low | Abandoned - Tendency for island growth, defect-assisted transport below 10 nm |
| ZnS/Si/ZnS | 1 | Yes | Yes | Yes | Med. | ZnS on Si growth established, Si quantum well growth under study |
| $SiO_2$/Si/$SiO_2$ Lateral overgrowth | 3.2 | No | Yes | No | Med. | Process for forming oxide islands established, overgrowth process under development |
| ZnS/Si/ZnS Lateral overgrowth | 1 | Yes | Yes | Yes | Med. | ZnS islands have been prepared for first overgrowth experiments |
| $SiO_2$/SiGe(C)/$SiO_2$ Lateral overgrowth | 3.2 | No | Yes | No | Med. | Oxide islands have been prepared for first overgrowth experiments |
| Si/SiGe resonant interband tunnel diode | - | - | - | - | High | World's first demonstration on Si; room temperature peak-to-valley current ratio of 1.6 |

980505

A paradigm shift from other approaches was spearheaded by a team of researchers lead by Berger (then at the University of Delaware), Naval Research Laboratory and Raytheon Systems.

- DARPA Award of Excellence (1998)
- Late News at International Electron Devices Meeting (1998)
- Best Science/Engineering Dissertation (2000)
- Special Invitation to 2003 ITRS Meeting
- IEEE Fellow (2011)

Front page of the Wall Street Journal (October 1, 1998).



A 'TUNNEL' VISION for faster circuitry nears reality, researchers say.

In 1957, Nobel laureate Leo Esaki discovered that electrons could "tunnel" through solid barriers via tiny electrical devices and the "semiconductor tunnel diode" was born. Now, researchers at the University of Delaware, the Naval Research Laboratory and Raytheon Systems Co. say they can mass-produce tunnel diodes on silicon wafers, advancing the possibility of broad commercial use.

"This is the first tunnel diode that is compatible with a silicon integrated-circuit process," says Alan Seabaugh, a Raytheon scientist. The new tunnel diodes will replace previously cumbersome ones, allowing them to meld with high-tech transistors on chips, says Prof. Paul Berger of Delaware. Initial uses could include high-speed data-transfer, such as converting analog data to digital format in radar receivers.

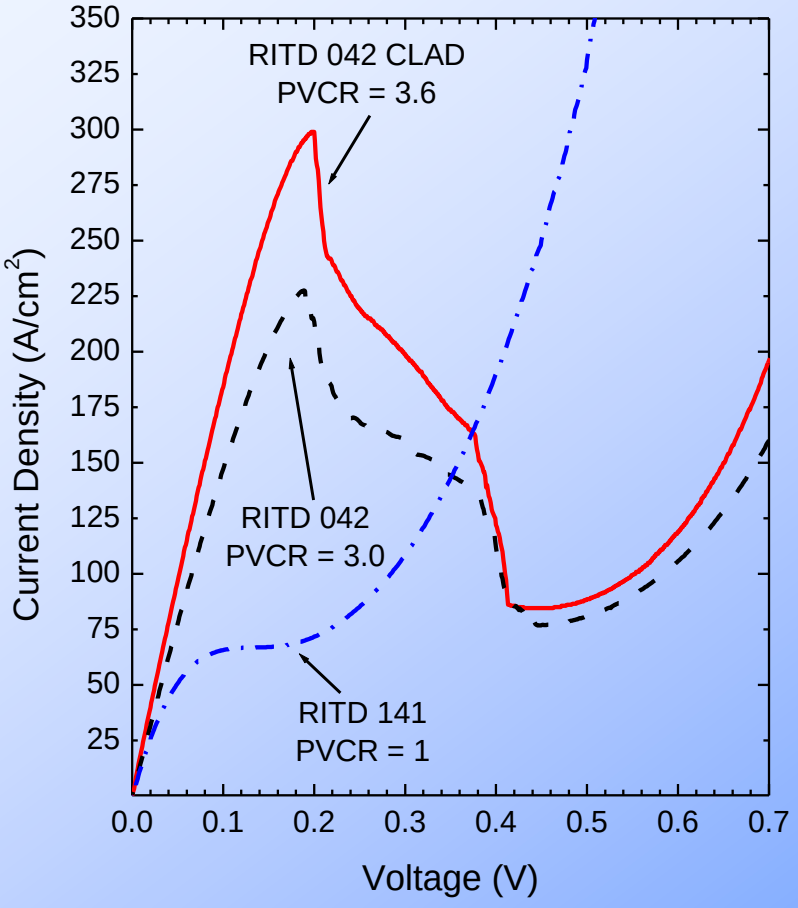
*Down the road, the new technology could mean fewer battery recharges for laptops and other consumer devices.*

# 5 Key Features of the Original RITD Design

- A pair of **δ-doping planes of B and P (or Sb)** provide highly degenerate doping levels which can confine quantum states in potential energy wells. The gap between δ-doping planes is assumed the tunneling distance.
- An **intrinsic layer** is used as the central tunneling spacer, which reduces carrier scattering. Both Si and $Si/Si_{1-x}Ge_x$ composite spacers have been explored. The addition of Ge provides greater momentum mixing and therefore higher current densities.
- Fixed **offsets between the δ-doping planes and the tunneling spacer** were introduced in some SiGe designs to minimize the outdiffusion of dopants and impurity accumulation into the central tunneling spacer.
- Samples were epitaxially grown by **low-temperature molecular beam epitaxy (LT-MBE)** to allow for greater dopant incorporation and abrupt interfaces minimizing segregation and diffusion.
- Short post growth **rapid thermal annealing (RTA) heat treatments** were introduced to reduce the point defect density associated with low temperature growth. Diffusion during annealing may decrease the spacer thickness and reduce as-grown δ-doping levels.


- "Si-Based Resonant Interband Tunneling Diodes," Paul R. Berger, Sean L. Rommel, Phillip E. Thompson, Karl D. Hobart, and Roger Lake, [Issued on October 12, 2004, U. S. Patent #6,803,598].
- "Method of Making Interband Tunneling Diodes," Paul R. Berger, Sean L. Rommel, Phillip E. Thompson, Karl D. Hobart, and Roger Lake, (U. S. Patent #7,303,969).

# Isothermal Annealing Effects with Cladding

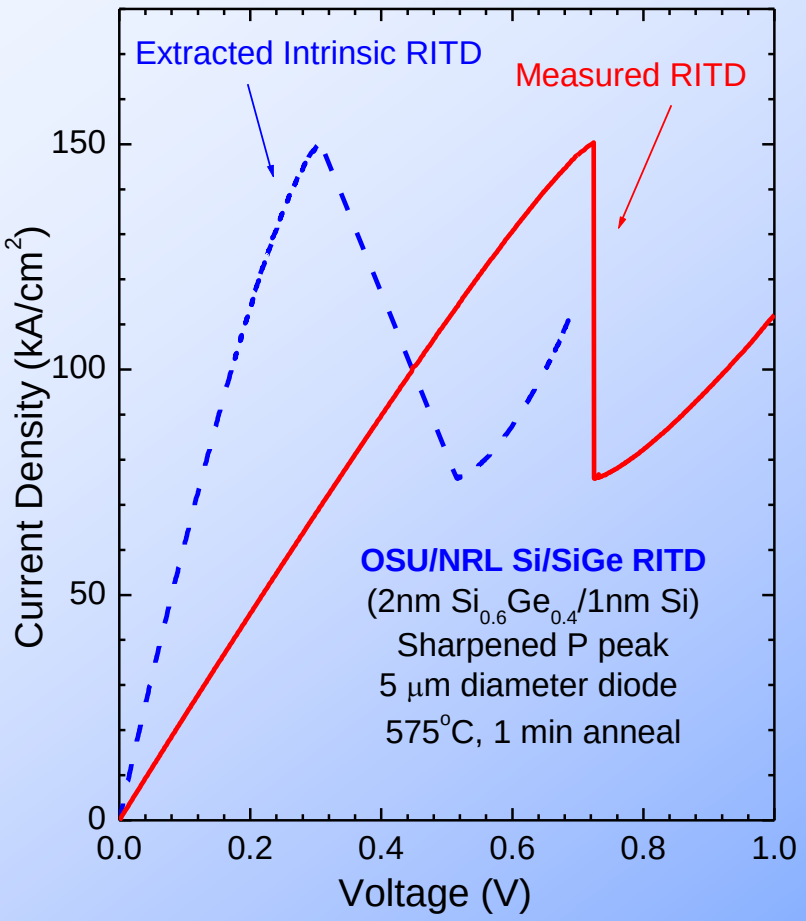



**Diffusion barrier cladding surrounding the δ-doping spike raises the process thermal budget and allows for greater defect annihilation before interdiffusion becomes serious**

"Diffusion Barrier Cladding in Si/SiGe Resonant Interband Tunneling Diodes And Their Patterned Growth on PMOS Source/Drain Regions," Niu Jin, Sung-Yong Chung, Anthony T. Rice, Paul R. Berger, Phillip E. Thompson, Cristian Rivas, Roger Lake, Stephen Sudirgo, Jeremy J. Kempisty, Branislav Curanovic, Sean L. Rommel, Karl D. Hirschman, Santosh K. Kurinec, Peter H. Chi and David S. Simons, *Special Issue on "Nanoelectronics" in IEEE Trans. Elect. Dev., **vol. 50**, pp. 1876-1884 (September 2003).*

**Annealed 825 ºC for 1 minute**

# Very High Peak Current Densities




**$Si/Si_{0.6}Ge_{0.4}/Si$ RITDs Grown at 320 °C**

Tunnel Barrier

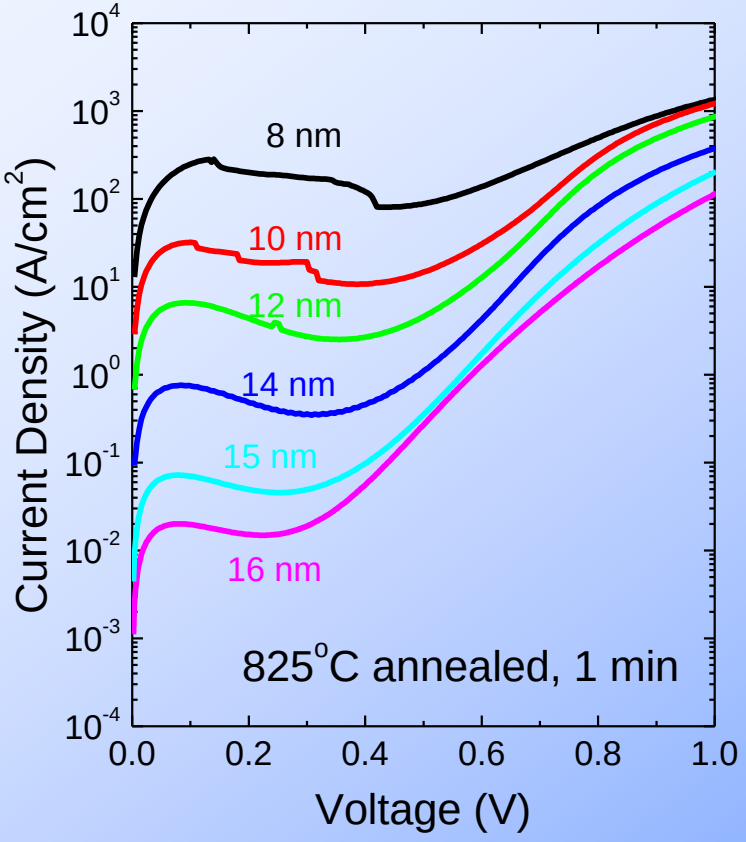
| |
|---|
| 100 nm n+ Si |
| P δ-doping plane |
| 1 nm undoped Si |
| 2 nm undoped $Si_{0.6}Ge_{0.4}$ |
| B δ-doping plane |
| 1 nm undoped $Si_{0.6}Ge_{0.4}$ |
| 100 nm p+ Si |
| p+ Si substrate |

*"151 kA/cm² Peak Current Densities in Si/SiGe Resonant Interband Tunneling Diodes for High-Power Mixed-Signal Applications," Niu Jin, Sung-Yong Chung, Anthony T. Rice, Paul R. Berger, Ronghua Yu, Phillip E. Thompson, and Roger Lake., Appl. Phys. Lett., **83**, 3308 (2003).*

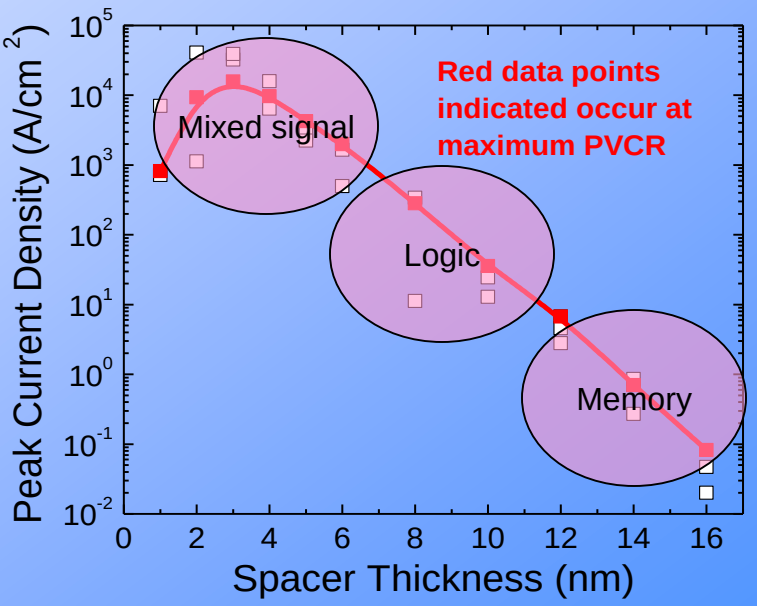
**By reducing tunnel barrier, over 150 kA/cm² current density!**

**High current densities valuable for fast switching and RF Mixed Signals**

# Tailorable Peak Current Densities




Current densities can be engineered over ~8 orders of magnitude by controlling RITD spacer thickness between the δ-doping pair from 1 nm up to 16 nm.




**By widening spacer, below 20 mA/cm² current density!**

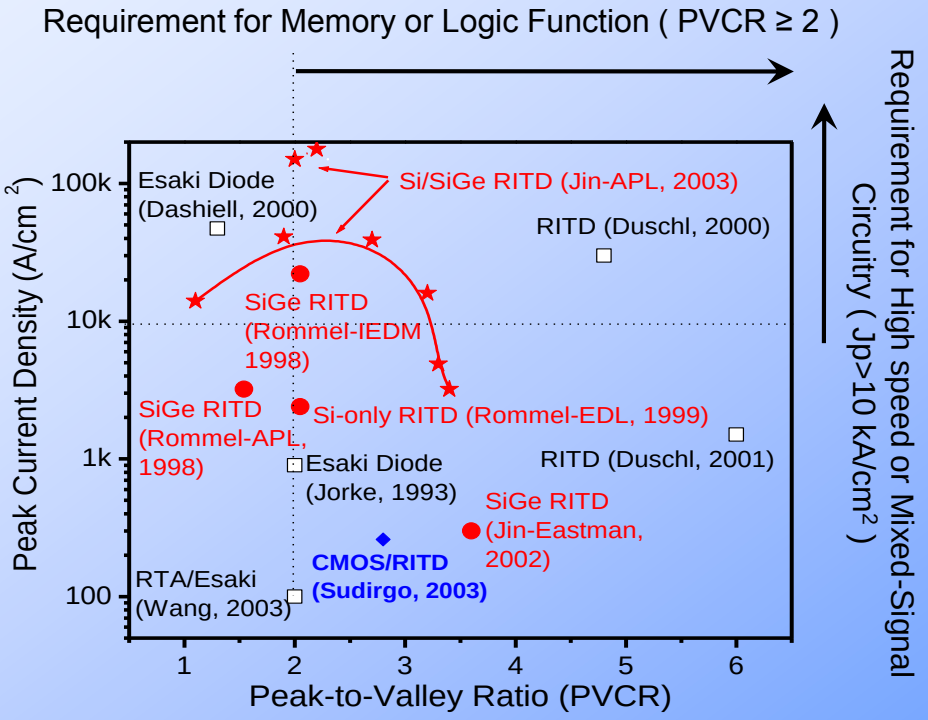
**Low current densities valuable for memory and low power consumption**



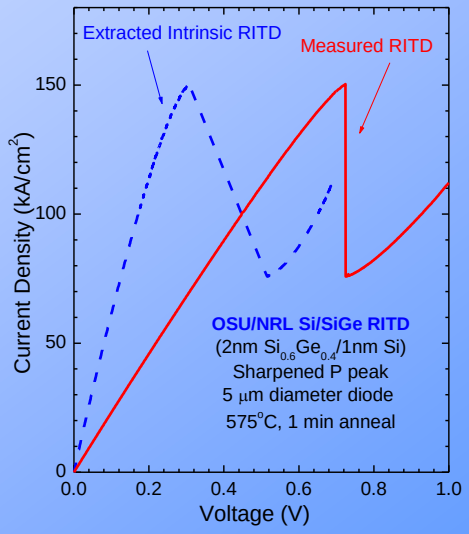
National Science Foundation Celebrating 50 Years

# RF Mixed Signal Applications Enabled

Results highlighted here demonstrate the highest reported peak current density for Si-based interband tunnel diodes that is 3 times larger than the previous world record. A high current density is needed to generate large amounts of microwave power output for radio transmission in small distributed sensor networks




Solid circles (●) indicate prior work by Berger group, open squares (□) indicate prior work by other groups, and stars (*) indicate recent work by Berger group.




*"151 kA/cm² Peak Current Densities in Si/SiGe Resonant Interband Tunneling Diodes for High-Power Mixed-Signal Applications," Niu Jin, Sung-Yong Chung, Anthony T. Rice, Paul R. Berger, Ronghua Yu, Phillip E. Thompson, and Roger Lake., Appl. Phys. Lett., **83**, 3308 (2003).*

# Microwave Performance of RITDs

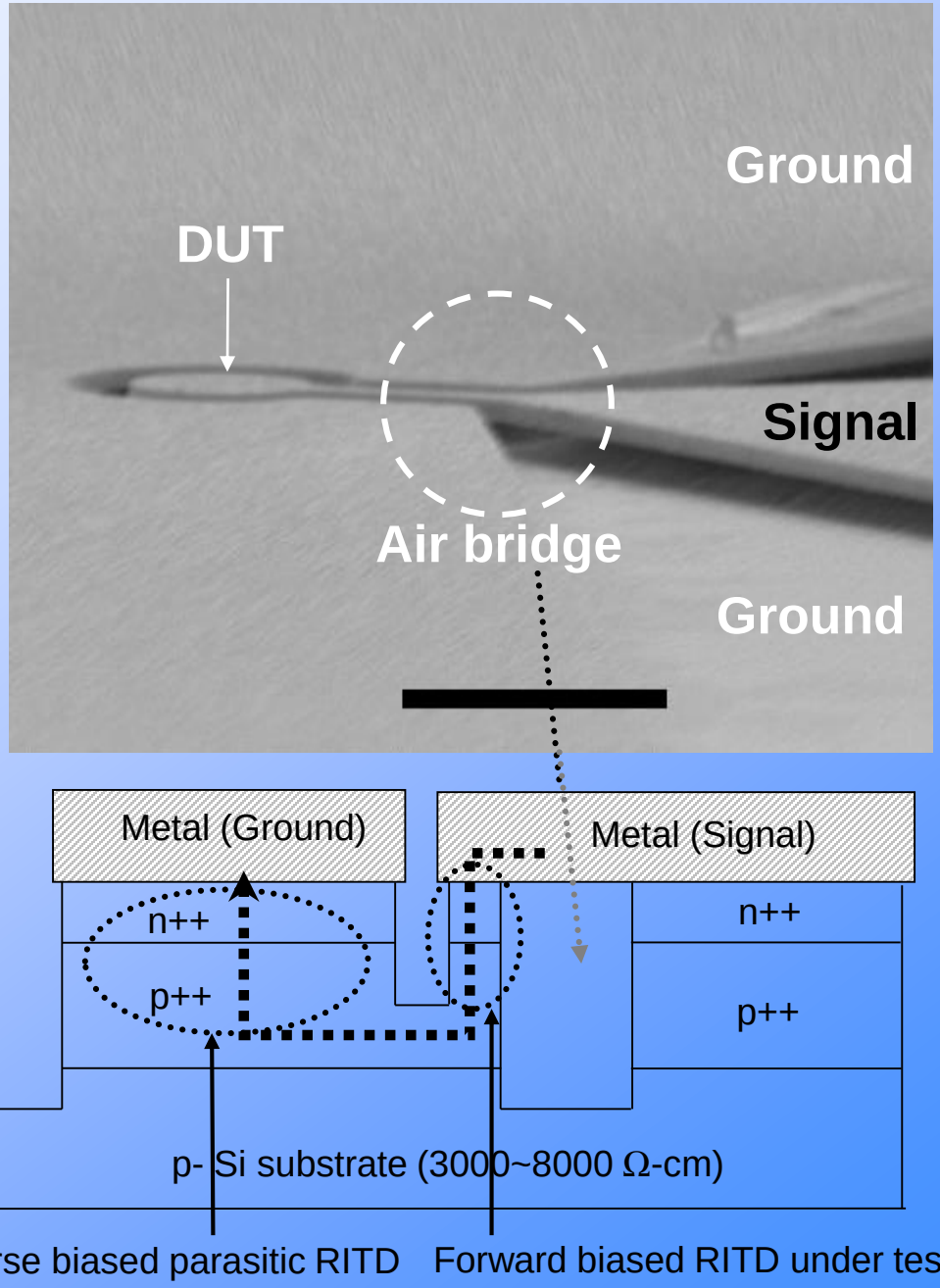
| |
|---|
| 5 nm $n^+$ Si |
| P δ-doping plane |
| 104 nm $n^+$ Si |
| P δ-doping plane |
| 1 nm undoped Si |
| 1.5 nm undoped $Si_{0.45}Ge_{0.55}$ |
| B δ-doping plane |
| 1 nm $p^+$ $Si_{0.45}Ge_{0.55}$ |
| 264 nm $p^+$ Si |
| p Si Substrate (3000-8500 Ω·cm) |

## STRUCTURE Uniqueness

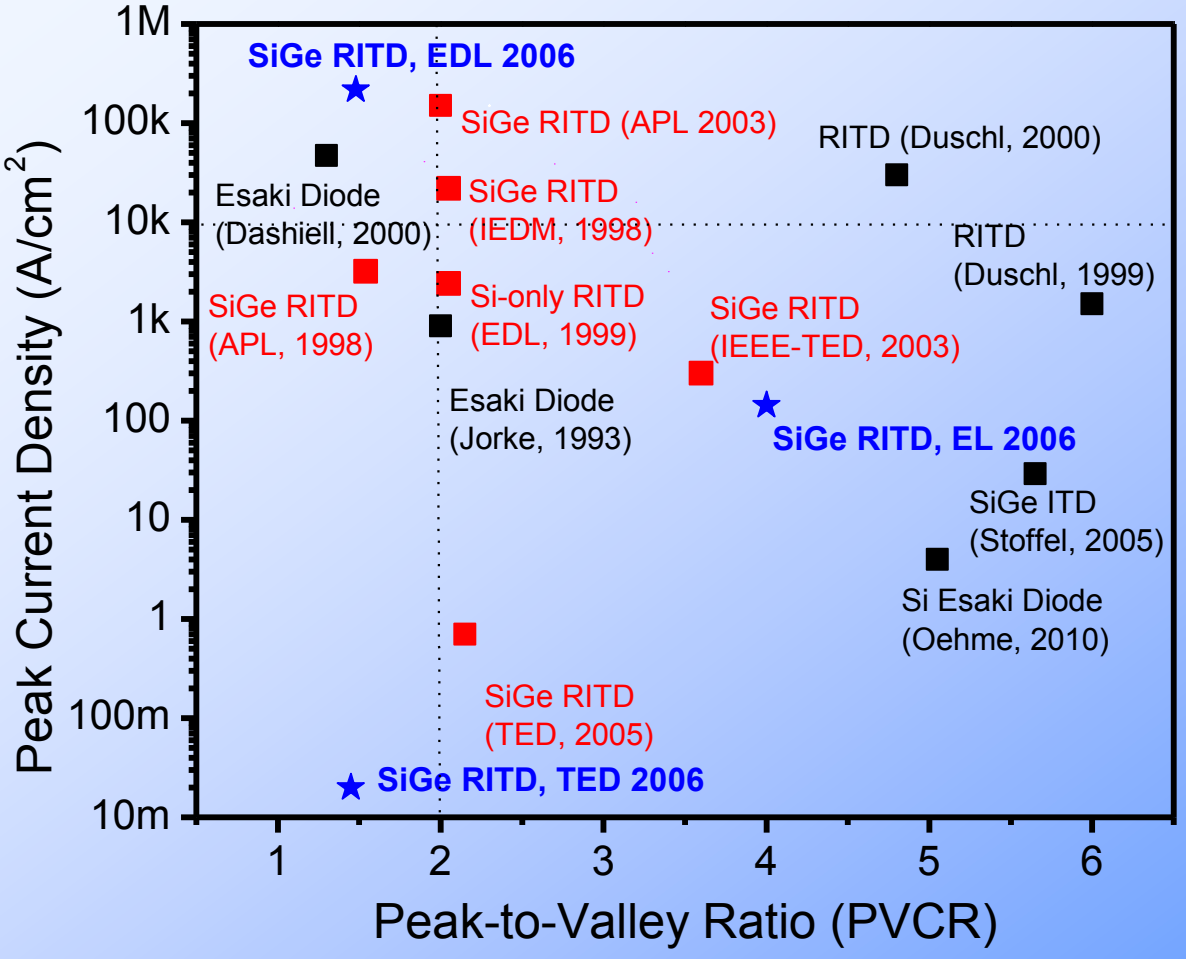
- Additional P δ-doped layer was inserted for better ohmic contact.
- Ni silicide was formed.
- Minimum space thickness (2.5 nm) with the highest Ge fraction (55 %) was tried.
- **218 kA/cm$^2$ peak current density.**
- **20.2 GHz cutoff frequency.**
- **35.9 mV/ps of speed index.**

# Device Fabrication For RF measurement

- 1 metal & 2 etching processes have been developed, resulting in **0.34 $\mu m^2$** sized RITDs.
- Air-bridge is formed to isolate a active device from huge pad.
- Ni silicidation through P $\delta$-doped quantum well by rapid thermal sintering at 430 $^oC$ for 30 seconds, resulting in a specific contact resistivity of $5.3 \times 10^{-7}$ $\Omega$-cm$^2$, which is extracted from RF measurement.



# Si-based Interband Tunnel Diode Technology (PCD & PVCR)



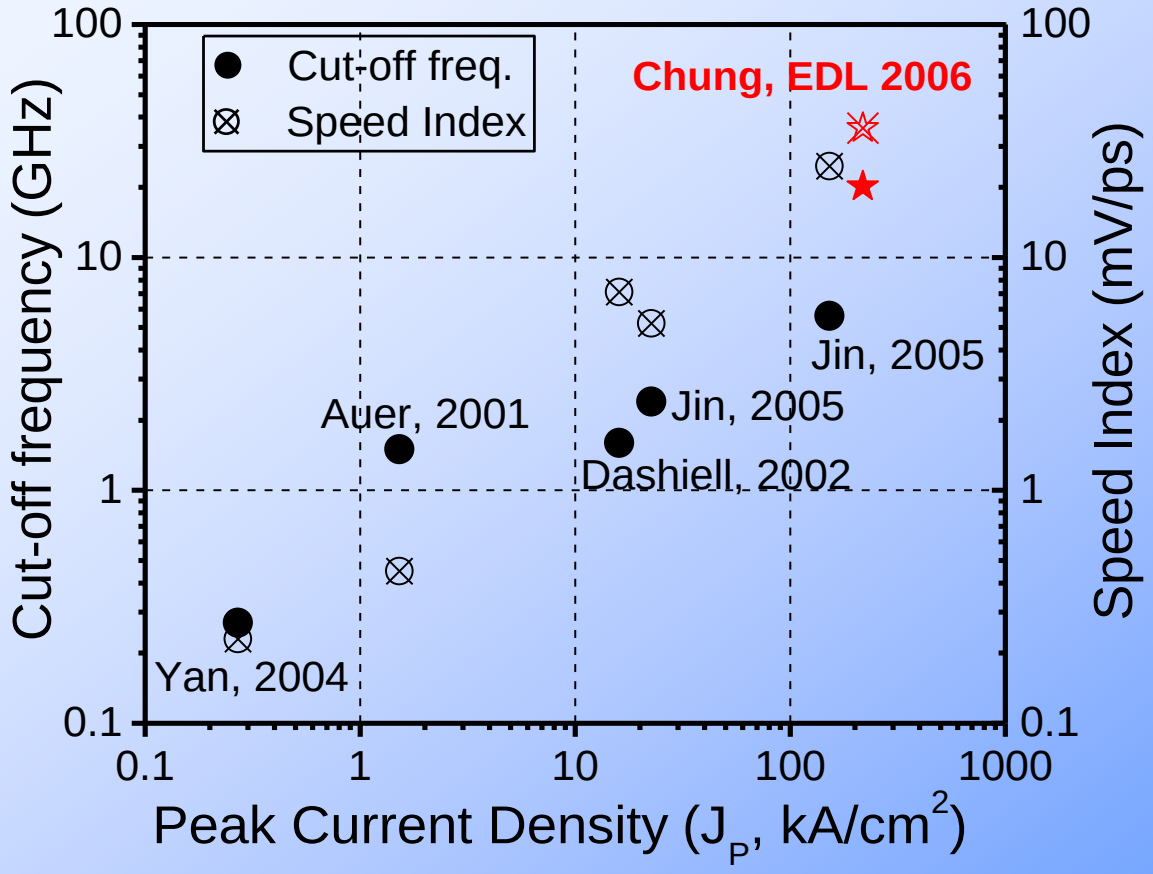

## Technology Availability

PVCR up to **4**

PCD: **20 mA/cm²** to **218 kA/cm²**

*"Si/SiGe Resonant Interband Tunnel Diode with $f_{r0}$ 20.2 GHz and Peak Current Density 218 kA/cm2 for K-band Mixed-Signal Applications," Sung-Yong Chung, Ronghua Yu, Niu Jin, Si-Young Park, Paul R. Berger, and Phillip E. Thompson, IEEE Electron Device Letters 27, pp. 364-367 (May 2006).*

# Si-based Interband Tunnel Diode Technology (Speed)




**Technology Availability**

$f_T$: up to **20.2 GHz**

Switching Speed: ~ **36 mV/ps**

*"Si/SiGe Resonant Interband Tunnel Diode with $f_{r0}$ 20.2 GHz and Peak Current Density 218 kA/cm2 for K-band Mixed-Signal Applications," Sung-Yong Chung, Ronghua Yu, Niu Jin, Si-Young Park, Paul R. Berger, and Phillip E. Thompson, IEEE Electron Device Letters 27, pp. 364-367 (May 2006).*

# Tensile Strain on Virtual SiGe

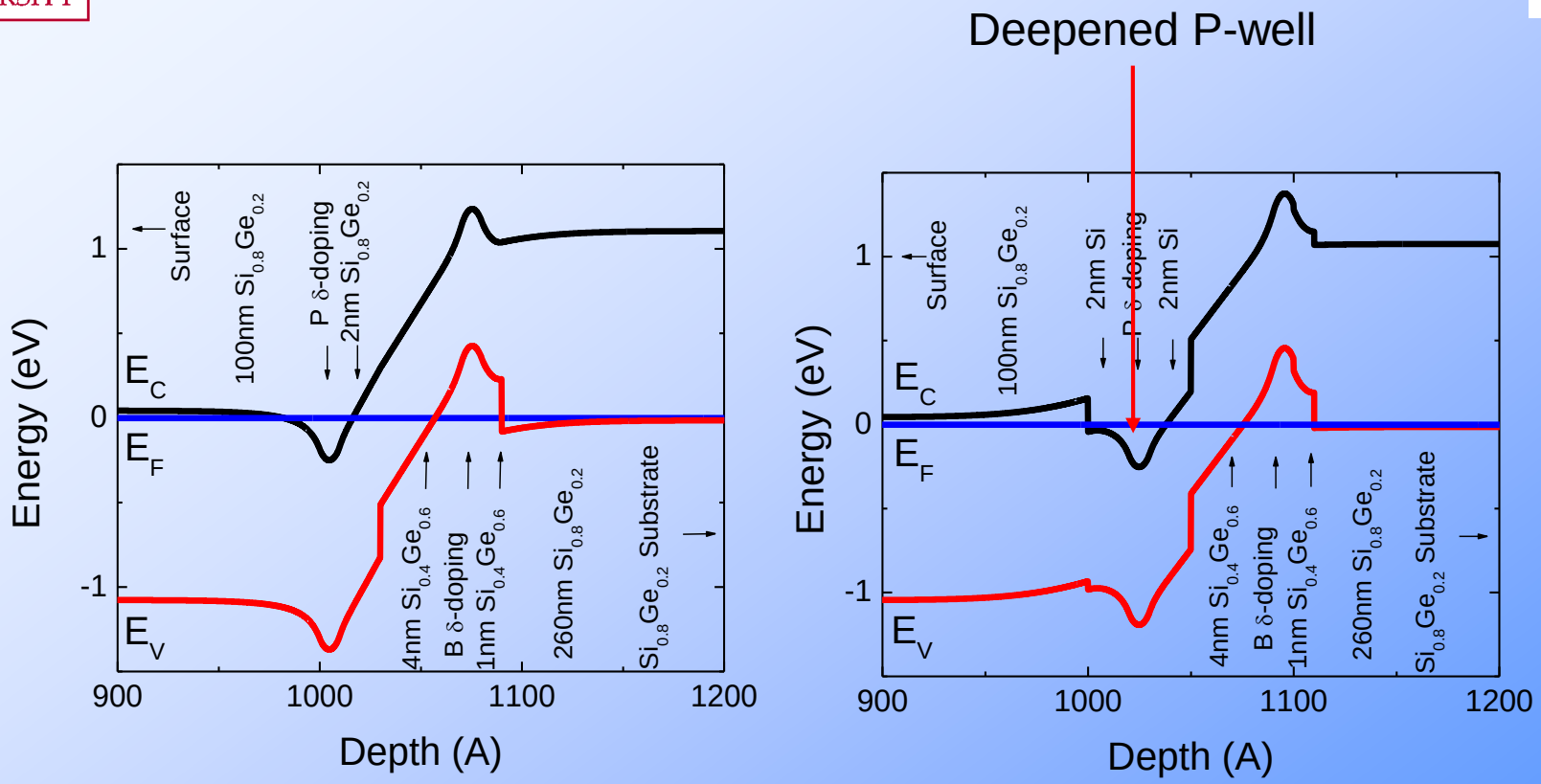
- SiGe virtual substrates utilized for higher Ge content in the spacer to increase tunneling probability
- Thin tensilely strained Si layer cladding around P δ-doping spike acting as a P diffusion inhibitor

| Structure 'A' |
|---|
| 100 nm n+ $Si_{0.8}Ge_{0.2}$ |
| P δ-doping layer |
| 2 nm i $Si_{0.8}Ge_{0.2}$ spacer |
| 4 nm i $Si_{0.4}Ge_{0.6}$ spacer |
| B δ-doping layer |
| 1 nm p+ $Si_{0.4}Ge_{0.6}$ |
| 260 nm p+ $Si_{0.8}Ge_{0.2}$ |
| 17.5 nm Cap Si |
| $Si_{0.8}Ge_{0.2}$ substrate |

| Structure 'B' |
|---|
| 100 nm n+ $Si_{0.8}Ge_{0.2}$ |
| ***2 nm n+ Si*** |
| P δ-doping layer |
| ***2 nm i Si spacer*** |
| 4 nm i $Si_{0.4}Ge_{0.6}$ spacer |
| B δ-doping layer |
| 1 nm p+ $Si_{0.4}Ge_{0.6}$ |
| 260 nm p+ $Si_{0.8}Ge_{0.2}$ |
| 17.5 nm Cap Si |
| $Si_{0.8}Ge_{0.2}$ substrate |

"Strain Engineered Si/SiGe Resonant Interband Tunneling Diodes Grown on $Si_{0.8}Ge_{0.2}$ Virtual Substrates," *N. Jin et.al.*, *IEEE EDL, 29, 599 (2008)*

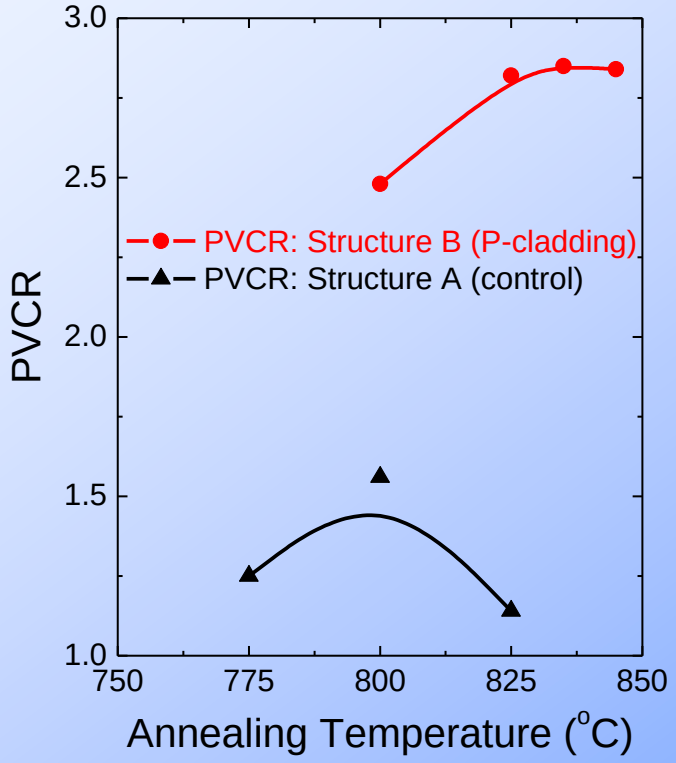
# Tensile Strain on Virtual SiGe

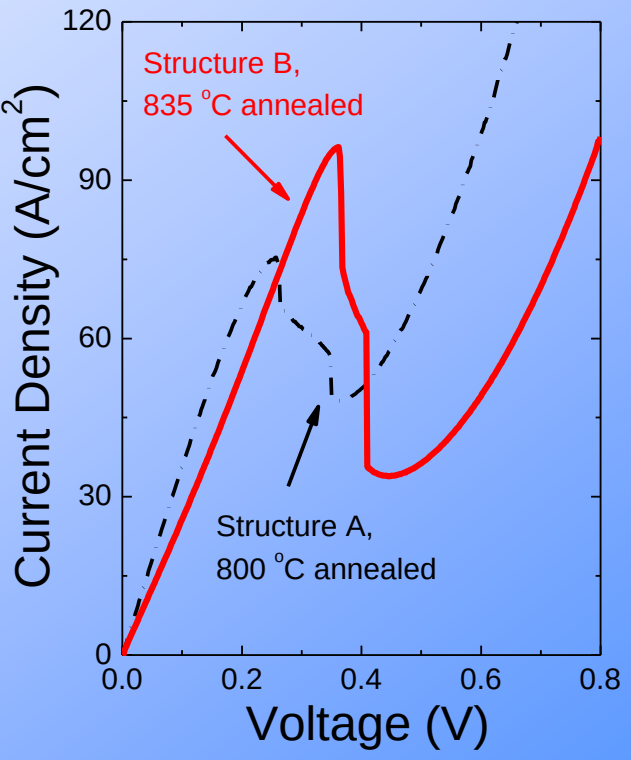



"Strain Engineered Si/SiGe Resonant Interband Tunneling Diodes Grown on $Si_{0.8}Ge_{0.2}$ Virtual Substrates," *N. Jin et.al., IEEE EDL, 29, 599 (2008)*

# Tensile Strain on Virtual SiGe

- Increase in optimal annealing temperature due to reduced P diffusion
- **1.8x increase in PVCR**




"Strain Engineered Si/SiGe Resonant Interband Tunneling Diodes Grown on $Si_{0.8}Ge_{0.2}$ Virtual Substrates," *N. Jin et.al., IEEE EDL, 29, 599 (2008)*

# Outside Barriers

- Tensilely strained p-type and compressively strained $Si_{0.5}Ge_{0.5}$ n-type added.

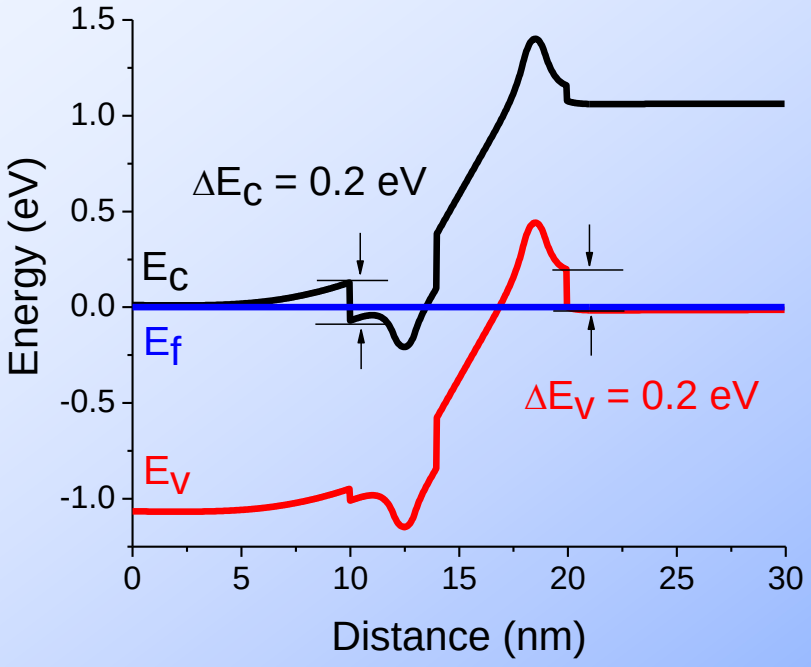
| |
|---|
| 100 nm n+ $Si_{0.8}Ge_{0.2}$ |
| 2 nm n+ Si |
| P delta doping layer |
| 1 nm i Si spacer |
| 4 nm i $Si_{0.5}Ge_{0.5}$ spacer |
| B delta doping layer |
| 1 nm p+ $Si_{0.5}Ge_{0.5}$ |
| 260 nm p+ $Si_{0.8}Ge_{0.2}$ |
| $Si_{0.8}Ge_{0.2}$ substrate |

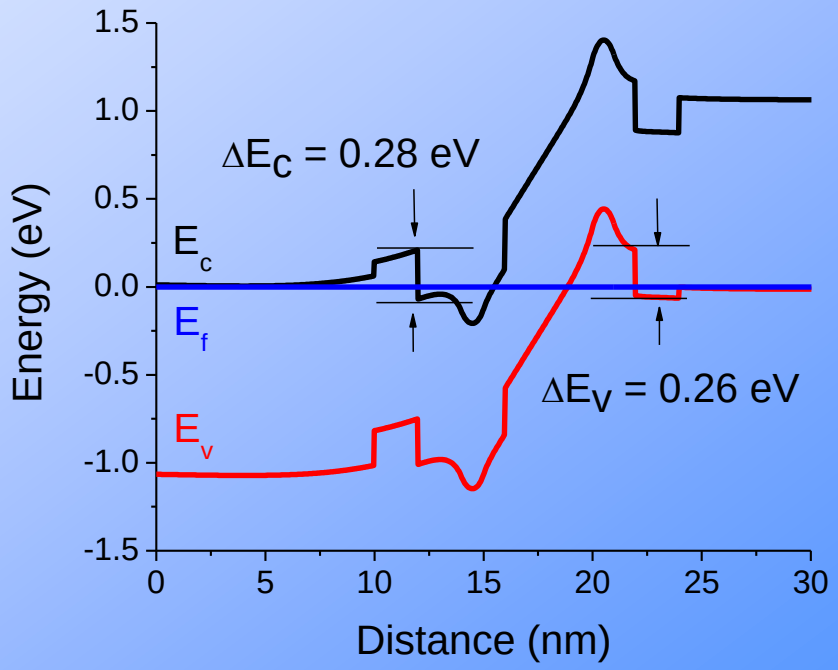
| |
|---|
| 100 nm n+ $Si_{0.8}Ge_{0.2}$ |
| ***2 nm n+ $Si_{0.5}Ge_{0.5}$*** |
| 2 nm n+ Si |
| P delta doping layer |
| 1 nm i Si spacer |
| 4 nm i $Si_{0.5}Ge_{0.5}$ spacer |
| B delta doping layer |
| 1 nm p+ $Si_{0.5}Ge_{0.5}$ |
| ***2 nm p+ Si*** |
| 260 nm p+ $Si_{0.8}Ge_{0.2}$ |
| $Si_{0.8}Ge_{0.2}$ substrate |

"Strain Engineered Si/SiGe Resonant Interband Tunneling Diodes with Outside Barriers Grown on $Si_{0.8}Ge_{0.2}$ Virtual Substrates," *A. Ramesh et.al.*, *APL, 93, 102113 (2008).*

# Outside Barriers

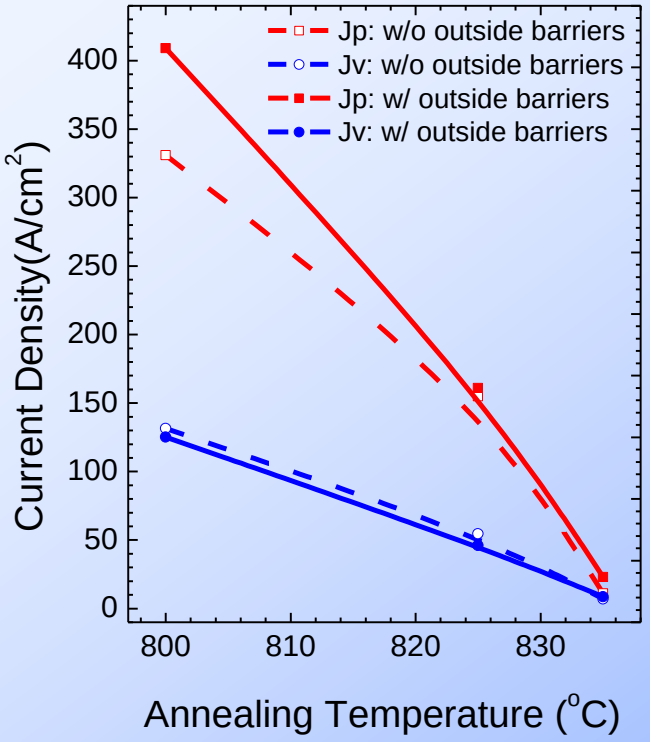
- Electron and hole quantum well deepened.

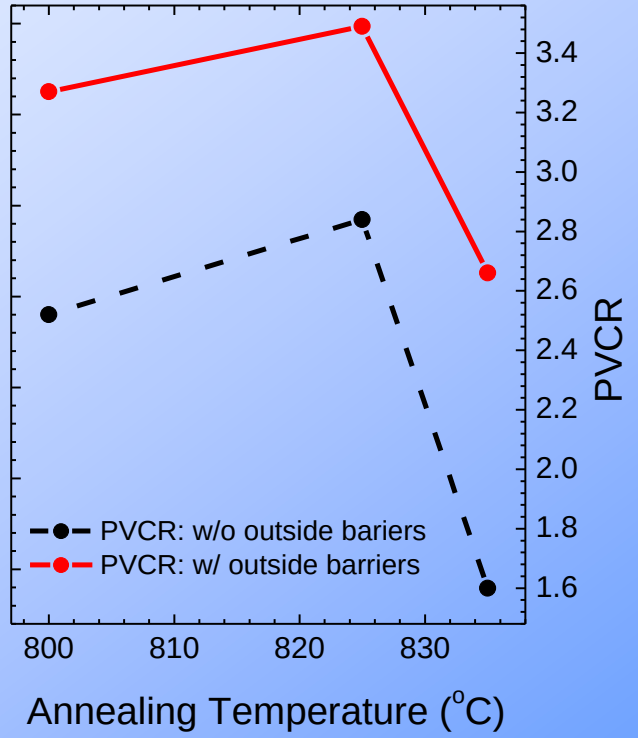



"Strain Engineered Si/SiGe Resonant Interband Tunneling Diodes with Outside Barriers Grown on $Si_{0.8}Ge_{0.2}$ Virtual Substrates," *A. Ramesh et.al.*, APL, 93, 102113 (2008).

# Device Results



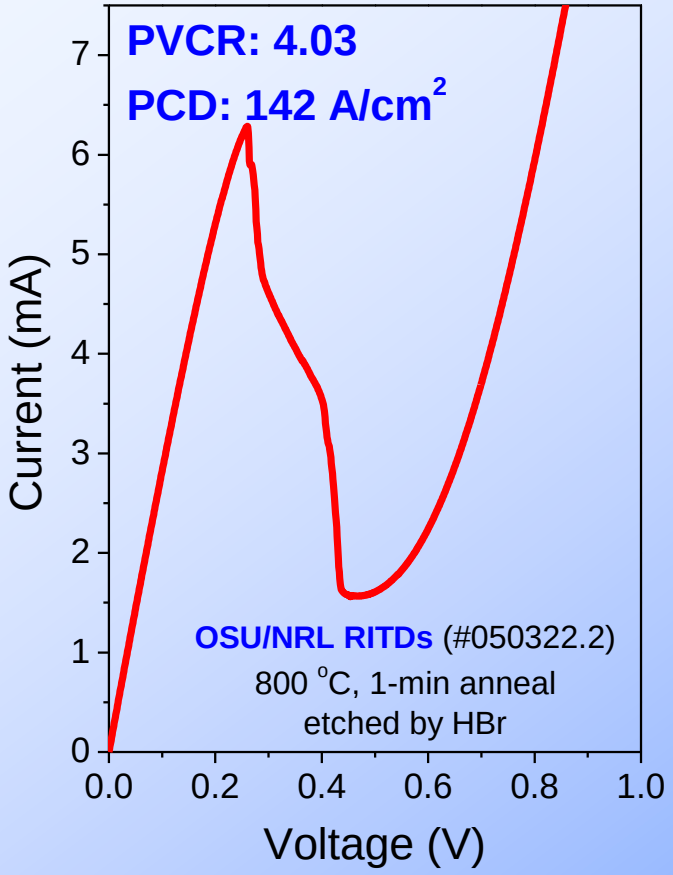




- It is shown that outside barriers can enhance the Jp while reduce the Jv.
- The QW is deepened due to the accumulation of bandgap offset **(Enhance Jp)**
- The barrier can block the non-resonant tunneling current **(Reduce Jv)**

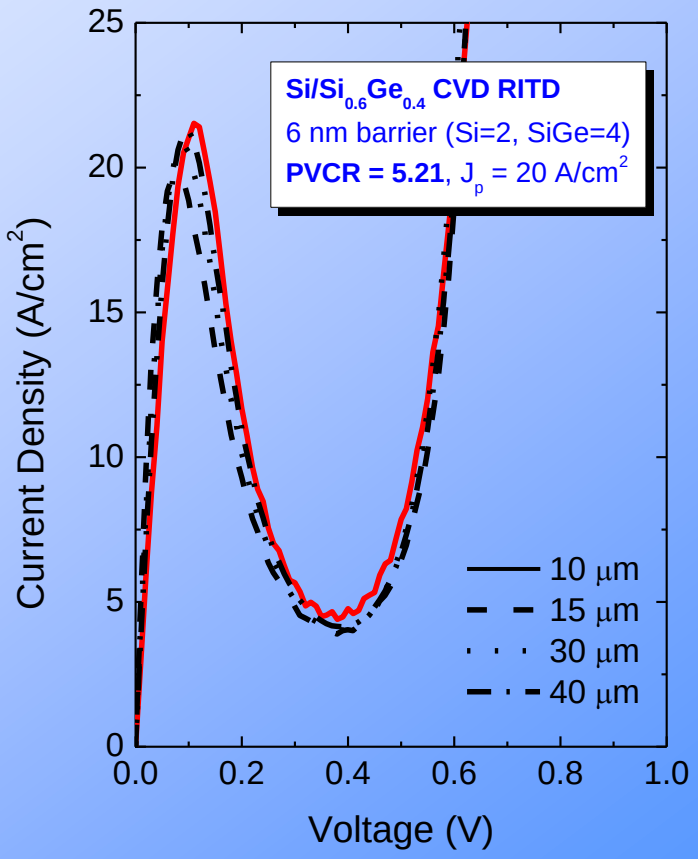
"Strain Engineered Si/SiGe Resonant Interband Tunneling Diodes with Outside Barriers Grown on $Si_{0.8}Ge_{0.2}$ Virtual Substrates," *A. Ramesh et.al.*, APL, 93, 102113 (2008).

# Technology Transfer: RITD

## MBE Prototype




## CVD Tech Transfer *

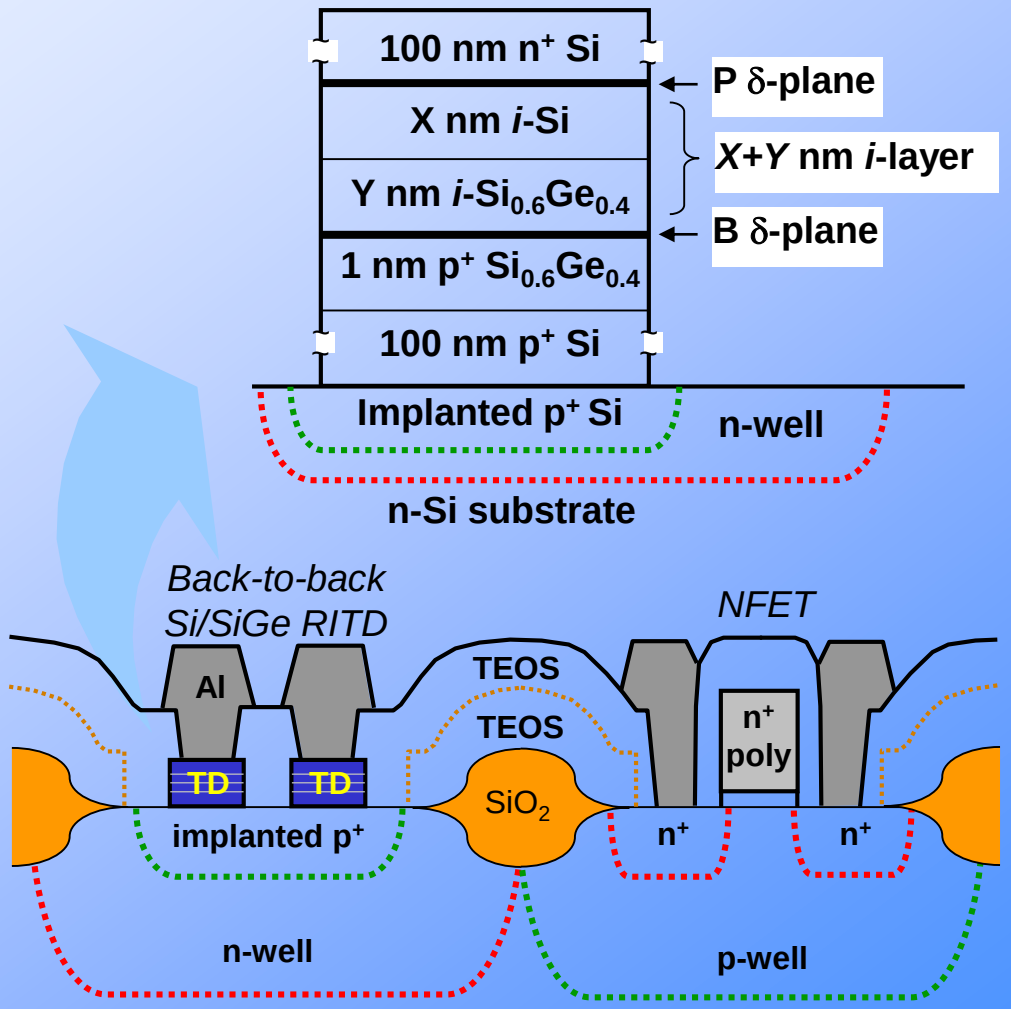



*** Grown on a standard ASM reactor (200 mm) at IMEC**

"High 5.2 Peak-to-Valley Current Ratio in Si/SiGe Resonant Interband Tunnel Diodes Grown by Chemical Vapor Deposition," *A. Ramesh et.al.*, APL, 100, 092104 (2012).

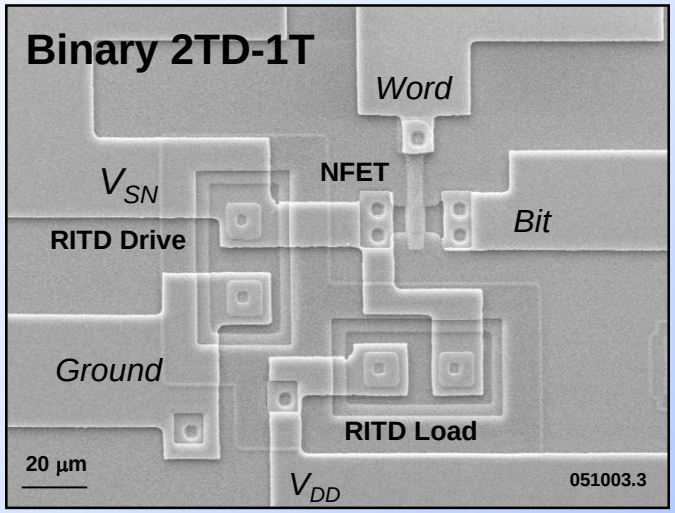
# Fabrication Technology Developed

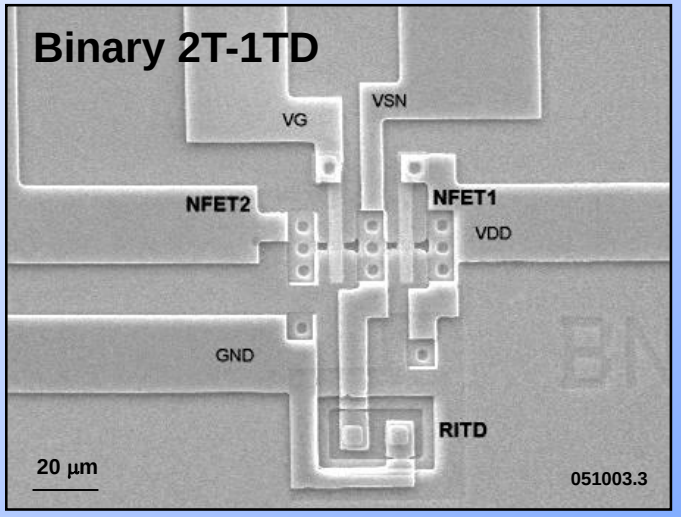
- Over 80 major steps
- LOCOS isolation
- Double well technology
- n+ polysilicon gate
- Self-aligned S/D
- Low Temperature Molecular Beam Epitaxy (NRL)
- Post Growth Rapid Thermal Anneal (OSU)
- Al(1%Si) Metalization

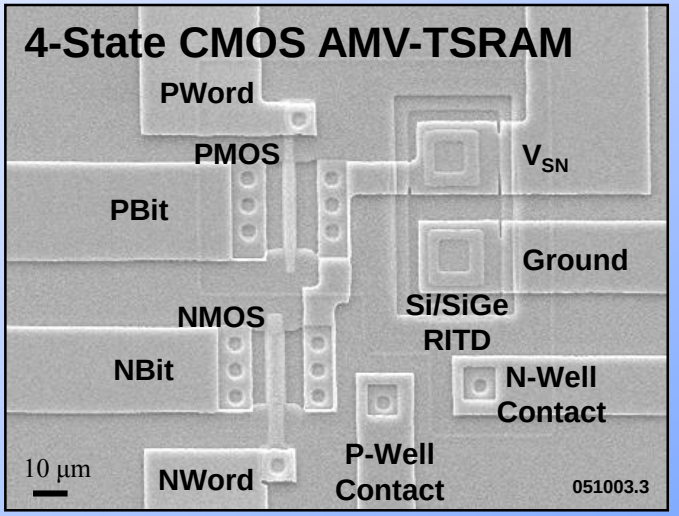


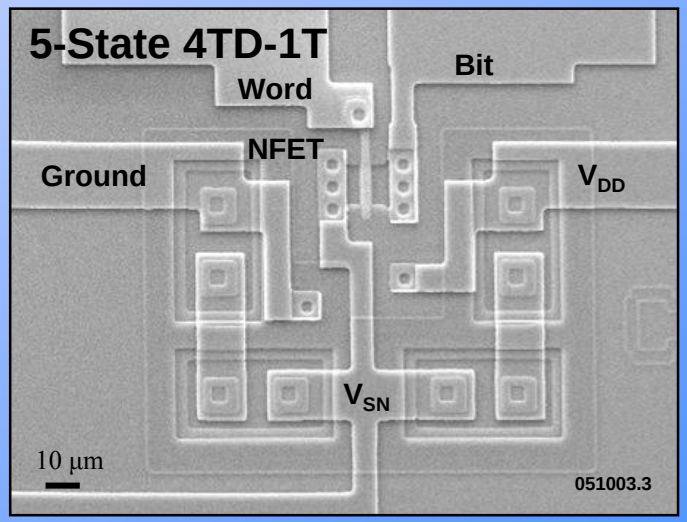

"NMOS/SiGe Resonant Interband Tunneling Diode Static Random Access Memory," S. Sudirgo, *et al.*, *Proceedings of the Device Research Conference (State College, PA, USA, 2006)*, p. 265..

# SEM Micrograph Gallery



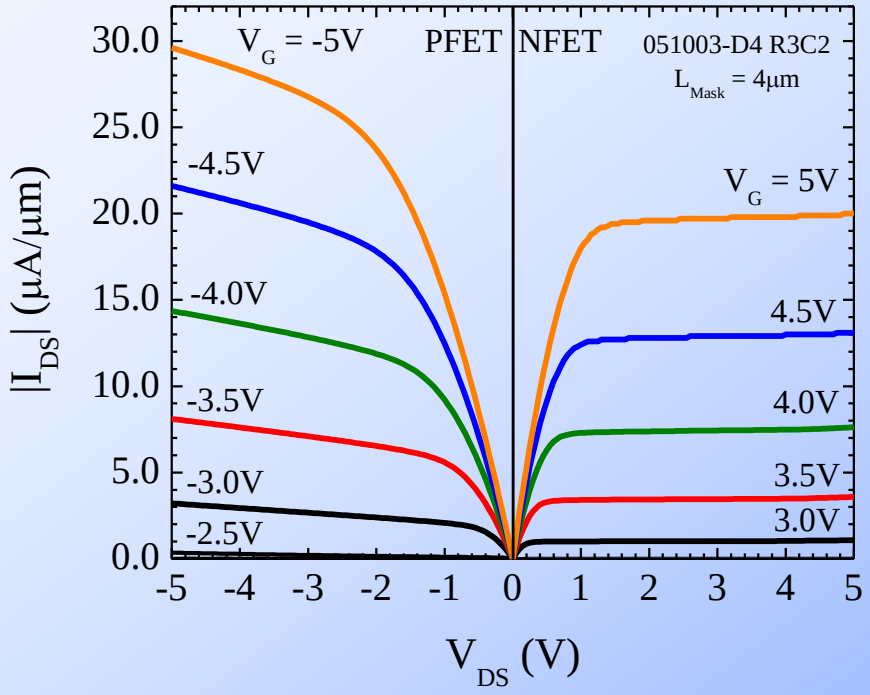



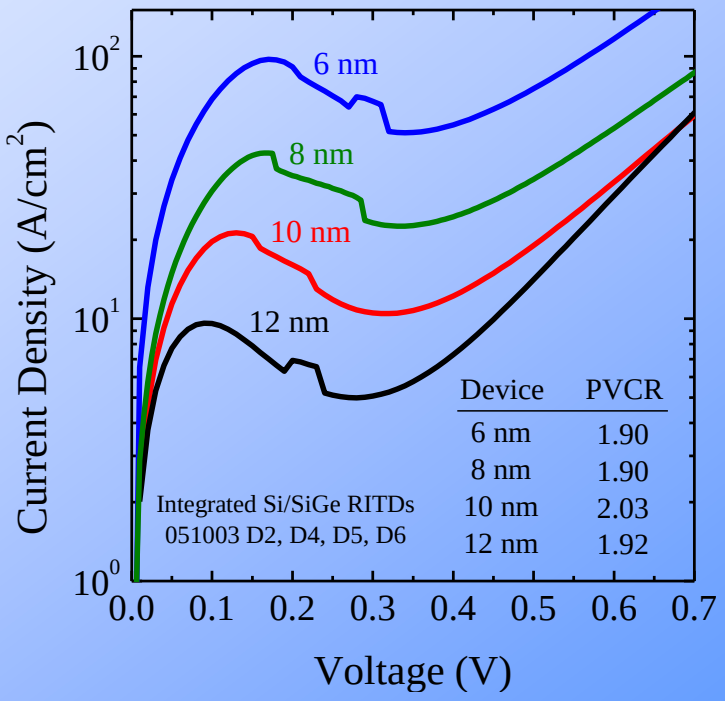




"NMOS/SiGe Resonant Interband Tunneling Diode Static Random Access Memory," S. Sudirgo, *et al.*, *Proceedings of the Device Research Conference (State College, PA, USA, 2006)*, p. 265..

# Integrated CMOS and Si/SiGe RITD

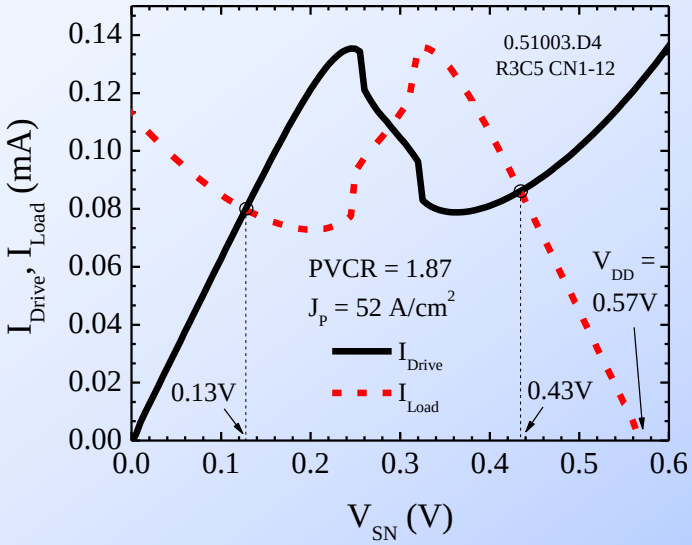


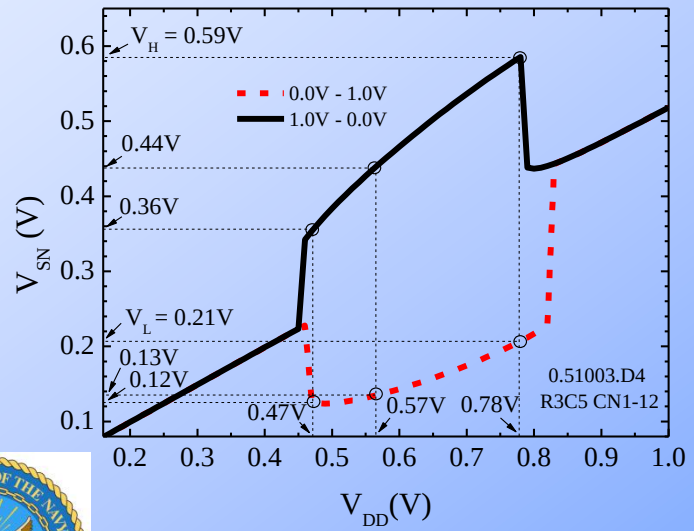




- Integrated NMOS exhibits a typical $V_T$ around 3.0 V.
- Integrated PMOS has $V_T$ around -2.65 V.
- Si/SiGe RITDs with various i-layer thicknesses: 6, 8, 10, and 12 nm.
- $J_P$ ranges from 10-100 A/cm$^2$, and PVCR up to 2.3.

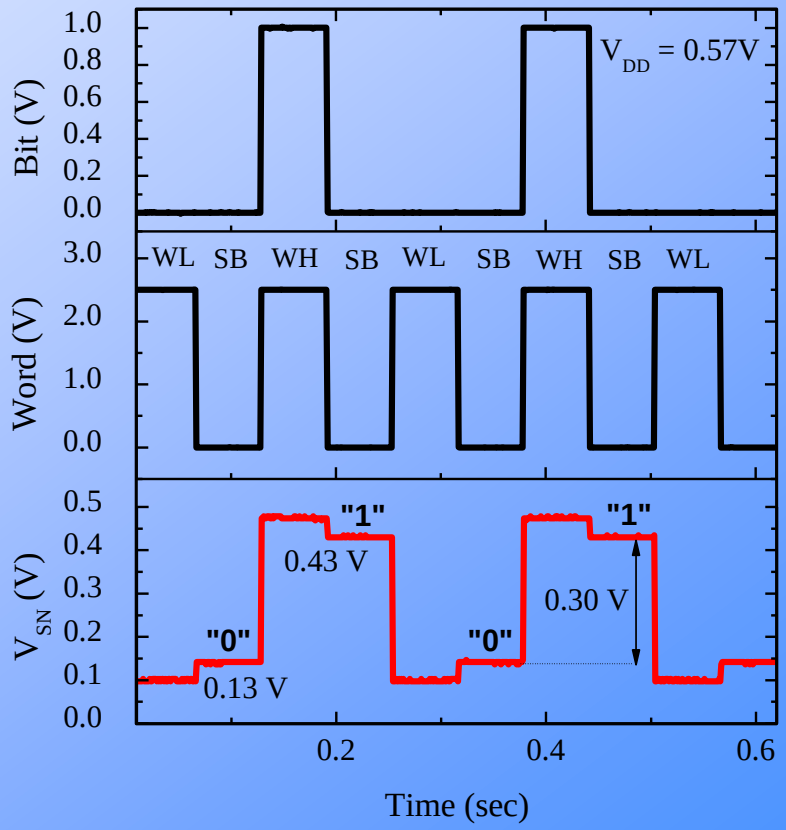
"NMOS/SiGe Resonant Interband Tunneling Diode Static Random Access Memory," S. Sudirgo, *et al.*, *Proceedings of the Device Research Conference (State College, PA, USA, 2006)*, p. 265..

# The First Integrated Si/SiGe TSRAM




- Low voltage operation down to **0.37 V** and %$V_{SWING}$ up to 53.5%.

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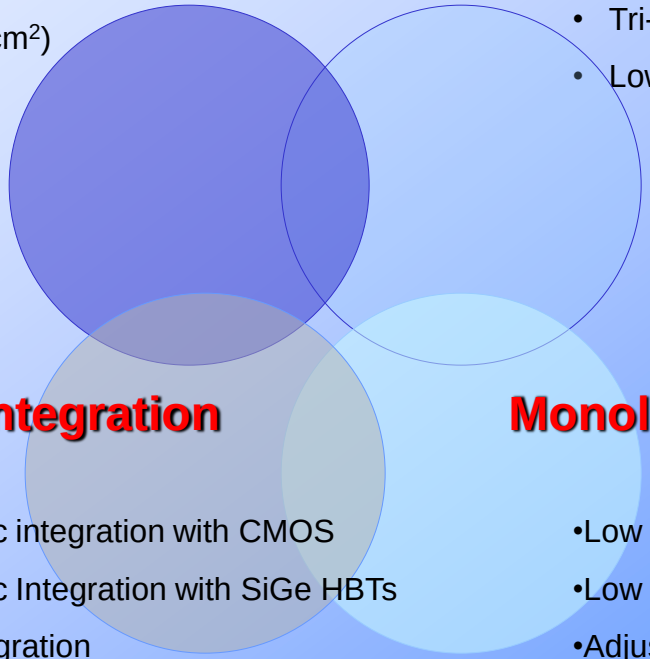
# Si-Based RITD Results Summary

## Device Optimization

- High PVCR (5.2)
- High PCD (≥ 218 kA/cm$^2$)
- Low PCD (≤ 20 mA/cm$^2$)

## Hybrid Circuit Prototyping

- Vertically stacked back-to-back RITDs for symmetric NDR
- Tri-state logic with vertically stacked RITDs
- Low voltage MOBILE latches (CMOS-RITD)



## Device Integration

- Monolithic integration with CMOS
- Monolithic Integration with SiGe HBTs
- CVD Integration

## Monolithic Circuits

- Low power/low voltage TSRAM
- Low power/low voltage MOBILE
- Adjustable PVCR (HBT-RITD)



National Science Foundation Celebrating 50 Years

# For Further Reading


- Paul R. Berger, Anisha Ramesh "Negative Differential Resistance Devices and Circuits" in *Comprehensive Semiconductor Science and Technology, Elsevier, Volume 5, Chapter 13, pp. 176–241 (2011).*
- A. C. Seabaugh, B. Brar, T. Broekaert, G. Frazier, and P. van der Wagt, "Resonant tunneling circuit technology: has it arrived?" *1997 GaAs IC Symposium*, pp. 119-122.
- A. Seabaugh and R. Lake, "Tunnel diodes," *Encyl. Appl. Phys.*, vol. 22, pp. 335-359 (1998).
- J.P. Sun, G.I. Haddad, P. Mazumder, J.N. Schulman, "Resonant tunneling diodes: Models and properties," *Proc. of IEEE*, vol. 86, pp. 641-661 (1998).
- P. Mazumder, S. Kulkarni, Bhattacharya M, J.P. Sun, G.I. Haddad, "Digital circuit applications of resonant tunneling devices, *Proc. IEEE*, vol. 86, pp. 664-686 (1998).
- J. P. A. van der Wagt, "Tunneling-Based SRAM," *Proc. of IEEE*, vol. 87, pp. 571-595 (1999).
- A. Seabaugh, B. Brar, T. Broekaert, F. Morris, P. van der Wagt, and G. Frazier, "Resonant-tunneling mixed-signal circuit technology," *Solid State Electronics*, vol. 43 pp. 1355-1365 (1999).
- K. Maezawa, T. Akeyoshi, and T. Mizutani, "Flexible and reduced-complexity logic circuits implemented with resonant tunneling transistors," *International Electron Devices Meeting Technical Digest*, pp. 415-418 (1993).