Growth temperature and dopant species effects on deep levels in Si grown by low temperature molecular beam epitaxy

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Deep-level transient spectroscopy measurements were performed in order to investigate the effects of substrate growth temperature and dopant species on deep levels in Si layers during low-temperature molecular beam epitaxial growth. The structures studied were n^+-p junctions using B doping for the p layer and p^+-n junctions using P doping for the n layer. While the density of hole traps H1 (0.38–0.41 eV) in the B-doped p layers showed a clear increase with decreasing growth temperature from 600 to 370 °C, the electron trap density was relatively constant. Interestingly, the minority carrier electron traps E1 (0.42–0.45 eV) and E2 (0.257 eV), found in the B-doped p layers, are similar to the majority carrier electron traps E11 (0.48 eV) and E22 (0.269 eV) observed in P-doped n layers grown at 600 °C. It is hypothesized that these dominating electron traps are associated with pure divacancy defects and are independent of the dopant species. [DOI: 10.1063/1.1569029]

I. INTRODUCTION

Epitaxially grown Si, combined with SiGe alloys, is now widely used to realize nanometer and heterostructure devices such as heterojunction bipolar transistors[1–4] and more recently resonant interband tunneling diodes (RITDs).[5,6] SiGe devices are attractive to device engineers due to their compatibility with existing silicon processes and superior performance. Device performance is adversely affected by the presence of defects, because their energy levels, generally located near the midband, act as generation-recombination centers that can quench carrier lifetime and degrade device performance. Molecular beam epitaxy (MBE) has proven to be a good tool for producing high-quality epitaxial layers under nonequilibrium growth conditions. Low-temperature molecular beam epitaxial (LT-MBE) growth has been especially useful as device sizes scale down to a few nanometers. The overall amount of dopant concentrations achievable using epitaxial growth techniques is limited due to segregation and out-diffusion which become more pronounced at higher growth temperatures that are closer to equilibrium conditions. LT-MBE is a far-from-equilibrium growth technique that minimizes segregation and diffusion. Thus, the investigation of defects in LT-MBE-grown material can help to optimize the growth process for optimal device performance. For example,[5,6] Si-based RITDs utilize δ doping via LT-MBE because it offers the opportunity to realize the high sheet carrier concentrations needed to achieve degeneracy ($\sim 10^{20}$ cm^{-3}) for interband tunnel diodes. However, LT-MBE concurrently creates defects that lead to an elevated valley current by tunneling through defects in the forbidden band gap. This leads to a suppressed peak-to-valley current ratio (PVCR) figure of merit for the RITD. The most dominant defects in LT-MBE growth are point defects created by the limited adatom mobility on the epitaxial surface leading to vacancies and by the strains and stresses stemming from different atomic radii between Si and the dopants chosen. Defect complexes can arise from a combination of these defects. An effective method to study the electrical characteristics of defects is through deep-level transient spectroscopy (DLTS).[7] The DLTS technique has been widely used in many forms since its inception in 1974, since it provides useful information on the deep levels, including activation enthalpy, capture cross section, and density of defects or impurities. The aim of this paper is to present the characteristics of deep levels in Si and their dependence on MBE growth temperature as well as dopant species and propose their possible identifications and origins by comparing their properties with those of previously identified deep levels in MBE-grown Si. For the purposes of this investigation, DLTS provides energy information about the deep levels within the forbidden band gap that will be useful in subsequent device analysis.

II. EXPERIMENT

Two different types of step junction diode (SJD), p^+-n and n^+-p, were studied in this work. A p^+-n SJD structure

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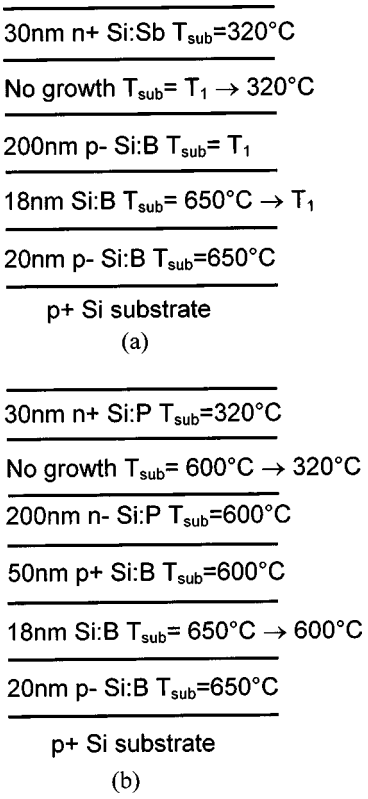

FIG. 1. Schematic diagrams of the basic structure of the Si:Sb,Si:B n^+-p (a) and Si:B,Si:P p^+-n (b) step junction diode structures. The key difference between the Si:Sb,Si:B n^+-p SJDs and the Si:B,Si:P p^+-n SJD is the substrate growth temperature (T_{sub}), which was varied during growth of the Si:B 200 nm p layer in the former. MBE growth temperatures (T_1) were set to 600, 500, 420, and 370 °C for samples A, B, C, and D, respectively. The growth rate was 1 Å/s for all layers.

was prepared as a reference sample to compare phosphorus dopant effects on defects, while four n^+-p SJD samples grown at different substrate growth temperatures were prepared to study the temperature effect on defects. Boron and antimony were used as the p-type and n-type dopants for the n^+-p SJD structures, and boron and phosphorus for the p^+-n SJD structures, respectively. Sb segregation[8] made it difficult to reliably control the low n-type doping levels needed in p^+-n SJD structures, so they were not included in this study. All samples were grown in a Vacuum Generators V-80 molecular beam epitaxy system using solid sources. The schematics of the basic structures for DLTS studies are shown in Figs. 1(a) and 1(b). For each n^+-p SJD structure, a 20 nm Si buffer layer was grown at 650 °C on the p^+-Si substrate. During the temperature adjustment to the intended substrate temperature, an 18 nm B-doped layer was grown. The B-doped p layer of 200 nm thickness was grown at the substrate growth temperature T_1, where T_1 was 370, 420, 500, or 600 °C, with nominal doping concentration of 1×10^{17} cm^{-3}. The thickness of the B-doped p layer was determined to be large enough so as to allow examination of the temperature effect upon deep-level defects and densities within the p layer. Subsequently, an Sb-doped n^+ layer of 30 nm thickness was grown. For the Sb-doped n^+ layer, the substrate temperature was decreased and fixed at 320 °C to reduce Sb segregation during Si MBE growth.[8] The Sb doping concentration was targeted to be 1×10^{18} cm^{-3}. All growth was carried out at a rate of 0.1 nm/s. For the p^+-n SJD structure, basically the growth sequence was the same as for the n^+-p SJD structures, except for using P as the dopant for the n and n^+ layers, and the differences are shown in Fig. 1(b).

Ti/Au Ohmic contacts (150 μm in diameter) were patterned photolithographically using lift-off and electron-beam evaporation while the backside Ohmic contacts of Ti/Au were made by deposition across the full surface. All diodes were formed by mesa etching and were approximately 300 nm deep. The wet etchant for mesa etching was $HF:H_2O:HNO_3$ (1:100:100) by volume ratio and etch rates varied between 100 and 150 nm/min.

The I-V characteristics were first checked at room temperature by an Agilent 4156C parameter analyzer. A Bio-Rad DL4600 system with a 100 mV test signal at 1 MHz was used to measure the C-V and DLTS characteristics. The C-V data, used to calculate the carrier profile, were taken in the temperature interval of 100 to 350 K to establish if the carrier concentration was a function of temperature.

The principle of DLTS measurement is based on the physics of thermal emission and capture by traps and the associated junction capacitance variations. It depends on the repetitive filling and emptying of traps by the use of a bias voltage applied to a junction. The processes of carrier emission and capture in deep-level traps can be briefly described as follows for a deep electron trap. Under quiescent reverse bias conditions, electron traps in a part of the junction depletion region are occupied. By the application of a forward or reduced reverse bias pulse, the traps in the junction depletion region can be partly or fully filled. On switching back to the quiescent reverse bias, the traps emit electrons to the conduction band with a characteristic time constant τ, resulting in a transient change of the depletion layer width and diode capacitance. The decay time constant in the capacitance transient curve is a function of sample temperature. Thus, the DLTS spectrum,[7] a continuous temperature versus capacitance signal, can be obtained.

In the DLTS measurements, the temperature was varied from 100 to 350 K. Typical bias voltages (V_b) of -4.5 to -1 V were used with filling pulse heights (V_f) of -0.5 to $+0.5$ V, a pulse width (W_f) of 0.1 or 1 ms, and a rate window of 50/s. In order to get the Arrehenius plots, rate windows were varied in the range of 4/s–1000/s and corresponding peak temperatures were recorded. The rate window is set by the DLTS instrumentation and determined by the two sampling periods at t_1 and t_2 between which the change in capacitance due to the capture/emission processes is measured. The rate window (i.e., $1/\tau$) is defined as $\ln(t_2/t_1)/(t_2-t_1)$. For a given rate window, there may be maxima (for majority traps) and minima (for minority traps) in the DLTS spectrum which are related to defects. Since the temperatures at which the minima and maxima occur are a function of the rate window, we can use Arrhenius analyses[7] to determine activation energies and capture cross sections for the traps (see below).

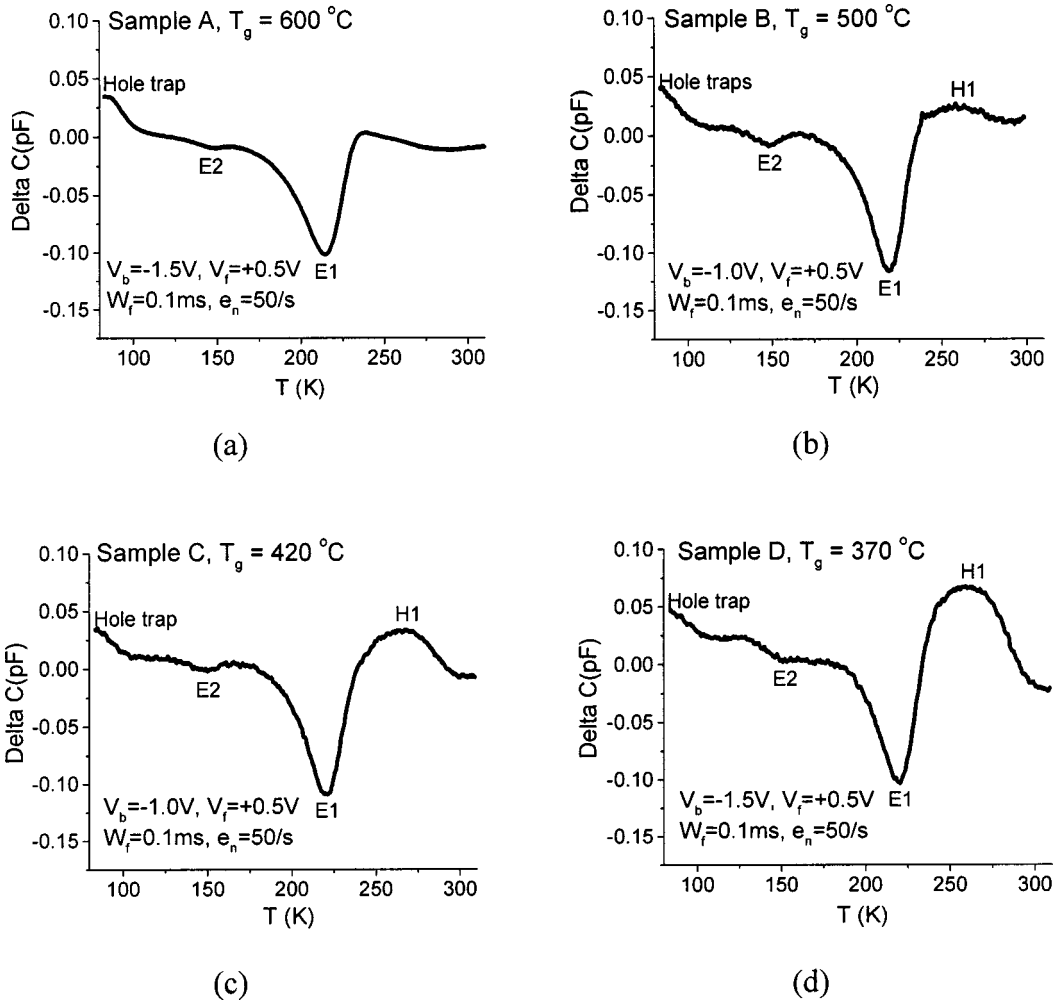

FIG. 2. The DLTS spectra of the MBE-grown Si:Sb,Si:B n^+-p step junction diodes (a)–(d) at substrate growth temperatures of 600, 500, 420, and 370 °C, respectively. T_g indicates growth temperature for each sample. The E1 $[E_C-(0.42-0.45)\ \text{eV}]$ and E2 $(E_C-0.257\ \text{eV})$ traps in the Si:B doped p layer were observed around 225 and 150 K, respectively. The H2 $[(0.38-0.41)\ \text{eV}-E_V]$ hole trap in the Si:B doped p layer was observed around 275 K and its density is strongly dependent on the substrate growth temperatures of the Si:B layer. The temperature variation in the DLTS measurements was set to vary from 100 to 350 K. Working voltages were set individually for each sample. Typical bias voltages (V_b) of -1.5 to -1 V were used with a filling pulse height (V_f) of 0.5 V, a pulse width (W_f) of 0.1 ms, and a rate window of 50/s.

III. RESULTS

A. As-grown n^+-p SJD structures at different substrate growth temperatures

Figures 2(a)–2(d), present typical DLTS spectra measured on n^+-p SJD samples A, B, C, and D, respectively. As described before, samples A, B, C, and D are distinguished by the substrate temperature during the growth of the lightly doped p layer of 600, 500, 420, or 370 °C, respectively. During the DLTS measurement, bias voltages were set such that minority carrier traps as well as majority carrier traps could be detected.

DLTS measurements for sample A, Fig. 2(a), which was grown at a growth temperature of 600 °C, revealed two clearly discernible traps labeled E1 and E2 at around 225 and 150 K, respectively, when a filling pulse was swept from -1.0 or -1.5 V to $+0.5$ V with a rate window of 50/s in the DLTS measurements. Since the E1 and E2 peaks appeared as negative peaks and these samples were n^+-p SJD structures, these traps are indicative of minority carrier (electron) traps. These electron traps were also found in the samples that were grown at 500, 420, and 370 °C, Figs. 2(b)–2(d). It is observed that the two peaks have little dependence on growth temperature, and show no shift in peak position for the four samples. In addition, the H1 peak was found in some of these samples. Since the H1 peak responds to majority carrier filling pulse and is positive, it represents the majority carrier (hole) traps observed in the B-doped p layers. The peak was not present in sample A, but was found in samples B, C, and D, over a broad range of measurement temperatures, 250–280 K, for the given rate window. It is also observed that the apparent intensity of the H1 peak increased as the growth temperature decreased.

The Arrhenius plots of T^2/e_n versus $1000/T$ for the major traps observed in MBE-grown n^+-p and p^+-n SJD structures are shown in Fig. 3, revealing the activation energies E_T and capture cross sections σ_n or σ_p, found in the samples studied. The Arrhenius plot is obtained from the emission time constant equation[9]

$$\frac{T^2}{e_n}=\frac{\exp[(E_C-E_T)/kT]}{\gamma_n\sigma_n}, \tag{1}$$

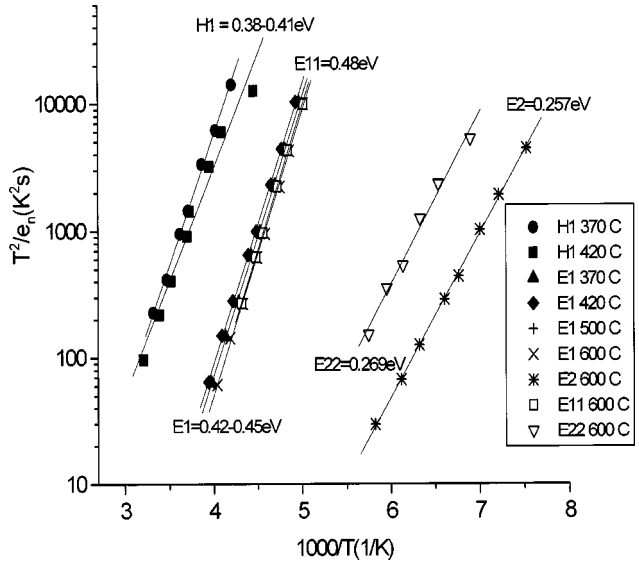

FIG. 3. Arrhenius plots of T^2/e_n vs $1000/T$ for the deep levels of E1, E2, E11, E22, and H1 observed in MBE-grown n^+-p and p^+-n SJDs. The Arrhenius plots are obtained from peak position temperatures and rate windows used. The trap E11 is estimated to be an association of dopants with vacancy defects, created by thermal stresses due to low growth temperature and the strains stemming from the differences of the atomic radii of Si and dopants. The trap E1 is estimated as a pure doubly negatively charged divacancy V-V $(-2/-)$ and E2 and E22 are estimated to be related to doubly negatively charged divacancies. The hole trap H1 is argued to be related to the impurities and/or vacancy defects. Energy levels obtained from the slopes of the plots and capture cross sections obtained from their intercepts of T^2/e_n at $1000/T=0$ are summarized in Table I.

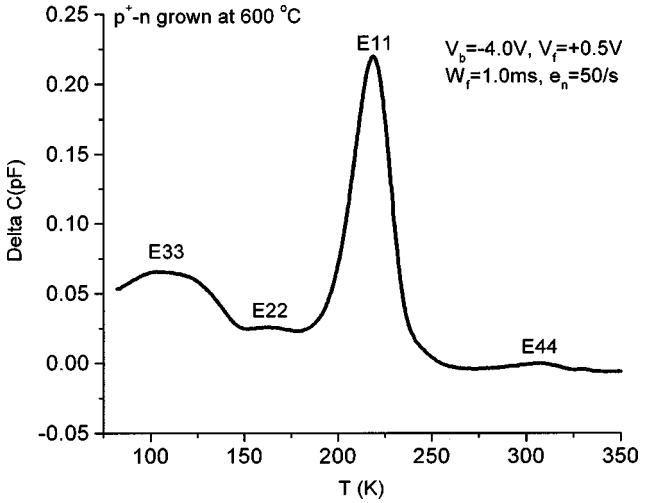

FIG. 4. The DLTS spectra of MBE-grown Si:B,Si:P p^+-n SJD grown at 600 °C. The E11 ($E_C-0.48$ eV) and E22 ($E_C-0.269$ eV) traps were observed and reveal the existence of E center+V-V $(0/-)$ complexes.

where γ_n is a modified coefficient $(v_{\text{th}}/T^{1/2})(N_C/T^{3/2})=3.25\times10^{21}(m_n/m_o)$ $\text{cm}^{-2}\,\text{s}^{-1}\,\text{K}^{-2}$, e_n is the rate window (s^{-1}), σ_n, σ_p are the electron and hole capture cross sections (cm^2), E_C-E_T is the energy needed for electron emission (eV), k is Boltzmann's constant $(8.617\times10^{-5}$ eV/K), m_n is the electron density-of-states effective mass,[10] and T is the experimental temperature during the DLTS measurement at which a specific defect registers a peak/valley in the DLTS spectrum for a given value of the rate window. For hole traps, (E_C-E_T) and the subscript n in Eq. (1) should be replaced by (E_T-E_V) and the subscript p. The coefficient $\gamma_{n,p}$ values[9] are 1.07×10^{21} $\text{cm}^{-2}\,\text{s}^{-1}\,\text{K}^{-2}$ for n-Si and 1.78×10^{21} $\text{cm}^{-2}\,\text{s}^{-1}\,\text{K}^{-2}$ for p-Si. The slope of the $\ln(T^2/e_{n,p})$ versus $1000/T$ Arrhenius plots determines the trap activation energy (E_C-E_T or E_T-E_V). The intercept of the Arrhenius plots at $1000/T=0$ is $\ln[1/(\gamma_n\sigma_n)]$ and determines the capture cross section (σ_n or σ_p) of the observed trap. The energy levels measured are E1 $[E_C-(0.42-0.45)$ eV], E2 ($E_C-0.257$ eV), and H1 $[(0.38-0.41)$ eV$-E_V]$. The corresponding capture cross sections are $\sigma_n(E_1)$ $(9.3\times10^{-15}-8.8\times10^{-14}$ $\text{cm}^2)$, $\sigma_n(E_2)$ $(1.1\times10^{-15}$ $\text{cm}^2)$, and $\sigma_p(H_1)$ $(1.9\times10^{-18}-1.1\times10^{-17}$ $\text{cm}^2)$.

B. As-grown p^+-n SJD sample grown at 600 °C of substrate temperature

Figure 4 shows the DLTS spectra for the p^+-n SJD sample grown at 600 °C. Like the n^+-p SJD structures, no other heat treatment has been added after growth was completed. During the measurement, the majority carrier pulse was set to have a V_b of -4.0 V and a V_f of $+0.5$. Several DLTS peaks, labeled E11, E22, E33, and E44, were observed. In this article, the discussion of the traps found in the p^+-n sample will be limited to E11 and E22. Since all the peaks are positive and this sample has a p^+-n SJD structure, those peaks are expected to indicate majority electron traps in the P-doped n layer. No minority carrier peak with concentration above 10^{13} cm^{-3} was revealed. A dominant DLTS peak, labeled E11, emerged as the measuring temperature reached 220 K. Despite the fact that this peak represents majority electron carrier traps in the lightly P-doped layer, the calculated activation energy level of $E_C-0.48$ eV and capture cross section $(8.4\times10^{-14}$ $\text{cm}^2)$ using Eq. (1) are similar to those of the E1 trap which was indicative of a minority carrier electron trap measured in the lightly B-doped p layer of the n^+-p SJD structures, Fig. 2. Another minor peak, E22, with an energy level of $E_C-0.269$ eV reveals a similar equivalency to the E2 trap, observed in the n^+-p SJD structure. The Arrhenius plots for E11 and E22 are shown in Fig. 3.

The observed characteristics of electron and hole traps, including activation energy levels, capture cross sections, and minimum trap densities, are listed in Table I. Since the trap level may not be completely depopulated or filled by the emission and capture of carriers during the DLTS measurement, the measured trap density is only a lower boundary. For the traps E1 and E2 in the n^+-p SJD structures, the trap density values listed in Table I may be further suppressed by the limited number of minority carriers injected from the n^+ layer, making the trap density difficult to estimate. Table I also compares the relative H1 trap density within the B-doped layer as a function of MBE growth temperature. According to the C-V measurements taken in the temperature interval of 100–350 K, for the given samples, the carrier density was not found to change as a function of temperature.

TABLE I. Activation energy (E_T), capture cross section ($\sigma_{n,p}$) as deduced from the Arrhenius plot, and its trap density, for the peaks E1, E2, E11, E22, and H1 found in the p^+-n and n^+-p diodes studied. The concentration of a trap is obtained directly from the capacitance change. The relationship for an electron trap in an n^+-p SJD is simply $N=2(\Delta C/C)(N_A-N_D)$. N is the trap concentration, ΔC is the capacitance change at $t=0$, C is the junction capacitance under quiescent reverse-biased conditions, and N_A-N_D is the net acceptor concentration on the p side of the junction where the trap is observed. The trap density is listed according to the Si:B p-layer growth temperature in the MBE system.

Major trap label	Sample (growth temperature) and trap density (cm^{-3})				Level (eV)	$\sigma_{n,p}$ (cm^2)	Assignment
	A (600 °C)	B (500 °C)	C (420 °C)	D (370 °C)			
E1	2.0×10^{15}	2.3×10^{15}	2.2×10^{15}	2.1×10^{15}	$E_C-(0.42-0.45)$	9.3×10^{-15}–8.8×10^{-14}	Strained $V(0/-)+\alpha$
E2	2.0×10^{14}	1.5×10^{14}	7.1×10^{13}	4.3×10^{13}	$E_C-(0.257)$	1.1×10^{-15}	$V(-2/-)$
E11	4.4×10^{15}				$E_C-(0.48)$	8.4×10^{-14}	$V-\mathrm{P}+V(0/-)$
E22	5.2×10^{14}				$E_C-(0.269)$	3.3×10^{-16}	$V(-2/-)$
H1		4.0×10^{14}	7.7×10^{14}	1.3×10^{15}	$(0.381-0.41)-E_V$	1.9×10^{-18}–1.1×10^{-17}	$B-V$ pair or impurities

IV. DISCUSSION

So far, many defect research groups have studied defects in silicon grown by chemical vapor deposition (CVD),[11,12] Czochralski (CZ) technique,[11] molecular-beam epitaxy,[13–18] or ion implantation.[19,20] But there remains some confusion in the literature about the role of dopants as a vacancy complex. Monakhov *et al.*[11] studied CVD-grown samples and CZ-grown bulk samples by irradiating with protons to intentionally induce defects in the samples, while Larsen and co-workers[13,14] used MBE-grown samples also irradiated by protons. Both samples had *n*-type Schottky diode structures and the DLTS technique was used to study defects in their work. In the work of Svensson *et al.*,[19,20] Si samples of *n* type grown by the CZ technique were ion implanted with low doses of various ions and defects were studied by DLTS. From the work above, the commonly presented result was the existence of two specific deep-level defects thought to be related to divacancy defects.[21,22] Previous work has determined that a singly negatively charged divacancy V-V $(0/-)$ is associated with a trap level located around 0.42 eV below the conduction band edge and a doubly negatively charged divacancy V-V $(-2/-)$ is associated with a trap level located around 0.25 eV below the conduction band edge.[21] Two electron traps that have similar DLTS characteristics, as compared by their activation enthalpy and capture cross section, were detected in the MBE as-grown samples studied here, regardless of which dopants were used.

Vacancy-related defects during LT-MBE have been reported.[15–17] However, since different analytical techniques [optically detected magnetic resonance[16] and positron annihilation spectroscopy[17]] were adopted to detect the defects, the vacancy defects were not represented by their activation enthalpy and capture cross section which is often more useful to the study of electronic materials for device applications. In this study, the electrical traps of MBE-grown Si were studied by the DLTS technique.

Based upon the similar electrical signatures, the E1 and E2 traps found in n^+-p diode samples grown at different temperatures, Figs. 2(a)–2(d), are tentatively assigned to V-V $(0/-)$ related complexes and V-V $(-2/-)$, respectively. In addition, the E11 and E22 traps found in p^+-n SJD samples grown at 600 °C, Fig. 3, also display similar characteristics to a singly negatively charged V-V $(-/0)$ and a doubly negatively charged V-V $(-2/-)$, respectively. Another particular point is that, unlike previous work in which proton irradiation[11–14] or ion implantation[19,20] was used to create intrinsic defects, low MBE growth temperatures can cause the formation of well-known divacancy defects in as-grown samples.[15–17]

Figures 2(a)–2(d) show clearly that one positive peak, H1, indicating majority hole traps, is strongly dependent on the growth temperature employed. The H1 peak increases as the growth temperature decreases and reaches its highest level at the lowest growth temperature of 370 °C. The E1 and E2 peaks, however, appear invariant to the growth temperature utilized. Two possibilities can be suggested to explain the independent electron trap peaks with respect to growth temperature. (i) Since the peaks respond to minority electron carrier emission injected with a forward injection pulse, only the lower limit of the trap concentrations for the E1 and E2 levels was detected. Therefore, the real E1 and E2 trap concentrations may exhibit a temperature dependence like H1, but be masked. (ii) The other possibility is that the highest growth temperature (600 °C) among the samples is still low enough to saturate the defect formation rate. Thus, even at reduced growth temperatures, the amount of defects in all the samples is the same, provided that the other growth conditions are identical. But this is not a likely scenario. More studies will be performed with p^+-n SJDs grown at different growth temperatures, since the majority carrier trap concentration of E11 and E22 in a p^+-n diode (Fig. 4) is not limited by the applied pulse.

Many previous studies have mentioned the possibility of a dopant effect on the creation of singly negatively charged divacancy V $(0/-)$ complexes. Larsen and co-workers[13,14] used Sb as the *n*-type dopant for the MBE-grown p^+-n diode samples, where the observed $E_C-0.434$ eV trap level using DLTS was tentatively assigned as an Sb-V (E center) $+V$-V $(0/-)$; while Monakov *et al.*[11] studied P-doped p^+-n diode samples grown by chemical vapor deposition and found a trap at $E_C-0.44$ eV using DLTS and tentatively assigned it as a vacancy donor pair (E center) overlapped with V-V $(0/-)$. In our work, the existence of the E center + divacancy complexes is well proved. E11 traps are located around $E_C-0.48$ eV. These traps display similar characteristics to a divacancy V-V $(0/-)+$E center complex because

the sample measured is a P-doped p^+-n diode and the activation enthalpy energy for the E11 inside the forbidden band gap deviates slightly from the pure divacancy, V-V $(0/-)$, position. However, the E1 traps found in B-doped n^+-p SJD samples are located at $E_C-(0.42-0.45)$ eV. Thus, the possible defect nature of the E1 traps is closest to pure divacancy defects. In general, the mechanism for E center creation is explained by the fact that doping with P results in a contraction of the silicon lattice[23] due to different atomic radii of P in a Si matrix. However, because doping with Sb conversely causes an expansion of the silicon lattice, it is not unexpected that both P and Sb can play the same role as the origin of the divacancy complexes with an E center that were measured.

The mechanism for the creation of divacancy defects assigned to the E1 and E2 traps observed in the MBE as-grown samples is suggested to be as follows. In Si implanted with heavy ions,[19,20] the creation of V-V $(0/-)$ and V-V $(-2/-)$ is explained by the presence of a local lattice distortion and strain in the damaged peak region. The local distortion and strain formed during ion implantation create enough unstable high energy to cause Jahn-Teller distortion[24] for divacancy creation. In the MBE-grown layers studied, the local lattice distortion can be due to electrically inactive intrinsic defects that can form during MBE growth. Since MBE is a nonequilibrium growth technique, even at 600 °C, the Si adatom surface mobility is kinetically limited and creates vacancies and interstitials during growth. However, it should be noted that doubly and singly negatively charged divacancies, themselves, are not strongly affected by dopants, although dopants can cause defect complexes by combining with existing divacancy defects. This explanation is well supported in this work.

In the studied boron-doped n^+-p diodes, not only were H1 traps found that are strongly temperature dependent, but also E1 and E2 traps are detected in all samples despite different growth temperatures, Figs. 2(a)–2(d). There are three possible suggestions to explain this.

(i) That growth at 600 °C is high enough for B to be fully electrically activated, but that at reduced growth temperatures (below 420 °C), boron's adatom mobility becomes limited and it creates electrically inactive dopant-related defect complexes that act as hole traps, shown in Fig. 2. The lower the growth temperature, the more boron-related defects are expected to be created. However, boron acts more as an interstitial diffuser rather than a segregator due to the small atomic radius of B. Thus, B should be uniformly distributed throughout the film. Also, more important, previous work has shown that B is fully activated, even at substrate temperatures as low as 320 °C, so this is not likely.

(ii) That past investigations of samples grown by the same MBE system were monitored by secondary ion mass spectroscopy (with elemental detection limits in Si) and were observed to contain trace amounts of Cr ($<10^{15}$ cm^{-3}), Al ($<10^{15}$ cm^{-3}) and Ta ($<10^{16}$ cm^{-3}).[25] According to Chen and Milnes,[26] Cr, Al, and Ta can be placed, respectively, at the energy levels of $0.11\,\text{eV}-E_V$, $(0.392, 0.312,$ or $0.214\,\text{eV})-E_V$, and $0.4\,\text{eV}-E_V$ all acting as hole traps. Therefore, these impurity-related complexes can be another candidate for the measured H1 trap. Since Cr, Al, and Ta are known to segregate as the substrate temperature increases, the observed temperature dependence of the H1 trap is a likely scenario.

(iii) That Fe and Cu impurities,[9] even though they have not been monitored with concentrations above the 10^{13} cm^{-1} SIMS detection limit in past work,[25] have energy signatures (enthalpy, cross section, and characteristic temperature at the same rate window) closest to those of the H1 trap; these impurities also appear to be H1 traps.

V. CONCLUSION

In conclusion, DLTS measurements were performed on n^+-p SJDs using B doping for the lightly doped p layer and p^+-n SJDs using P doping for the lightly doped n layer to investigate the substrate growth temperature effects on deep levels during MBE growth as well as effects of dopant species. This work reveals that in MBE as-grown Si, two vacancy-related fundamental defects in the Si material, doubly and singly negatively charged divacancies, are created at growth temperatures at or below 600 °C without intentionally introducing defects and/or impurities. In addition, the dopant species do not affect the creation of divacancies. Instead, n-type dopants may play an important role in creating divacancy complexes acting as an E center. In this DLTS work, another major peak, H1, which is indicative of hole traps, is observed in Si:Sb, and Si:B n^+-p samples grown below 600 °C. Hole traps show strong growth temperature dependence. It is argued that the origin of hole traps is related to impurities in the MBE system used and/or vacancy defects, and their temperature dependence is due to impurity segregation during growth.

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