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Monolithically integrated Si/SiGe resonant interband tunnel diode/CMOS demonstrating low voltage MOBILE operation

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Abstract

The first demonstration of the monolithic integration of CMOS and Si/SiGe resonant interband tunnel diodes (RITD) with negative differential resistance (NDR) is reported in this paper. The Si/SiGe RITDs exhibited a peak-to-valley current ratio (PVCR) up to 2.8 and peak current density (J_p) of 0.26 kA/cm^2 at room temperature. This study focused on the utilization of a pair of tunnel diodes connected in series to form a latch. Employing a FET to supply current into the latch, a RITD/NMOS monostable–bistable transition logic element (MOBILE) was realized. The latch exhibited a voltage swing of 84% at an applied supply voltage of 0.5 V. This logic element enables low voltage operation for high density circuit design of embedded memory.

1. Introduction

Resonant tunnel diode-field effect transistors (RTD-FET) circuits in III–V materials have demonstrated reduced power consumption in circuits such as ultra-low power III–V compound memory using tunneling-SRAM [1], as well as improved speed for logic applications such as multiplexers [2] and analog-to-digital converters [3]. Tunneling diode based SRAM (T-SRAM) uses a tunnel diode pair to store a bit of data, and takes the refresh-free and fast write speed of SRAM and puts it into the footprint of a DRAM cell by reducing component count (1 transistor and 2TDs versus 6 transistors in conventional CMOS) [1]. An InP-based high electron mobility transistors (HEMT)/RTD comparator circuit, for example, had a significantly smaller component count, taking 1/6 the area, while outperforming the HEMT-only circuit in speed and power consumption [3]. Furthermore, the integration of RTDs with FETs, has led to improved mixed-signal circuitry and is currently being sought to produce THz signal generation and detection.

The development of an epitaxially grown SiGe tunnel diode was realized in 1998 [4]. In essence, there are five key features of the original structure of the Si/SiGe resonant interband tunnel diode (RITD) design: (i) an intrinsic tunneling barrier called spacer (ii) δ-doped injectors, (iii) off-set of the δ-doping planes from the heterojunctions interfaces, (iv) low temperature molecular beam epitaxial growth (LT-MBE), and (v) post-growth rapid thermal annealing (RTA) for dopant activation and point defect reduction. The tunnel barrier in these structures nominally is defined by the placement of δ-doping planes; variations to the intrinsic layer between these planes allow the scaling of current density [5]. Fig. 1 shows the RITD structure used as the control growth template in this study. Discrete devices with this structure typically exhibit a peak-to-valley current ratio (PVCR) of 3.6 and peak current density (J_p) of

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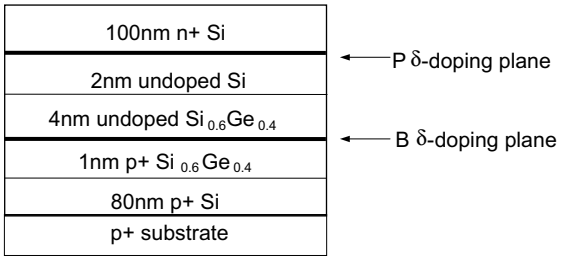

Fig. 1. Schematic diagram of the Si/SiGe RITD [6].

0.3 kA/cm^2 [6]. Similar structures have been replicated in different studies that resulted in PVCR reported up to 6.0 [7], and J_p as high as 151 kA/cm^2 [8].

2. Integration strategy and fabrication

A comparatively relaxed CMOS process was used for integration feasibility studies. The process included (i) twin-well technology, (ii) localized oxidation on silicon (LOCOS) for isolation, (iii) 37 nm SiO_2 gate dielectric, (iv) heavily n-doped polysilicon gate, (v) self-aligned source and drain formation, and (vi) Al(1%Si) for contact and metallization [9].

Based on thermal budget considerations, the integration of the RITDs was carried out after all CMOS high thermal front-end steps up to the source/drain formation, but prior to metallization steps. RITD structures were grown on p+ implanted regions created for the source/drain of the PMOS through openings in a 300 nm thick chemical vapor deposition (CVD) oxide (Fig. 2). During LT-MBE growth, the substrate temperature was varied from 650 to 320 °C to minimize dopant diffusion and segregation. The devices were annealed using rapid thermal annealing (RTA) at 825 °C for 1 min to reduce point defects formed during the low temperature MBE growth process. The tunnel diodes were patterned using plasma etch in SF_6/He gas mixture. Contact cut openings were defined simultaneously for both CMOS and RITD devices using conventional photolithography technique. Via sputtering, a 300 nm thick layer of Al(1%Si) was deposited onto the wafers for contact metallization. After patterning and etching the metal layer, the integrated devices were sintered at 420 °C for 20 min.

3. Electrical characteristics

Figs. 3 and 4 show the electrical characteristics of each of the discrete devices in the monolithically integrated CMOS/RITD circuit. The measured I_D–V_{DS} characteristics of the NMOS and PMOS FETs, both with L_{eff} of 1.5 μm and width of 32 μm, are shown in Fig. 3. The NMOS is operating in depletion mode, which has a threshold voltage (V_{th}) of −0.4 V. The V_{th} of PMOS is slightly higher than the designed value at −2.0 volts. The variations in the V_{th} of the CMOS were attributed to the inaccuracy of dose counter on the ion implanter. A more in depth performance analysis, design, and simulation of the CMOS devices is given in Ref. [9].

A 25×25 μm^2 Si/SiGe RITD grown in the same die exhibits negative differential resistance (NDR) behavior with a PVCR of 2.8 and a J_p of 0.26 kA/cm^2 as shown in Fig. 4. Compared to Jin's discrete RITDs [7], a slight increase in series resistance as indicated by higher peak voltage of the integrated tunnel diodes is observed. This increase is attributed to higher contact resistance, in which Al(1%Si) is used in contrast to PtSi on Jin's devices. Unlike the discrete devices that utilized backside contact to access the p^+ side of the diode, the integrated RITD uses planar contact, resulting in current crowding that leads to higher series resistance. The integrated tunnel diode also shows a slight reduction in PVCR due to the effect of patterned growth and the propagation of implant damage. Detailed studies on the process integration effects on RITD device performance are reported elsewhere [10]. The smallest diode fabricated in this study was a 16×16 μm^2 RITD with PVCR of 2.2 and J_p of 0.25 kA/cm^2.

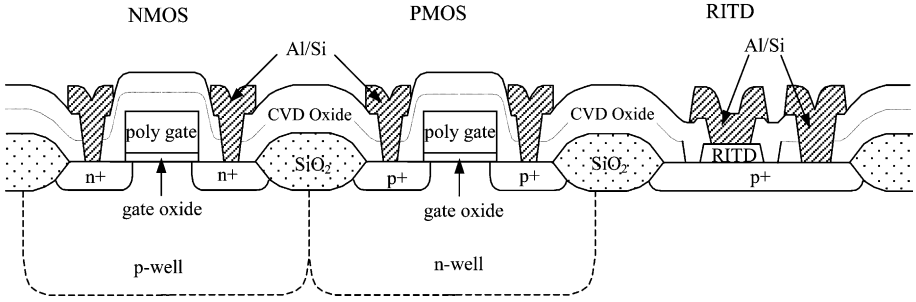

Fig. 2. Schematic diagram of the monolithically integrated CMOS and Si/SiGe RITD.

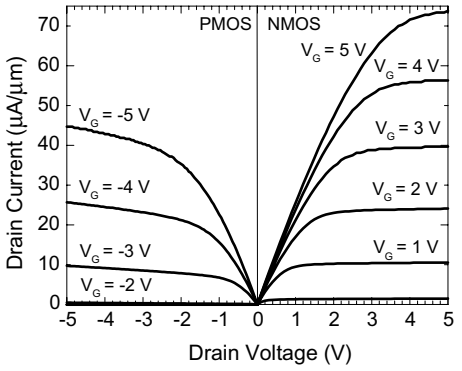

Fig. 3. I_D–V_{DS} characteristics of NMOS and PMOS, both with a $L_{eff} = 1.5$ μm.

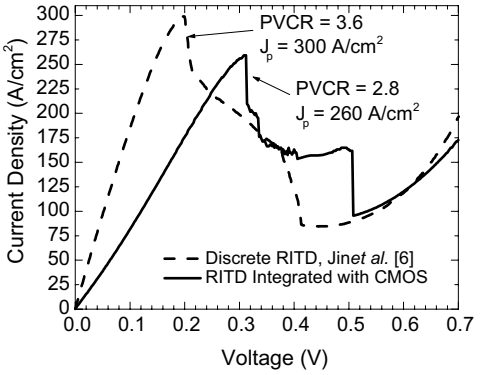

Fig. 4. *I–V* characteristics of the first integrated 25×25 μm^2 patterned growth RITD. The RITD is in the same die as the CMOS devices plotted in Fig. 3.

4. Si/SiGe RITD/CMOS logic element

A common element in RITD-FET circuit designs is a tunnel diode latch [11]. A latch consists of a pair of tunnel diodes in series as illustrated in the inset of Fig. 5. RITD1 and RITD2 functioned as the load and driver, respectively. Fig. 5 shows the *I–V* characteristics of two 25×25 μm^2 RITDs in series. The first RITD has a PVCR of 2.8 and the second 2.6 with J_p of 0.26 kA/cm^2 for both devices.

A monostable–bistable transition logic element (MOBILE) latch was realized by incorporating a FET into the middle node, known as the sense node as shown in the inset of Fig. 6. An FET operating in the saturation region exhibits nearly infinite resistance and acts as current source that is used to charge or discharge the RITD latch. In order to match the operating current of the RITDs used in the latch, an NMOS transistor with L_{eff} of 1.5 μm and width of 32 μm was chosen. With gate bias (V_G) and drain-to-source bias (V_{DS}) of the NMOS both set at 3.5 V, the drain current (I_D) flows at 1.54 mA,

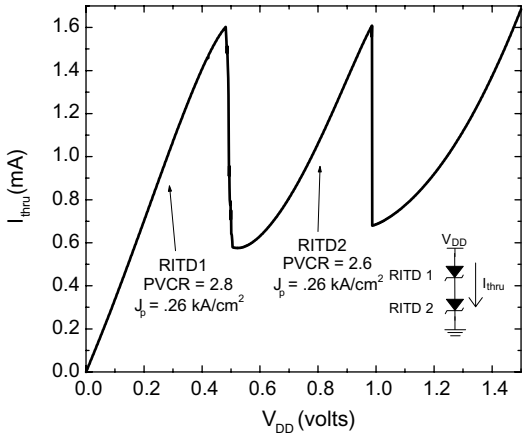

Fig. 5. *I–V* characteristics of two 25×25 μm^2 RITDs in series with PVCR of 2.8 and 2.6, and J_p of 0.26 kA/cm^2.

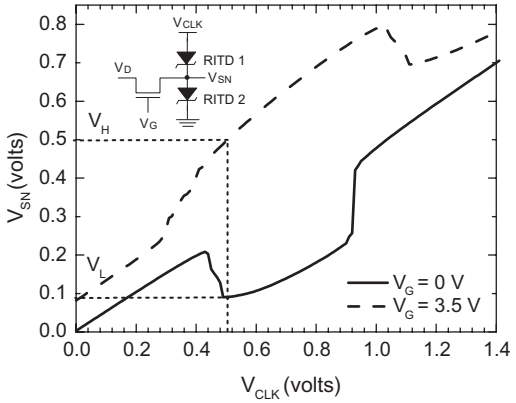

Fig. 6. Voltage at sense node vs. applied clock voltage of a NMOS-RITDs MOBILE latch with 84% voltage swing of the applied V_{CLK} at 0.5 V.

which is slightly less than the peak current of the RITDs at 1.6 mA. It should be noted that while this paper explicitly focuses on adjusting the NMOS to the tunnel diodes characteristics, the current density of the Si/SiGe RITD can easily be modified to match the FET characteristics by altering the intrinsic spacer layer thickness [4,8].

Fig. 6 shows the voltage measured at the sense node (V_{SN}) as a function of applied clock voltage (V_{CLK}) when the NMOS is in the off-state (i.e. $V_G = 0$ V) and on-state (i.e. $V_G = 3.5$ V). The circuit latches to two distinct voltage values at the sense node for a given V_{CLK}, demonstrating bistable operation. A figure-of-merit to characterize this type of latch is known as percentage voltage swing ($\%V_{swing}$), which is the ratio between the voltage difference of logic high and low ($V_H - V_L$), and the applied clock voltage. For the applied V_{CLK} of 0.5 V, the RITD-NMOS MOBILE latch using integrated

devices shows a high voltage swing up to 84%. This is a very significant result since the best reported voltage swing on Si-based RITD MOBILE latch was 81% using an external source of current source and no integrated transistor [12].

5. Conclusions

Si/SiGe RITDs grown by MBE have been monolithically integrated with CMOS. The integrated tunnel diodes results in a PVCR of 2.8 at room temperature with peak-current density of 0.26 kA/cm^2. A MOBILE logic gate that utilized a pair of RITDs connected in series and a NMOS as current injector into the sense node has also been demonstrated. The RITD/NMOS MOBILE latch exhibits a high voltage swing up to 84% at low operating applied clock voltage of 0.5 V. This logic element enables low voltage operation of digital circuit design for high density storage.

Acknowledgements

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References

[1] van der Wagt JP, Seabaugh AC, Beam E. RTD/HFET low standby power SRAM gain cell. IEEE Electron Dev Lett 1998;19:7–9.

[2] Chan HL, Mohan S, Mazumder P, Haddad GI. Compact multiple-valued multiplexers using negative differential resistance devices. IEEE J Solid-State Circ 1996;31:1151–6.

[3] Broekaert T, Brar B, van der Wagt JP, Seabaugh A, Morris F, Moise T, et al. A monolithic 4-bit 2-gsps resonant tunneling analog-to-digital converter. IEEE J Solid-State Circ 1998;33:1342–9.

[4] Rommel SL, Dillon TE, Dashiell MW, Feng H, Kolodzey J, Berger PR, et al. Room temperature operation of epitaxially grown Si/$Si_{0.5}Ge_{0.5}$/Si resonant interband tunneling diodes. Appl Phys Lett 1998;73:2191–3.

[5] Rommel SL, Jin N, Dillon TE, Di Giacomo SJ, Banyai J, Cord BM, et al. Development of δ B/i-Si/δ Sb and δ B/i-Si/δ Sb/i-Si/δ B Resonant Interband Tunnel Diodes for Integrated Circuit Applications, 58th Device Research Conf., June 2000. p. 159–160.

[6] Jin N, Chung SY, Rice AT, Berger PR, Yu R, Thompson PE, et al. Diffusion barrier cladding in Si/SiGe resonant interband tunneling diodes and their patterned growth on PMOS source/drain regions. IEEE Trans Electron Dev 2003;50:1876–84.

[7] Eberl K, Duschl R, Schmidt OG, Denker U, Haug R. Si-Based resonant inter- and intraband tunneling diodes. J Cryst Growth 2001;227–228:770–6.

[8] Jin N, Chung SY, Rice AT, Berger PR, Yu R, Thompson PE, et al. 151 kA/cm^2 peak current densities in Si/SiGe resonant interband tunneling diodes for high power mixed-signal applications. App Phys Lett 2003;83:3308–10.

[9] Hirschman KD, Hebding J, Saxer R, Tabakman K. Semiconductor process and device Modeling. A graduate course/undergraduate elective in microelectronic engineering at RIT. In: Proc. of the Fifteenth Biennial University/Government/Industry Microelectronics Symp., 2003. p. 138–146.

[10] Sudirgo S, Curanovic B, Rommel SL, Hirschman KD, Kurinec SK, Jin N, et al. Challenges in integration of resonant interband tunnel Devices with CMOS. In: Proc. of the Fifteenth Biennial University/Government/Industry Microelectronics Symp. 2003. p. 275–278.

[11] Goto E, Murata K, Nakasawa K, Moto-Oka T, Matsuoka Y, Ishibashi Y, et al. Esaki diode high speed logical circuits. Mater Sci Eng B 1995:259–62.

[12] Auer U, Prost W, Agethen M, Tegude F-J, Duschl R, Eberl K. Low-voltage MOBILE logic module based on Si/SiGe interband tunnelling diodes. IEEE Electron Dev Lett 2001;22:215–7.