Tri-State Logic Using Vertically Integrated Si–SiGe Resonant Interband Tunneling Diodes With Double NDR

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***Abstract*—A vertically integrated npnp Si-based resonant interband tunneling diode (RITD) pair is realized with low-temperature molecular beam epitaxy by stacking two RITDs with a connecting backward diode between them. The current–voltage characteristics of the vertically integrated RITD pair demonstrates two sequential negative differential resistance regions in the forward-biasing condition. Tri-state logic is demonstrated by using the vertically integrated RITDs as the drive and an off-chip resistor as the load.**

***Index Terms*—Molecular beam epitaxy (MBE), multivalued logic, negative differential resistance (NDR), resonant interband tunneling diodes (RITD), silicon, silicon germanium.**

I. Introduction

As ultra-large-scale-integration (ULSI) moves toward deep-submicrometer technology ($\leq$90 nm), chip area, signal delay, and dynamic power dissipation are becoming dominated by interconnections rather than by the intrinsic device speed [1]. Compared to conventional binary logic, multiple valued logic (MVL) has a tremendous potential to overcome the limitations associated with interconnection complexity, because more information can be conveyed by multivalued signals than binary logic, so that fewer interconnects will be required to transmit information [2]. The success of the MVL approach is greatly dependent on the availability of devices which are suitable for MVL operations. Due to the bi-state nature of conventional transistors, the resulting MVL basic building blocks are relatively complex, which would unfavorably increase device count and offset the advantages of MVL. With the unique folded current-voltage (*I–V*) characteristics, multiple-peaked tunneling diodes are ideal for MVL implementation, because multilevel quantization and switching between several operational points can be very easily obtained. This is clearly evident when a resistive load line or transistor load is placed across multiple negative differential resistance (NDR) peaks.

Since MVL circuitry was demonstrated by using a multiple-peaked resonant tunneling diode (RTD) for the first time [3], many RTD-MVL circuits, such as multivalued memory cell, analog-to-digital converters (ADC), counter, decoder, and programmable logic arrays (PLAs) (see [4] and references therein) with greatly reduced complexity and component count have been reported. Ultrahigh circuit speed is also achievable due to the picosecond switching speed of multiple-peaked RTDs. However, all these above mentioned multiple-peaked RTDs utilize III-V semiconductors, which are not compatible with main stream Si CMOS technology. Only recently have Si-based tunnel diodes been developed that can be epitaxially grown and readily integrated monolithically like their III-V counterparts.

The development of Si-based resonant interband tunneling diodes (RITD) [5]–[7] and successes in their monolithic integration [7]–[9] with CMOS transistors [7] and Si–SiGe heterojunction bipolar transistor (HBT) technology [8] paves the way for highly functional Si-based tunnel diode-transistor circuits. To solve the polarity mismatch between the npn SiGe HBT and the n-on-p RITD vertically above, a reversed-biased Si-backward diode was inserted between the RITD and HBT that effectively serially connects the two vertically stacked devices [8]. In this letter, we report the first double-peaked Si-based tunneling structure, using two vertically stacked RITDs with an Si-based backward diode connecting the top and bottom RITDs, which is suitable for MVL operations. A tri-state logic circuit was then demonstrated using the RITD stack with an external resistor.

II. Experimental

The generic structure of a single Si-based RITD is shown in Fig. 1(a). The spacer layer sandwiched between the two δ-doping spikes is composed of two layers, an intrinsic Si layer of thickness L_1, which is below the P δ-doping layer and an intrinsic $Si_{0.6}Ge_{0.4}$ layer of thickness L_2 that is above the B δ-doping layer. Note that there are thin $Si_{0.6}Ge_{0.4}$ cladding layers surrounding the B δ-doping layer. Strained SiGe has been shown to suppress B diffusion [10]. Thin strained SiGe

Manuscript received March 1, 2004; revised June 7, 2004. This work was supported in part by the National Science Foundation under Grants ECS-0196208, ECS-0196054, and ECS-0323657, in part by the Office of Naval Research, and in part by The Ohio State University Center for Materials Research. The review of this paper was arranged by Editor E. Sangiorgi.

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Digital Object Identifier 10.1109/LED.2004.833845

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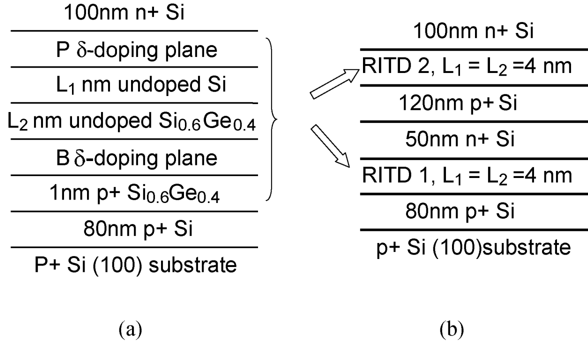

Fig. 1. (a) Schematic of the generic Si-based RITD design used in this study. (b) Schematic of the vertically stacked RITD pair using an npnp configuration of two generic Si-based RITDs connected serially by a backward diode.

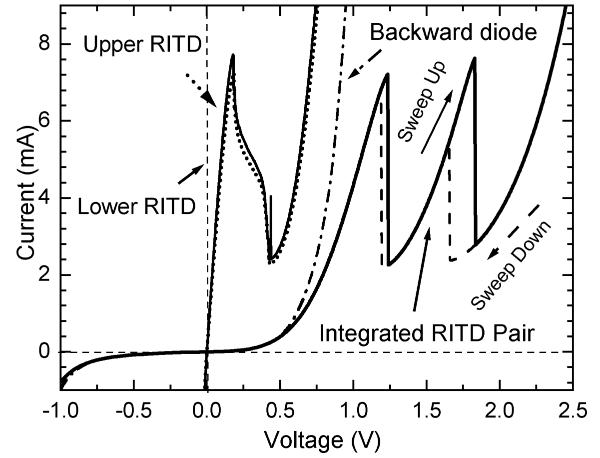

Fig. 2. Measured room-temperature *I–V* characteristics of a 50 μm-diameter vertically stacked RITD pair, "discrete" upper and lower RITDs, and backward diode all annealed at 825 °C for 1 min.

layers are effective in suppressing B outdiffusion in δ-doped structures, so that the sharp B peak can be maintained during post-growth annealing [7]. As a result, RITDs with SiGe cladding can be post-growth annealed at higher temperatures to more effectively remove point defects created within the spacer during LT-MBE. Fewer point defects reduce contributions to the valley current, which leads to a higher peak-to-valley current ratio (PVCR) [7].

Fig. 1(b) shows the structure of the reported vertically stacked RITDs with an npnp configuration. The top RITD and bottom RITD have the same spacer configuration with L_1 of 4 nm and L_2 of 4 nm in order to obtain similar PVCR and peak current density (J_p) values. Note there is a backward diode between the top diode and bottom RITD, which will be reverse biased during active operation, that effectively connects the top RITD and bottom RITD as a small series resistance, under the forward biasing condition for the vertically stacked RITDs.

The entire vertically integrated RITD pair was grown by molecular beam epitaxy (MBE) using elemental Si and Ge in electron-beam sources on 75-mm B-doped $(\rho = 0.015 - 0.04\ \Omega \cdot \text{cm})$ Si (100) wafers. The doping levels for both n^+ and p^+ layers are $5 \times 10^{19}\ \text{cm}^{-3}$, while both the B and P δ-doping sheet concentrations were maintained at $1 \times 10^{14}\ \text{cm}^{-2}$. Prior to device fabrication, portions of the grown wafers were rapid thermal annealed (RTA) using a forming gas ambient (N_2/H_2) in a Modular Process Technology corporation RTP-600S furnace at various temperatures for 1 min. Ti/Au dots with various diameters were patterned on the surface of the wafers via standard contact lithography and liftoff. A buffered oxide etch was used prior to metallization. Using the metal dots as a self-aligned mask, HF/HNO_3 wet etching was performed to isolate the diodes into mesas. Finally, a Ti/Au backside contact was evaporated on all of the samples.

III. Results and Discussions

Fig. 2 shows the room-temperature current–voltage (*I–V*) characteristics of a vertically integrated RITD pair with the best combination of PVCR using an 825 °C, 1-min anneal. Double NDR regions in the forward-biasing condition were observed, with one diode showing a PVCR of 3.25 and J_p of 0.37 kA/cm^2, and another diode showing a PVCR of 3.21 with J_p of 0.39 kA/cm^2.

Note, the peak voltage of the first NDR region occurs around 1.2 V, which is much higher than the 0.1–0.2 V observed for prior discrete RITDs [5]–[7]. Hysteresis was observed when the voltage was swept forward and backward, which is also indicative of a large series resistance [11]. To properly identify the specific contribution to the double NDR and large series resistance by the upper RITD, lower RITD and backward diode, etching was performed to isolate each p-n junction. The *I–V* characteristics of both "discrete" RITDs are also plotted in Fig. 2 for comparison. The discrete upper and lower RITD exhibit almost identical *I–V* characteristics with their peak voltage around 0.2 V. The upper RITD shows a slightly lower peak current, therefore it will reach the bias state for NDR before the lower RITD in the integrated RITD pair and manifest as the first measured NDR for the vertical pair. The *I–V* characteristic of the "discrete" backward diode, Fig. 2, confirms that the large nonlinear series resistance in the integrated RITD pair causing the peak voltage shift and hysteresis originated from the reverse-biased backward diode.

To demonstrate tri-state logic, the vertically stacked RITD pair was combined with a resistor. The stacked RITD operated as the drive and a 1-kΩ off-chip resistor as the load, as shown schematically in Fig. 3(a). The load line analysis of the circuit with a representative stacked RITD pair and 1-kΩ resistor is shown in Fig. 3(b). The initial operating point of the tri-state latch is P1 by biasing V_{pulse} with a dc bias of 5.8 V, a positive triggering pulse is then fed to the resistor to momentarily lift the load line past the first peak and the operating point is moved to P2 at the trailing edge of the pulse. Note, that during this "write" operation, V_{out} deviates slightly from P2, until V_{pulse} is returned to its quiescent state of 5.8 V. An even higher triggering pulse then allows P3 to be accessed. Similarly, negative pulses superimposed on the dc bias of 5.8 V can lower the load line past the valley region and shift the operating point backward, stepping down from P3 to P2 or P1. Fig. 3(c) shows the resulting waveform of the state transitions from "0" to "1," "1" to "2," "2" to "1," and "1" to "0," effectively demonstrating the tri-state latching operation. The "0," "1," and "2" latched states correspond to 1.05, 1.55, and 2.04 V, respectively. Note, the intermediary point P2 can be bypassed when moving between states

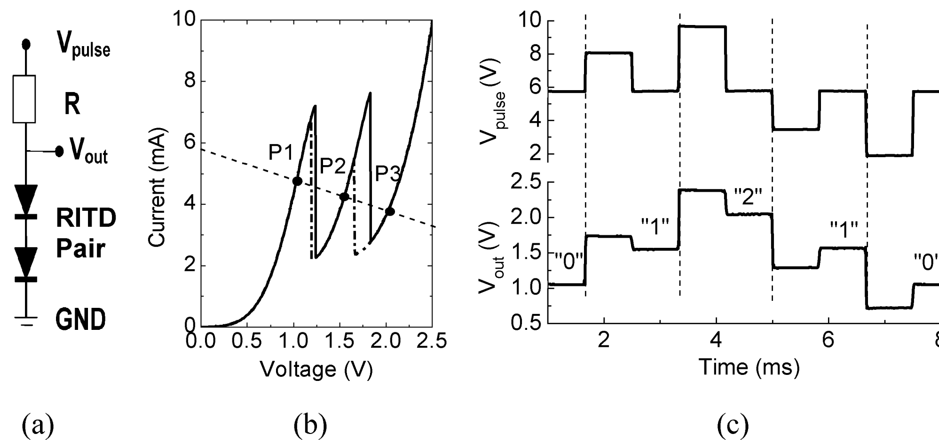

Fig. 3. (a) Circuit schematics of tri-state latch. (b) Load line analysis of the circuit with a representative vertically stacked RITD pair as the drive and a 1-kΩ resistor as the load. (c) Oscilloscope capture of the resulting waveform with V_{pulse} and V_{out} showing tri-state logic functionality.

P1 and P3, although this operation is not shown here. Intrinsic switching speeds were not evaluated at this time as the circuit should be limited by the parasitics associated with the external resistance and capacitance.

The noise margin of each state was defined as the minimum value of the current difference between the operating point and peak, and the current difference between operating point and valley [12]. In this presented circuit using a dc bias of 5.8 V, the noise margin for states "0," "1," and "2" were estimated to be 2.36, 2.05, and 1.42 mA, respectively. Therefore, the noise margin of this circuit is equal to 1.42 mA, which is limited by the state "2." By increasing the dc bias to 6.3 V and therefore equalizing the noise margin of states "0" and "2," this circuit would have a maximum noise margin of 1.88 mA. Using a constant current source as the load should further improve the noise margin up to half of the peak and valley current difference.

IV. Conclusion

Vertically integrated npnp Si-based resonant interband tunneling diode (RITD) pairs were successfully built with double NDR regions under forward bias. Tri-state logic was demonstrated by a breadboarded circuit using the vertically integrated RITD pair as the drive and an off-chip resistor as the load.

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