High Sensitivity Si-Based Backward Diodes for Zero-Biased Square-Law Detection and the Effect of Post-Growth Annealing on Performance

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Abstract—**High-sensitivity Si-based backward diodes were realized that are monolithically integratable with transistor circuitry. Potential applications include large area focal plane arrays. The Si-based backward diodes exhibit a high zero-biased curvature coefficient, γ, of 31 V^{-1} and a low zero biased junction capacitance, C_j, of 9 fF/μm^2, all at room temperature. The predicted low frequency voltage sensitivity, β_V, for a 50 Ω source is 3100 V/W. The high sensitivity, low junction capacitance, and Si/SiGe heterojunction bipolar transistor compatibility of the Si-based backward diodes make them very attractive for zero-bias square-law detector applications.**

Index Terms—**Backward diodes, millimeter-wave detectors, Si/SiGe heterojunction.**

I. INTRODUCTION

PASSIVE imaging systems and radiometers require highly sensitive detectors that can operate at millimeter-wave frequencies. Biased Schottky diodes are commonly used for these applications, however, the biasing circuit greatly increases the system and pixel complexity and also leads to extra noise and drift [1]. Zero-bias diode detectors are advantageous because no biasing circuit is required, but they require a large zero bias nonlinearity or curvature. Discrete Ge backward diodes [2] and planar-doped barrier GaAs diodes [3] have previously been used for zero bias detection with high nonlinearity. However, because of the chosen substrates, these devices are not readily suitable for direct-detection imaging applications, where a mass-producible technology is required to fabricate a large number of

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identical devices into compact pixilated imaging arrays. Recently, III-V material -based heterojunction backward diodes [4], [5] were realized that are excellent candidates for zero-bias detector applications due to their high sensitivity, high bandwidth, modest temperature dependence and mass production capability [6], [7]. However, the high cost of Sb-based backward diodes and their incompatibly with main-stream silicon read-out circuitry, may limit their use for cost-sensitive applications.

Epitaxially grown Si based backward diodes was previously used in a multiemitter Si/SiGe HBT to eliminate the need for a base contact [8]. In this letter, we report on the first epitaxially grown high sensitivity Si-based backward diodes for zero-bias diode detector applications. The fabricated diodes exhibit a curvature coefficient of 31 V^{-1} and associated junction capacitance of 9 fF/μm^2 at room temperature. This curvature corresponds to a low frequency voltage sensitivity, β_V, of 3100 V/W when driven from a 50 Ω source. Modeling indicates that an intrinsic cutoff frequency over 100 GHz can be achieved with Ni silicide technology which yields low contact resistance in the range of 10^{-7} Ω·cm^2 [9], [10], which makes this device promising for millimeter-wave operation. These Si-based backward diodes are processed similar to earlier reports of Si-based resonant interband tunnel diodes [11], [12] that have already been integrated with CMOS [13] and SiGe HBTs [14].

II. DEVICE DESIGN AND FABRICATION

The key to obtain highly nonlinear current-voltage characteristics with a high curvature coefficient at zero bias is to minimize any forward tunneling current, so that it can be substantially smaller than the backward tunneling current at comparable voltage levels. Since the amount of forward tunneling current depends on the available empty states on the p-side and available electrons on the n-side, one straightforward approach is to reduce the average majority carrier concentration at an Esaki tunnel junction [15], so that the Fermi level is just below the valence band on the p-side and just above the conduction band on the n-side, respectively. In this study, the Fermi level is adjusted by controlled dopant diffusion during post-growth rapid thermal annealing.

Fig. 1(a) shows the Si-based backward diode structure studied here, which is a step p-i-n structure comprised of an 80 nm B-doped p$^+$ Si layer, 1 nm undoped Si$_{0.6}$Ge$_{0.4}$ layer, 1 nm undoped Si layer, and a 100 nm P-doped n$^+$ Si cap layer. The SiGe layer is used to reduce the tunnel barrier height, to enhance
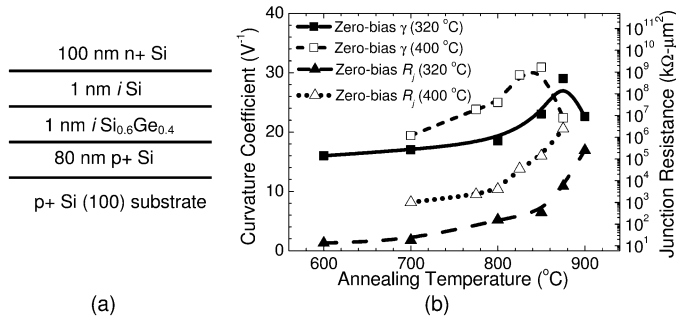
Fig. 1. (a) Schematic of the layered device structure of the Si/SiGe backward diodes used in this study. (b) The zero-bias curvature coefficient and junction resistance of Si/SiGe backward diodes (18 μm diameter mesas) are plotted as a function of the temperature of the 1-min post-growth rapid thermal annealing heat treatment. The lines are joins of the data. The epitaxial growth was done at a substrate temperature of 320 °C or 400 °C.

Fig. 2. (a) Normalized I–V characteristics of several backward diodes grown at 320 °C and annealed at various temperatures for 1 min by normalizing with respect to the zero biased junction conductance. (b) I–V characteristics and γ as a function of biasing voltage of a Si/SiGe backward diode grown at 400 °C and annealed at 850 °C for 1 min.

the momentum mixing, and hence to reduce the junction resistance. This entire structure was grown by molecular beam epitaxy (MBE) using elemental Si and Ge in electron-beam sources on 75 mm B-doped ($\rho = 0.015 - 0.04 \,\Omega\cdot$ cm) Si (100) wafers. The nominal doping levels for both the p-side and n-side are 5×10^{19} cm^{-3}. Two structures were grown with different substrate temperatures (320 °C and 400 °C) during growth of the active region. The low growth temperatures are employed to minimize Ge and dopant segregation.

Prior to device fabrication, portions of the grown wafers were rapid thermal annealed (RTA) using a forming gas ambient (N$_2$/H$_2$) in a Modular Process Technology Corporation RTP-600S furnace at temperatures between 600 °C and 900 °C for 1 min. There are two functions of the anneal. The main purpose is to controllably interdiffuse the dopant atoms so that various effective doping levels at the metallurgical junction can be readily obtained by simply varying the annealing temperatures rather than growing multiple MBE wafers. This enables rapid prototyping. The second purpose is to remove any point defects created during the low temperature MBE growth, in order to suppress the excess current component attributed to defect-related tunneling [16], [17]. Excess current has a concave-up characteristic, which will unfavorably compete with the concave-down characteristic of the desired forward tunneling current, and effectively reduce the curvature coefficient at zero bias. Details of the device fabrication process, which is identical to the process used to fabricate SiGe resonant interband tunneling diodes, can be found in [12].

III. RESULTS AND DISCUSSIONS

The curvature coefficient, γ, which is defined as the quotient of the second derivative by the first derivative, $(d^2I/dV^2)/(dI/dV)$, is the most commonly used figure-of-merit to quantify backward diode nonlinearity at zero bias. The voltage sensitivity, β_V, can subsequently be calculated to the first order by $\beta_V = 2\,Z_s\gamma$, where Z_s is the source impedance. Another important figure-of-merit is the junction resistance, R_j, determined by $R_j = dV/dI$ at zero bias.

Fig. 1(b) shows the measured curvature coefficient and junction resistance for the 18 μm diameter Si/SiGe backward diodes
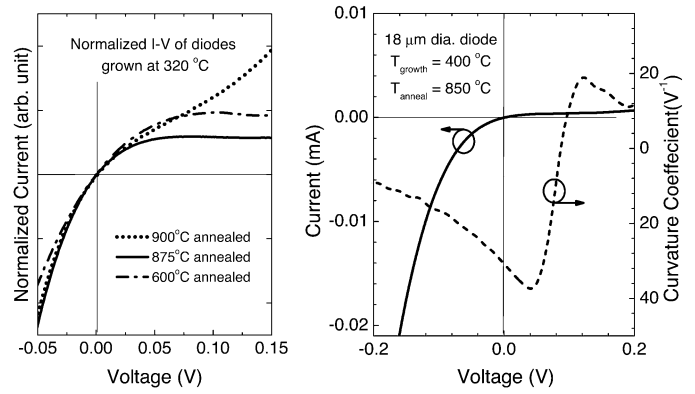
grown at 320 °C and 400 °C, and annealed at various temperatures. For the diodes grown at 320 °C, 600 °C annealing leads to a zero biased γ of 16 V^{-1} with a R_j of 13.5 kΩ μm^2, which is very close to the performance of a commercial discrete Ge backward diode for detector application (γ of 15.9 with a R_j of 18.2 kΩ μm^2) [4]. The junction resistance increases slowly as the annealing temperature increases for annealing temperatures below 800 °C. However, when the annealing temperature exceeds 800 °C, R$_j$ rises sharply, which can be attributed to a significantly increasing tunneling barrier width due to the P and B dopant interdiffusion and subsequent compensation of the central tunneling spacer region. The curvature coefficient, γ, exhibits a very good correlation with R$_j$ when annealing temperatures are below 875 °C. At 875 °C, the maximum γ value of 29 V^{-1} is obtained, which is almost double that of a commercial discrete Ge backward diode detector [4]. When the annealing temperature is further increased to 900 °C, γ drops to 23 V^{-1}.

In order to understand the relationship between γ and the annealing temperatures, the I–V characteristics of diodes grown at 320 °C and annealed at 600 °C, 875 °C, and 900 °C were normalized using a multiplicative scaling factor to have identical zero biased junction conductance (dI/dV) and these are plotted in Fig. 2(a). Since the zero biased junction conductance is exponentially dependent on the tunneling barrier width to the first order, the normalization process essentially excludes the effect of tunneling barrier width on the magnitude of the backward tunneling current, as well as the forward biased current, which consists of the desired forward tunneling current and any excess current present when the bias voltage is small. Note that γ is not altered by this normalization process. Fig. 2(a) clearly shows that after this scaling process, the normalized backward tunneling currents are almost identical, while the normalized forward bias currents are significantly different. Since the γ is determined by the ratio between the backward tunneling current and the forward biased current at the same small voltage level, the comparison between the γ of different diodes can be directly and readily made by comparing the normalized forward bias currents. A diode with a smaller normalized forward current under the same small bias condition will exhibit a larger γ.

It is clearly shown in Fig. 2(a) that when the annealing temperature increases from 600 °C to 875 °C, the normalized forward biased current decreases significantly. This is because dopant atoms diffuse faster at higher annealing temperature and reduce the effective doping densities on either side of the junction, so that the Fermi levels are much closer to the valence band on the p-side and the conduction band on the n-side respectively. This greatly limits the forward tunneling current. Also, the normalized excess current component, which is not explicitly shown here, is reduced with higher annealing temperatures. This occurs because point defects (e.g., vacancies created during LT-MBE within the tunneling barrier) that can induce an excess current are more effectively removed by higher annealing temperatures [16], [17]. The reduced normalized forward biased current leads to a sharp increase in the curvature coefficient in the range from 600 °C to 875 °C. However, when the annealing temperature is further increased to 900 °C, a strong concave up current component appears that reduces the curvature coefficient. With 900 °C annealing, dopant interdiffusion at the junction is significant so that a high concentration of both dopant atoms diffuse into the active region (tunneling barrier). As a consequence, defects may be formed that introduce extra energy states within the energy bandgap [18], which then leads to an increased normalized excess current. Furthermore, the energy states within the energy bandgap introduced by the P-B pairs may also act as recombination-generation centers. With the widened depletion region for 900 °C annealing from dopant compensation and neutralization, the recombination-generation current, which is a concave up current component, may become a more significant current component under small bias levels surpassing the tunneling component. Therefore, the concave up current which reduces the curvature coefficient at zero bias is identified as the excess current and/or recombination-generation current.

As shown in Fig. 1(b), the diodes grown at 400 °C exhibit similar trends of γ and R_j versus annealing temperature, except a shift of optimal annealing temperatures to lower values was observed, which can be attributed to more dopant diffusion during the MBE growth using a higher substrate temperature. Fig. 2(b) shows the *I–V* characteristic and γ as a function of bias voltage of the backward diode grown at 400 °C and annealed at 850 °C. The zero biased γ is as high as 31 V^{-1}, and the predicted low frequency voltage sensitivity β_V of this backward diode with a 50 Ω source is 3100 V/W. The zero biased junction capacitance, C_j, of this diode was measured as 9 fF/μm^2 using a HP 4284 LCR meter. With recent demonstrations of Ni silicide technology which yields low contact resistance in the range of 10^{-7} $\Omega \cdot$cm^2 [13], [14], the intrinsic cutoff frequency, $f_C = 1/(2\pi R_s C_j)$, was estimated to be well over 100 GHz. Although the zero biased R_j in the first-generation devices is measured as 140 M$\Omega \cdot \mu$m^2, the diodes still exhibit a usable unmatched sensitivity of 3100 V/W for a 50 Ω source. Further optimization of the heterostructure is expected to improve the junction resistance to both solve the mismatch problem and reduce the thermal noise. The high sensitivity, low junction capacitance, and SiGe HBT compatibility of the Si-based backward diodes grown by LT-MBE makes them very attractive for zero-bias square-law detector applications, potentially into the millimeter-wave regime.

IV. CONCLUSION

High sensitivity Si-based backward diodes which are suitable for zero-bias square-law detector applications have been demonstrated. Post-growth annealing effectively reduces the point defects. But, more importantly, various effective doping levels can be explored at the junction, hence a large variety of device configurations can be obtained simply by controlling the annealing temperatures. Diodes grown at 320 °C and annealed at 600 °C showed a zero biased γ of 16 V $^{-1}$ with a R_j of 13.5 k $\Omega\mu$m^2, which is very close to the reported performance of discrete commercial Ge backward diodes. While a 400 °C growth temperature and 850 °C annealing temperature lead to the highest zero biased γ of 31 V^{-1} with a zero bias C_j of 9 fF/μm^2, which projects to a low frequency voltage sensitivity β_V for a 50 Ω source of 3100 V/W, and an intrinsic cutoff frequency of over 100 GHz using state-of-the-art Ni silicide technology.

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