Room-temperature negative differential resistance in polymer tunnel diodes using a thin oxide layer and demonstration of threshold logic

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Conjugated polymers, with π molecular orbitals delocalized along the polymer chain, are useful organic semiconductors that provide the possibility of molecular electronics for low-power organic-based memory and logic. Quantum functional devices based upon carrier tunneling processes open vistas into very efficient and low-power consumption circuitry that would be ideal for these applications. We demonstrate here strong room temperature negative differential resistance (NDR) for poly[2-methoxy-5-(2′-ethyl-hexyloxy)-1,4-phenylenevinylene] (MEH-PPV) polymer tunnel diodes (PTD) using a thin TiO_2 tunneling layer ($\sim$2–8 nm) sandwiched between the MEH-PPV and the indium tin oxide anode. A key advantage is the pronounced NDR using a thick polymer layer with a large active area, circumnavigating the need for molecularly-sized junctions. Current-voltage measurements show large and reproducible NDR with a PVCR as high as 53 at room temperature. We also demonstrate basic logic circuit operation using a pair of these PTDs connected in series to form a monostable-bistable transition logic element (MOBILE) latch. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2130395]

Negative differential resistance (NDR) devices, in general, have tremendous potential for low power memory[1] and logic,[2] but successful demonstrations of room temperature NDR suitable for circuit applications has been restricted to rigid inorganic semiconductors. Smartcard technology, in particular, for banking and medical information, would be advanced by flexible low-power memory. The advantage of quantum functional circuits is illustrated by the N-shaped electrical characteristics of two serially connected NDR devices which can be exploited to form two stable latching points. When this pair is fashioned into a one transistor tunneling diode static random access memory (1T TSRAM) cell utilizing NDR devices with extremely low valley current densities, the number of devices needed and the standby power consumption are greatly decreased from traditional six transistor SRAM memory.[1] The requirement of a NDR device for these circuit topologies is room temperature NDR operation with a reasonably high peak-to-valley current ratio (PVCR) ($\geqslant$3). The creation of a suitable organic-based NDR device could enable new opportunities in molecular and organic based memory and logic circuits.[3,4]

Since the first report of NDR using molecules as the active material,[5] electronic devices using single (or multiple) molecules that exhibit NDR have intrigued researchers for their potential in low power electronics,[3] but, to date, these demonstrations have limited yield, repeatability and often a nonoptimal current-voltage shape for proper latching behavior.[6–8] A prime motivator is the wide versatility in chemical and molecular structures that allows for a large ability to tune the diode behavior.

Comparatively much thicker layered organic devices, similar to polymer light emitting diodes,[9] which also exhibited NDR, would have a considerable advantage over molecular junctions, such as low fabrication costs and flexible substrates. During the past 10 years, attempts have been made to investigate NDR behavior in organic thin film devices that have similar configurations with molecular junctions but it has not been demonstrated successfully yet.[10–13] In addition, most organic thin film devices were operated under positive bias, and not explored in the negative bias regime. Recent reports of polymer thin film memory devices are based on bistable conductance states, not NDR behavior.[14,15] Here we report large and reproducible NDR behavior at room temperature in thick, large-area polymer tunnel diodes (PTD) that utilize a thin TiO_2 tunneling layer which was fashioned into a monostable-bistable transition logic element (MOBILE) latch[16,17] using a pair of PTDs connected in series with robust logic operation.

Indium tin oxide (ITO) coated glass substrates were used with a sheet resistance (R_s) below 10 Ω cm. TiO_2 layers were then added atop the ITO anodes by the following two steps. First, a thin layer of Ti metal was electron beam evaporated in a low pressure range ($\sim 10^{-7}$ Torr). Varying Ti layer thicknesses (2–20 nm) were deposited on a number of ITO-glass substrates to observe the dependence of NDR behavior on the thickness of the TiO_2 layer. Next, the Ti metal was oxidized using an inductively coupled plasma reactive ion etching (ICP-RIE) system with oxygen plasma at a rf power of 80 W and the substrate held at room temperature.[18] The duration of the plasma oxidation varied as a function of the Ti layer thickness in order to completely convert the metal layer to TiO_2. The TiO_2 layers were monitored using atomic force microscopy (AFM) and ellipsometry. AFM data indicates that the as-deposited metallic Ti layer with a grain structure converted to a smoother surface after oxygen plasma oxidation (Root mean square roughness $\sim$1 nm). The refractive index of the thinner TiO_2 layers was $\sim$2.2 as measured by ellipsometry, which clearly indicates the complete oxidation of the titanium films. For thicknesses $\geqslant$8 nm, the refractive index of the Ti/TiO_2 layer indicates an incomplete

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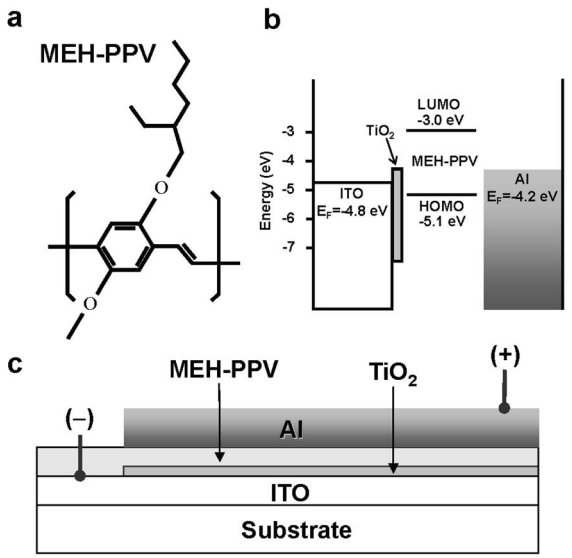

FIG. 1. Polymer material and device structure with its associated energy band diagram used in this study to demonstrate robust, bulk and large area polymer tunnel diodes. (a) The structure of MEH-PPV. (b) The flat band energy level diagram for the polymer tunnel diode. (c) The ITO/TiO_2/MEH-PPV/Al device structure consists of a polymer thin film ~25 nm thick between an aluminum cathode and a transparent conducting anode, ITO coated with a thin TiO_2 layer (2–20 nm). The active area of all the devices studied was 0.19 cm^2.

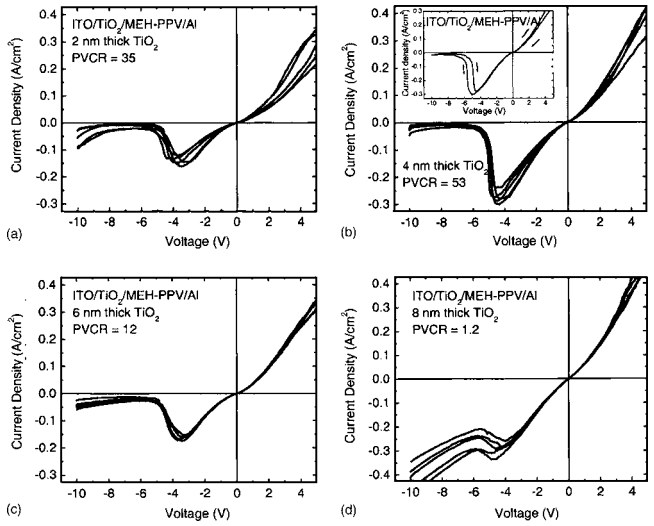

FIG. 2. *I-V* characteristics of 5 representative ITO/TiO_2/MEH-PPV/Al polymer tunnel diodes from the same sample which exhibit NDR under reverse bias with four different titanium layer thicknesses. (a) 2 nm; (b) 4 nm; (c) 6 nm; and (d) 8 nm. The inset of (b) in the upper left corner shows an *I-V* characteristic of polymer tunnel diode with hysteresis. The thickness of the as-deposited titanium layers before the plasma process is referred to as the thickness of the final TiO_2 layers.

oxidation and *I-V* characteristics also suggest the presence of metallic Ti below the TiO_2 along with a visual inspection of the layer transparency.

Thin films of poly[2-methoxy-5-(2′-ethyl-hexyloxy)-1,4-phenylenevinylene] (MEH-PPV) [Fig. 1(a)] were then spin coated atop the TiO_2 layer from a 0.5% MEH-PPV solution in 80% toluene and 20% tetrahydrofuran. This solution was warmed at 60 °C for 24 h. The spin-coated films were nominally 25 nm thick. The PTDs were completed by a shadowmask evaporation (~10^{-6} Torr) of an Al cathode, about 250 nm thick, directly onto the MEH-PPV [Fig. 1(c)]. All fabrication steps were performed in an inert glove box. Electrical measurements were performed with a semiconductor characterization system at room temperature under darkness. The ITO coated glass substrates of a control device (ITO/PEDOT:PSS/MEH-PPV/Al) was covered by PEDOT:PSS and was then annealed at 110 °C with a resulting thickness of ~60 nm. The resulting band diagram of the ITO/TiO_2/MEH-PPV/Al PTDs is shown in Fig. 1(b) and a schematic shown in Fig. 1(c).

Typical *I-V* characteristics of five different PTDs (a 2 nm thick TiO_2 layer) are shown in Fig. 2(a). Large and reproducible NDR is observed for all devices in a bias ranging from −10 V to 0 V. The measured peak current density for these devices was 0.13 A/cm^2, with a valley current density of ~0.004 A/cm^2, corresponding to a peak-to-valley current ratio (PVCR) of 35:1. The valley current density was generally two orders of magnitude lower than the peak current density for most measured PTDs ($\leqslant 5.0\times10^{-3}$ A/cm^2), which is ideally suited for low power organic-based memory. A small variation (±0.001 A/cm^2 in the peak current density and ±0.08 V in the peak current density position) was observed for successive sweeps. It should be noted that *I-V* characteristics for all the devices measured in this study were repeatable. After testing, the devices were stored in an inert glove box for 30 days with little variation in their peak current density and peak current position (not shown here). Some device-to-device variations were observed in the peak current density (±0.004 A/cm^2) and in the peak current position (±0.57 V). These device-to-device variations can be attributed to small variations in the thickness of TiO_2 layer and polymer films across each sample.

The effect of varying the thickness of TiO_2 to determine its influence on *I-V* characteristics is shown in Figs. 2(b)–2(d). The device with a 4 nm thick TiO_2 layer has a maximum peak current density of 0.29 A/cm^2 with a PVCR of 53:1 [Fig. 2(b)]. The inset in Fig. 2(b) is a forward and backward *I-V* sweep of the same device showing some hysteresis. A shift of about 0.6 V is observed. Some hysteresis is observed in all devices (up to an 8 nm TiO_2 layer) and is repeatable. As the TiO_2 layer thickness reaches 6 nm, the peak current density decreases [Fig. 2(c)]. However, the device with an 8 nm thick TiO_2 layer shows a large leakage current with its maximum peak current density of 0.23 A/cm^2 [Fig. 2(d)]. It was observed that the NDR behavior persists around −5 V with increasing TiO_2 layer thickness (up to 8 nm). However, due to a large leakage current in a bias range of −10 V and 0 V, the peak current density can not be measured quantitatively for devices with thicker TiO_2 layers. The large leakage current in thicker barrier samples can be ascribed to a localized current pathway through the remaining metallic Ti which was not completely oxidized and converted to TiO_2 during the plasma oxidation process. Table I summarizes the *I-V* characteristics of the devices illustrating the peak current density, peak voltage, valley current density, valley voltage, and PVCR.

Control devices, one without a TiO_2 layer (ITO/MEH-PPV/Al) and another inserting PEDOT:PSS between the ITO and MEH-PPV films (ITO/PEDOT:PSS/MEH-PPV/Al) did not exhibit NDR in the bias range of −10 V and 0 V (not shown here), which indicates that the observed NDR behav-

TABLE I. The peak current density (J_{peak}), peak voltage (V_{peak}), valley current density (J_{valley}), valley voltage (V_{valley}), and PVCR are calculated from the *I-V* curve of ITO/TiO_2/MEH-PPV/Al polymer tunnel diodes. Results from the best performed devices are presented.

Tunneling barrier (nm)	J_{peak} (A/cm^2)	V_{peak} (V)	J_{peak} (A/cm^2)	V_{valley} (V)	PVCR
2	−0.13	−3.3	−0.004	−6.4	34.5
4	−0.29	−4.4	−0.006	−7.4	53.4
6	−0.16	−3.5	−0.013	−6.1	12.4
8	−0.23	−5.6	−0.199	−5.6	1.2

ior is not induced by electron trapping in the ITO or metal spikes at the anode/polymer interface.[19]

The observed reverse-biased NDR behavior does not seem to occur via tunneling across the thin TiO_2 layer acting as a traditional tunneling barrier based upon the measured *I-V* characteristics and observed switching effects (not shown here). This is evidenced by the lack of the measured peak current density to exponentially decrease with increasing TiO_2 layer thickness (Table I).

Our results suggest that the NDR behavior observed occurs instead as a result of tunneling through localized defect sites[20] within the thin TiO_2 layers induced during the plasma oxidation that are confined to a small range of energies within the TiO_2 bandgap near the TiO_2 conduction band.[21] The mechanism for NDR under reverse bias in these ITO/TiO_2/MEH-PPV/Al PTDs is speculated to occur via electrons emitted from the *n*-type ITO, tunneling through defect states in the TiO_2, which are then collected by the lowest unoccupied molecular orbital (LUMO) level in the MEH-PPV [Fig. 1(b)]. This hypothesis is reinforced by the diminished NDR observed in a control sample where the TiO_2 layer was plasma-oxidized at ~400 °C, which is known to lead to better crystallinity[22] and therefore provides fewer defect states available for tunneling.

To demonstrate useful quantum functional circuit operation using the PTDs, a MOBILE latch operation employing the monostable-bistable transition[2] was used. First two PTDs with a 2 nm thick TiO_2 layer were serially connected and the bias (V_{DD}) was swept. The inset in Fig. 3 shows the two successive NDR regions. Next the MOBILE logic function was realized by incorporating a commercial junction field effect transistor (JFET) connected to the central storage node of the pair of serially connected PTDs, as shown in the lower right corner of Fig. 3. In order for the PTD pair to latch, charging or discharging was provided by the JEFT input current. With a JFET gate bias (V_G) of 1.5 V and drain-to-source bias (V_D) of 1 V, the input current was 20 mA. For an applied clock voltage (V_{CLK}) the output voltage at the sense node (V_{SN}) was measured when the JFET is in the off state (i.e., V_G=−3) and on-state (i.e., V_G=1.5 V) as shown in Fig. 3. The MOBILE circuit forms two stable latching points at the sense node, demonstrating bistable latching operation. For an applied V_{CLK} of −8 V, the voltages of the logic high (V_H) and low (V_L) are −1.95 V and −6.01 V, respectively. The percentage of voltage swing, which is ratio between V_H and V_L for applied V_{CLK}, was 51%. Thus, stable latching and quantum functional circuit operation is demonstrated.

In conclusion, NDR devices based upon a conjugated polymer platform were developed and applied towards a latching circuit. Their room temperature operation, large area, bulklike thickness and simple solution processable platform are key advantages.

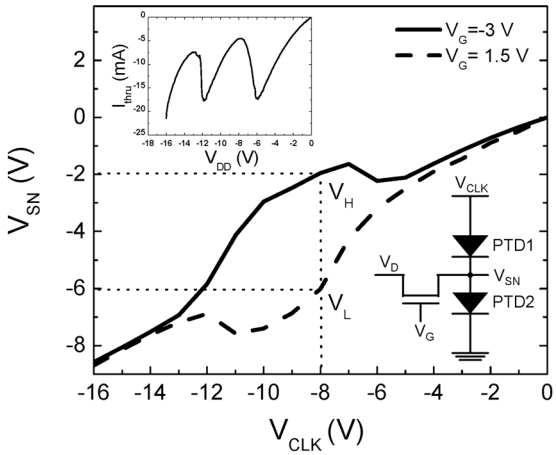

FIG. 3. Voltage at the sense node as a function of clock voltage of JFET-polymer tunnel diodes MOBILE latch with a 51% voltage swing of the applied V_{CLK} at −8 V. The inset in the upper left shows an *I-V* characteristics of two ITO/TiO_2/MEH-PPV/Al polymer tunnel diodes (a 2 nm thick TiO_2 layer) connected in series in a bias range of −16 V and 0 V.

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