NMOS/SiGe Resonant Interband Tunneling Diode Static Random Access Memory

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Tunneling-based static random access memory (SRAM) has been sought as a viable solution for a low power and high speed embedded memory application. The first cell design, proposed by Goto *et al.* [1], consists of two tunnel diodes connected in series, one acting as the drive and the other as the load as shown in Fig. 1. This configuration allows for bistable operation at a particular range of supply voltages (V_{DD}). The information is stored at the sense node, which can be altered by modulating current into the node via a FET. By injecting a current into the sense node, the cell is forced to latch to a high state as illustrated in Fig 1(b). During write low operation, the FET is used to discharge the cell, pulling the sense node potential to a low state as depicted in Fig 1(c). The demonstration of this type of bistable latch has been done in the III-V material system, showing a very promising performance both in speed and power dissipation [2]. Morimoto et al. realized the system in Si platform by utilizing p+Si/oxynitride/n+poly [3]. The result, however, was limited by the lack of capability to scale to lower current density. Previously the authors have shown a successful integration of Si/SiGe resonant interband tunnel diode (RITD) with CMOS, demonstrating a monostable-bistable logic element [4]. In this paper, the realization of integrated NMOS/SiGe RITD TSRAM with ultra-low voltage operation is reported for the first time.

Fig. 2 shows the device structure of the Si/SiGe RITD used in this study. It is a hybrid between a conventional Esaki and a resonant tunnel diode (RTD). The resonant states are established via δ-doping planes and the energy band offset between Si and SiGe. The variation on intrinsic layer thickness enables current scaling from 151 kA/cm^2 to 20 mA/cm^2 [5], providing design flexibility for targeted circuit applications. A Si/SiGe RITD with an 8 nm *i*-layer thickness was grown via low-temperature molecular beam epitaxy (LT-MBE) and integrated with CMOS through openings in the field SiO_2 layer. These layers were grown on top of implanted p^+ regions that are embedded in the n-well of the CMOS. Fig. 3 displays the SEM micrograph of two Si/SiGe RITDs integrated with an NFET to form a TSRAM cell.

The current-voltage load line characteristics of the drive and load tunnel diodes are shown in Fig. 4. The tunnel diodes have a peak-to-valley current ratio up to 1.87 and a peak current density up to 52.7 A/cm^2. The intersections between load and drive characteristics provide two stable latching points. Although there is another intersecting point at the negative differential resistance (NDR) region, this latching state is unstable due to inherent oscillatory instabilities of the circuit. The ratio of the difference between high and low-state with respect to V_{DD} reaches a maximum of 53.5% at a standby supply voltage of 0.57 V. The cell can either latch to a low-state at 0.13 V or a high-state at 0.43 V. Fig. 5 illustrates the transfer characteristics of the voltage at the sense node (V_{SN}) as a function of V_{DD}. The bistable curves were obtained by forward and backward sweeping the power supply voltage from 0 V to 1 V and from 1 V to 0 V, respectively. It is clear from this graph that the TSRAM exhibits bistable operations at V_{DD} ranges from 0.47 V to 0.78 V. The supply voltage range is determined primarily by the peak voltage of the drive tunnel diode that is dependent upon the amount of series resistance in the system. With V_{DD} at 0.57 V, the memory cell will have high-state at 0.44 V and low-state at 0.13 V. These numbers are in good agreement with the numbers from the load-line characteristics. Fig. 6 shows the corresponding time diagram of the TSRAM during latching high, latching low and standby conditions.

In conclusion, the authors have fabricated and demonstrated the first NMOS/SiGe RITD-based TSRAM cell that successfully operates at power supply voltages below 0.5 V. This work opens up new possibilities for the realization of ultra-low power TSRAM utilizing low current density Si/SiGe RITDs.

1. E. Goto, *et al.*, "Esaki diode high-speed logical circuits," *IRE Trans. Elec. Comp..*, vol. 9, pp. 25–29, Mar. 1960.
2. J.P.A. Van der Wagt, "Tunneling-based SRAM," *Proc. of IEEE*, vol. 87, pp. 571-595, April 1999.
3. H. Sorada, *et al.*, "A Monolithically Integrated Si-interband Tunneling Diode (IBTD)/MOSFET for Ultra Low Voltage Operation Below 0.5 V," Superlattices and Microstructures, vol.28, pp. 331-337, 2000.
4. S. Sudirgo, *et al.*, "Monolithically Integrated Si/SiGe Resonant Interband Tunnel Diode/CMOS Demonstrating Low Voltage MOBILE Operation," *Solid-State Elec.*, vol. 48, issues 10-11, pp. 1907-1910, Oct.-Nov., 2004.
5. N. Jin, *et al.*, "The Effect of Spacer Thicknesses on Si-based Resonant Interband Tunneling Diode Performance and their Application to Low-Power Tunneling Diode SRAM Circuits," *Submitted to Trans. Elec. Dev.*

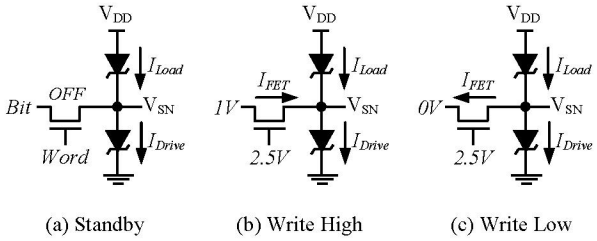

Fig. 1 Biasing conditions during (a) standby, (b) write high, and (c) write low operations.

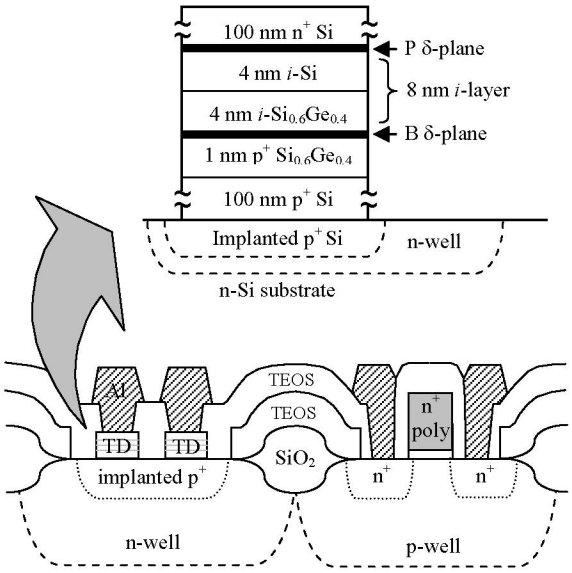

Fig. 2 Schematic diagram of NMOS/SiGe RITD with 8 nm *i*-layer integrated atop of a p^+ well of CMOS.

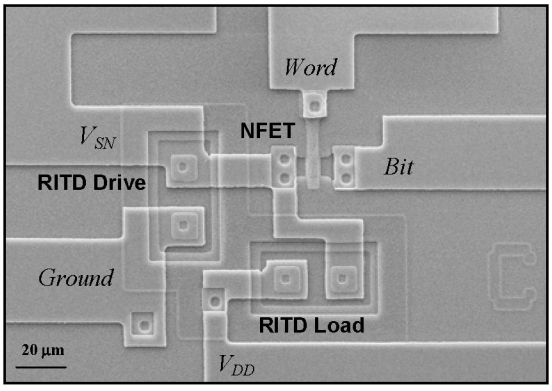

Fig. 3. SEM micrograph of two Si/SiGe RITDs monolithically integrated with an NFET to form a tunneling-based SRAM cell.

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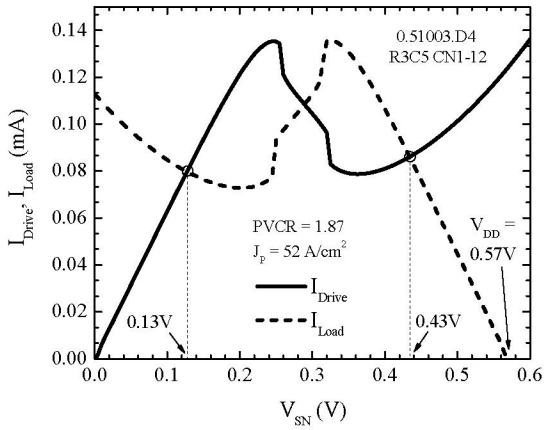

Fig. 4. Load line analysis of back-to-back tunnel diodes, providing two stable latching points at 0.13 V and 0.43 V at V_{DD} = 0.57 V.

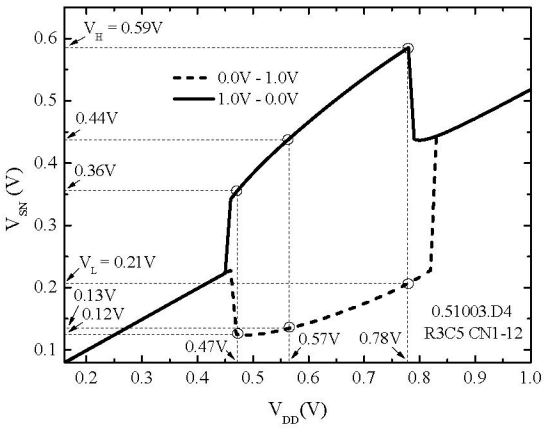

Fig. 5. Transfer characteristics of voltage at the sense node (V_{SN}) as a function of voltage supply (V_{DD}).

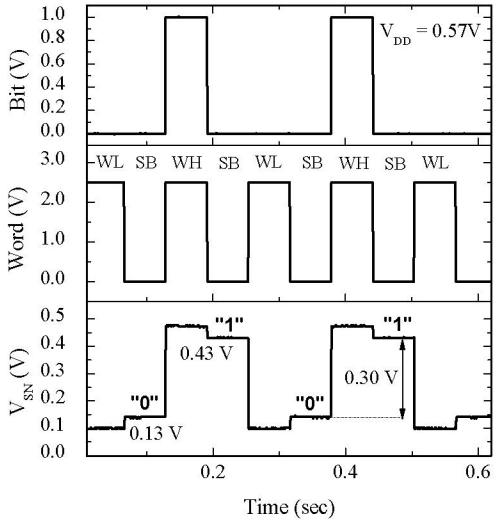

Fig. 6. Time diagram of T-SRAM cell during standby (SB), write high (WH) and low (WL) operations at V_{DD} of 0.57 V.