Low sidewall damage plasma etching using ICP-RIE with HBr chemistry of Si/SiGe resonant interband tunnel diodes

S.-Y. Park, S.-Y. Chung, R. Yu, P.R. Berger and
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The effect and influence of dry plasma etching processes of Si/SiGe using HBr for the formation of diode mesa structures has been investigated to minimise sidewall leakage current. To characterise sidewall damage electrically, Si-based resonant interband tunnel diodes (RITD) were processed and the completed RITDs compared by their peak-to-valley current ratio (PVCR) and valley current density (VCD), which are sensitive to defect related currents. Dry processed RITDs were compared to reference RITDs fabricated by wet chemical etching (HNO_3:HF:H_2O = 100:1:100). The combination of HBr process gas and very low substrate bias power (10 W) for inductively coupled plasma reactive ion etching (ICP-RIE) yielded the better results. The resulting RITDs processed by ICP-RIE using HBr chemistry show high PVCR of 4.02 with VCD of 32 A/cm^2 while wet etched RITDs show a PVCR of only 2.81 with VCD of 40 A/cm^2. Hydrogen passivation during the HBr plasma process may play a role that overcomes the slightly higher surface roughness compared to wet etching.

Introduction: Dry plasma etching of semiconductor devices is becoming the industry standard for its reliable process control. However, as Si/SiGe nanoelectronic devices are aggressively scaled, their sensitivity to plasma damage becomes more acute. Qualification of new etch chemistries only by their sidewall profile and surface roughness does not reveal the role of electrically active damage. In this Letter, we present a study using an HBr plasma to etch Si/SiGe resonant interband tunnel diodes (RITDs), which are a good test bed for qualifying electrically active damage.

Hybrid tunnel diode/transistor circuits have great potential in many circuit applications, which includes memory, digital logic, mixed-signal circuits, owing to superior high-speed performance, ultra-low power consumption and reduced device count compared to transistor-only topologies [1, 2]. Recent progress on Si-based RITDs [3, 4] coupled with their successful integration with CMOS and SiGe-based heterojunction bipolar transistors (HBT) make Si-based RITDs excellent candidates to extend the Si technology beyond the expected limitation forecasted by the International Technology Roadmap for Semiconductors (ITRS) [4]. Up to now, Si-based RITDs have demonstrated peak-to-valley current ratios (PVCR) up to 6.0 [5] and peak current density (PCD) as high as 151 kA/cm^2 [6], all at room temperature. The PVCR of Si-based RITDs is mainly limited by the excess current that consists of defect related tunnelling currents around the junction and leakage currents along the unpassivated mesa sidewall. The former is due to defects created during low temperature epitaxial growth, which can be reduced by a post-growth anneal [7]. The latter is due to sidewall current pathways through damage induced during mesa etching. Epitaxially induced defects should scale with area and sidewall damage should scale with perimeter.

In this study, inductively-coupled plasma reactive ion etching (ICP-RIE) processes were extensively studied to investigate ways to reduce the leakage current along the mesa sidewall. A similar study of tunnel diode valley current as function of diode area was performed by Fay *et al.* [8]. Preliminary to our investigation, the ICP power was varied and it was found that an ICP power of 250 W (combined with a minimum substrate bias power) produced a reasonably good etch rate for our purpose. Furthermore, the minimum substrate bias power, of around 10 W, was explored, while maintaining a high plasma density and successfully coupling the plasma to the lower electrode, with the goal of minimising surface damage. Using an HBr plasma chemistry, which contains both hydrogen and bromine radicals, the hydrogen radicals may have a secondary effect of passivating ionised defect centres in Si-based materials. The resulting plasma etched RITDs showed a PVCR up to 4.02, significantly higher than the control device (PVCR of 2.81) fabricated by wet chemical etching (HF:H_2O:HNO_3).

Experiment: Fig. 1*a* shows the schematic diagram of the basic Si-based RITD structure used for this etching study, which mainly consists of two quantum wells created by *n*-type and *p*-type δ-doped planes with intrinsic tunnelling spacer layers between the two δ-doped planes. The choice of a composite 4 nm Si/4 nm SiGe spacer layer was made to enhance the RITD's sensitivity to the sidewall leakage current component in terms of valley current density (VCD) and PVCR. A thick spacer layer reduces the desired tunnelling current component while raising the excess current contribution to the VCD owing to increased tunnelling barrier thickness [6].

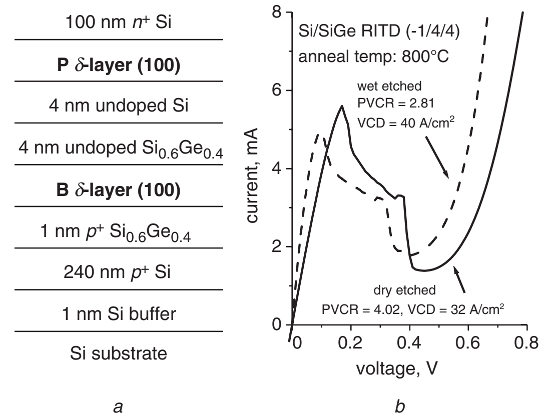

Fig. 1 *(a) Schematic diagram of 4 nm Si/4 nm Si/SiGe RITD (−1/4/4) test structure with 1 nm SiGe cladding below active region; (b) I-V characteristics of representative Si/SiGe RITD etched using HBr chemistry in ICP-RIE process compared with control RITD using wet etching, both with nominally 75 µm mesa diameters*

The Si/SiGe (−1/4/4) RITD structure was grown by low-temperature molecular beam epitaxial (LT-MBE) growth, shown in Fig. 1*a* following a general schematic described in ref. [9].

Prior to device fabrication, small portions from the whole wafer grown by LT-MBE were annealed separately in a rapid thermal annealing (RTA) furnace at 800°C for 60 s under a nitrogen gas ambient (N_2) to reduce the point defect density induced by the LT-MBE process. Self-aligned devices were fabricated by photolithographic and electron beam evaporator of metal contacts.

The ICP-RIE etching used an Oxford System100 with ICP180 tool and wet etching was via a standard HF:H_2O:HNO_3 (1:100:100) solution. The desired mesa structures were created on the wafer using the Ti/Au/Cr ohmic contact as a self-aligned mask. The optimal parameters used in this study included an HBr flow rate of 40 sccm with 250 W of ICP power (to sustain the plasma), 10 W of substrate bias power (to couple the plasma to the stage) at a 5 mtorr chamber pressure and with a nominal 20°C stage temperature. Samples were attached to a four-inch Si carrier wafer with high temperature grease facilitating a better heatsink during the plasma process to maintain the substrate nominally at room temperature. This resulted in an etching rate of about 80 nm/min. No post-plasma wet chemical treatment was used to reduce intrinsic plasma-induced damage.

Results: The minimum substrate bias power to strike a plasma during the plasma process was investigated. As the substrate bias power was increased from 3 to 10 W, the ICP power, chamber pressure, gas flow rate and chuck temperature were kept constant at 250 W, 5 mtorr, 40 sccm and 20°C, respectively. The ICP power and gas flow rate were varied previously, and these values were determined to yield suitable results. A 10 W substrate bias power was determined to be the minimum substrate bias power to create a stable and reliable plasma with a reasonable etch rate.

Fig. 1*b* shows room temperature I-V characteristics of a representative 75 µm diameter RITD processed with the specified HBr ICP-RIE process. The plasma-etched depth was about 240 nm for a 3 min process duration. The room temperature PVCRs for the HBr etched RITDs and wet etched RITDs were recorded as high as 4.02 with a PCD of 32 A/cm^2 and 2.81 with a VCD of 40 A/cm^2, respectively, Fig. 1*b*. This equates to ~40% enhancement in measured PVCR for the HBr plasma etched sample. The slight difference in the absolute peak currents of the wet etched sample and the plasma etched sample is due to the discrepancy in their respective diode areas as wet-etching results in mesa undercutting, unlike the vertical wall from plasma etching.

In spite of being exposed to energetic ions the PVCR for the plasma-etched RITDs were ~30% greater than that of wet-etched devices. One

explanation is that wet etching either induces some damage or leaves some residue on the surface that contributes to leakage current pathways. This effect would manifest itself as a perimeter dominated effect. Another explanation is that the plasma etching process with HBr, which includes hydrogen radicals, may have passivated ionised centres, thereby reducing bulk defect state densities, thus lowering the measured VCD [10], assuming the hydrogen penetration depth is sufficient to reach the active region.

Fig. 2 shows a comparison of the valley current for various RITD active areas of dry and wet etched samples showing that the valley current correlates linearly very strongly with the device active area. Fig. 2 indicates the effect of exposure to a hydrogen-only plasma on the valley current of a wet etched sample to test the role of hydrogen radical passivation. Both the area dependence of the VCD and the effect of the hydrogen plasma on the VCD of the wet-etched sample suggest that hydrogen passivation is the mechanism involved with the HBr results.

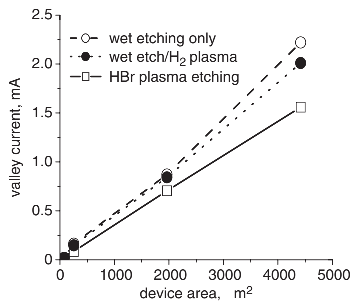

Fig. 2 *Valley current of Si/SiGe RITDs against device area of wet etched, HBr plasma etched and wet etched followed by hydrogen plasma treatment*

Inspection of surfaces with a scanning electron microscope indicate there is greater surface damage on the plasma-etched sample compared to the wet-etched sample, despite using a very low substrate bias power. Atomic force microscopy scans of the surfaces indicate the root mean square (RMS) surface roughness of the wet etched sample is only 2.3 nm, while the dry etched sample is 3.9 nm. Thus, dry etching with HBr induces slightly more physical damage than wet etching. However, a secondary effect, such as hydrogen passivation, must be overcoming the slightly increased physical damage.

Conclusion: ICP-RIE etching of Si/SiGe RITDs using a HBr chemistry with minimal substrate bias power to sustain a plasma is a promising approach with reasonable etch rates for Si/SiGe nanoelectronics with barely discernable ion induced damage on the sample. The PVCR of 4.02 with a VCD of 32 A/cm^2 for ICP etched samples is 30% higher than for wet etched devices.

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