Si/SiGe Resonant Interband Tunnel Diode With f_{r0} 20.2 GHz and Peak Current Density 218 kA/cm^2 for K-Band Mixed-Signal Applications

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***Abstract*—This letter presents the room-temperature high-frequency operation of Si/SiGe-based resonant interband tunnel diodes that were fabricated by low-temperature molecular beam epitaxy. The resulting devices show a resistive cutoff frequency f_{r0} of 20.2 GHz with a peak current density of 218 kA/cm^2, a speed index of 35.9 mV/ps, and a peak-to-valley current ratio of 1.47. A specific contact resistivity of $5.3 \times 10^{-7}\ \Omega \cdot cm^2$ extracted from RF measurements was achieved by Ni silicidation through a P δ-doped quantum well by rapid thermal sintering at 430 °C for 30 s. The resulting devices are very good candidates for RF high-power mixed-signal applications. The device structures presented here are compatible with a standard complementary metal–oxide–semiconductor or heterojunction bipolar transistor process.**

***Index Terms*—Microwave diodes, microwave oscillators, negative resistance devices, resonant tunneling diodes, semiconductor epitaxial layers, silicon alloys.**

I. Introduction

QUANTUM functional circuits based on negative differential resistance (NDR) devices such as tunnel diodes have superior performance to those based on conventional devices in terms of higher speed operation, lower power consumption, and reduced device count. Many quantum functional circuits for high-speed mixed-signal, low-power consumption memory, and ultrafast logic applications have already been demonstrated using III–V-based NDR devices [1]–[3]. However, such technology is not readily compatible with the mainstream Si-based platforms of CMOS and heterojunction bipolar transistor (HBT) technologies. Recently, we demonstrated the successful monolithic integration of Si-based resonant interband tunnel diodes (RITDs) with CMOS [4] and SiGe HBT [5], which makes them more attractive than III–V-based tunnel diodes for system level integration. The best measured RF results of Si-based tunnel diodes at room temperature were from a Si/SiGe RITD that exhibited a resistive cutoff frequency f_{r0} of 5.6 GHz with a peak current density (PCD) of 156 kA/cm^2, a speed index of 24.6 mV/ps, and a peak-to-valley current ratio (PVCR) of 1.2 [6]. There was also a report of an intraband Si-based resonant tunnel diode (RTD) with a high PCD of 282 kA/cm^2 and a PVCR of 2.4, but f_{r0} was not measured [7]. A more detailed discussion of the issues associated with high f_{r0} performance for Si-based tunnel diodes is included in [6], but it should be noted here that a high current density more directly equates to high-frequency operation in a tunnel diode than its PVCR.

In this letter, we report on Si-based RITD with an f_{r0} of 20.2 GHz, a PCD of 218 kA/cm^2, a speed index of 35.9 mV/ps, and a PVCR of 1.47. The resistive cutoff frequency, 20.2 GHz, is 3.6× higher than the highest f_{r0} for any reported Si-based tunnel diode [6], [8]–[10] and enables K-band mixed-signal and RF circuit applications for the first time, such as analog-to-digital converters, voltage-controlled oscillators, and ultrafast logic circuits. The speed index, 35.9 mV/ps, is also the highest value reported for any Si-based tunnel diode.

II. Device Design, Growth, and Fabrication

A schematic of the layered device used in this study is shown in Fig. 1(a). Epitaxial growth of the device was achieved by low-temperature molecular beam epitaxy (LT-MBE) growth using elemental Si and Ge in electron-beam sources. The structures were grown on highly resistive Si (100) substrates (3000–8000 $\Omega \cdot cm$). The bulk doping level for both n^+ and p^+ layers was 5×10^{19} cm^{-3}, whereas both the B and P δ-doping sheet carrier concentration was maintained at 1×10^{14} cm^{-2}. The nominally undoped tunneling spacer layer sandwiched between the two δ-doping layers is comprised of two layers, namely, 1) a 1.5-nm layer of undoped $Si_{0.45}Ge_{0.55}$ above the lower B δ-doping layer and 2) a 1-nm layer of undoped Si below the upper P δ-doping layer. The SiGe adjacent to the B δ-doping layer performs two roles, suppressing dopant interdiffusion

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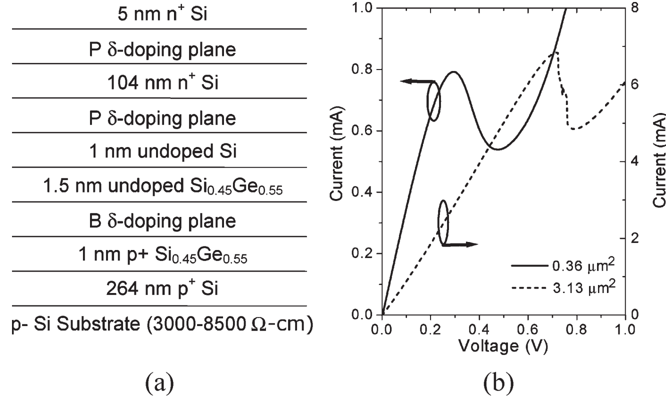

Fig. 1. (a) Schematic of the RITD layer structure used in this study. The upper P δ-doping plane is added to further lower the contact resistance of the Ni-silicide. (b) Measured $I-V$ characteristics of RITDs with different device areas. A weak oscillation in the NDR region occurs for the device with an estimated area of 3.13 μm^2, but is absent for the device with a 0.36-μm^2 area.

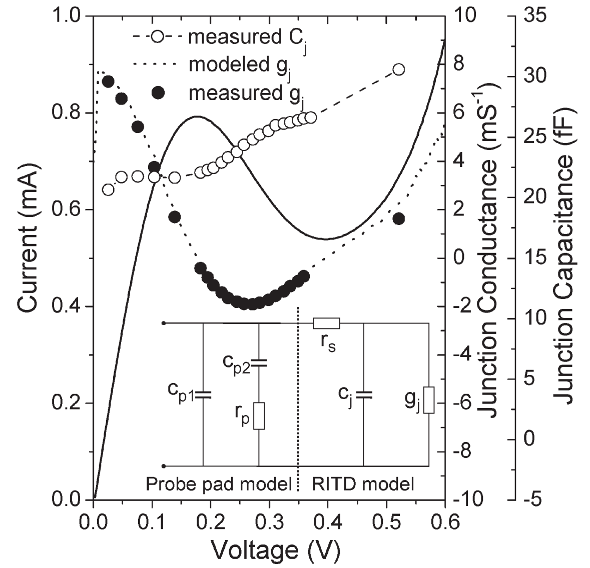

Fig. 2. Extracted g_j and C_j are plotted as a function of junction voltage with the intrinsic dc I–V curve. g_j is also computed directly from the dc I–V characteristics and compared. Very good agreement between the RF modeled and dc measured g_j is obtained. The inset is the small-signal equivalent circuit of the RITD and the probe pad. C_{p1} represents the fringe capacitance, C_{p2} is the metal-to-substrate parasitic capacitance, and r_p is the resistive substrate loss, respectively.

and enhancing tunneling probability by reducing the tunnel barrier and increasing momentum mixing. An additional 1 nm of p$^+$ $Si_{0.45}Ge_{0.55}$ underneath the B δ-doping layer is inserted to suppress B outdiffusion away from the junction, so that the sharp B δ-doping peak can be maintained during the growth and subsequent 1-min postgrowth annealing. Another P δ-doped layer inserted 5 nm below the cap layer during the growth is intended to lower the contact resistance in conjunction with Ni silicidation through this P δ-doped quantum well by rapid thermal sintering.

Prior to device fabrication, portions of the as-grown wafers were rapid thermal annealed (RTA) using a forming gas ambient (N_2/H_2) at 500 °C for 1 min. Annealing temperatures between 400 °C and 600 °C were investigated to determine the optimum annealing condition. Inasmuch as this RITD was designed for ultrahigh PCD, the overall device size and parasitics should be carefully taken into consideration for a valid RF measurement.

To make a valid RF measurement, the tunnel diode should be stable when it is biased in its NDR region. The stability criteria [11] are $R < (V_{\rm valley} - V_{\rm peak})/(I_{\rm peak} - I_{\rm valley})$ and $L/R < C|R_n|$, where R and L are the parasitic series resistance and inductance, respectively. $V_{\rm valley}$ and $V_{\rm peak}$ are the voltages corresponding to the valley current $I_{\rm valley}$ and the peak current $I_{\rm peak}$ of a tunnel diode in its current–voltage I–V characteristics, respectively. C is the junction capacitance, and R_n is the differential resistance dV/dI. Oscillations will take place in the NDR region unless both these two criteria are satisfied. Therefore, an RITD with an ultralarge current density span should have a very small diode size and small series resistance to satisfy the stability criteria.

To realize a very small sized device concurrently with a small series resistance to satisfy the dc stability conditions when the RITD is biased into the NDR region, a one-metal fabrication process [8] and Ni-silicidation process were utilized, resulting in the active mesa area as small as 0.36 μm^2 estimated from the PCD. The first photolithography step defined both anode and cathode contacts, as well as the ground-signal-ground probe pads, by deposition and lift-off of the layered contact of Ni/Cr/Au/Cr (5:200:100:10 nm) using electron beam evaporation. The samples were RTA at 430 °C for 30 s to form a Ni-silicide ohmic contact in the vicinity of the upper P δ-doped plane, which is located 5 nm below the surface. The 200 nm of intermediary Cr is expected to prevent Au from interdiffusing into the silicide during the annealing. An $HF/HNO_3/H_2O$ (1:100:100) solution was used to define the mesa and etch through the tunnel junction. Using photoresist as an etching mask defined with a second photolithography step after first the mesa etching, the second device isolation etching step was performed down to the p-substrate by inductively coupled plasma reactive ion etching (ICP-RIE) with an SF_6/O_2 gas mixture to avoid any unnecessary undercut of the mesa. The final processing step used wet etching again ($HF/HNO_3/H_2O$) to selectively undercut the metal to form an air bridge between the top of the active device and the large signal pad, so that the active device is fully defined and isolated from the large signal pad (refer to [6] for further details).

III. Results and Discussions

Fig. 1(b) shows the measured $I-V$ characteristics at room temperature obtained for two different device sizes, estimated to be 3.13 and 0.36 μm^2, respectively. The sizes of the active area were estimated from the measured PCD of 218 kA/cm^2 of a larger test device (5×5 μm^2), assuming that peak current scales linearly with device area [12]. Recent experiments confirmed that current scales remarkably well with area for diodes of 5 μm diameter and larger. For accurate determination of the PCD using the 5×5 μm^2 control device, the lateral extent (~ 0.5 μm) of the wet etch undercut measured by scanning electron microscopy was taken into account. Weak

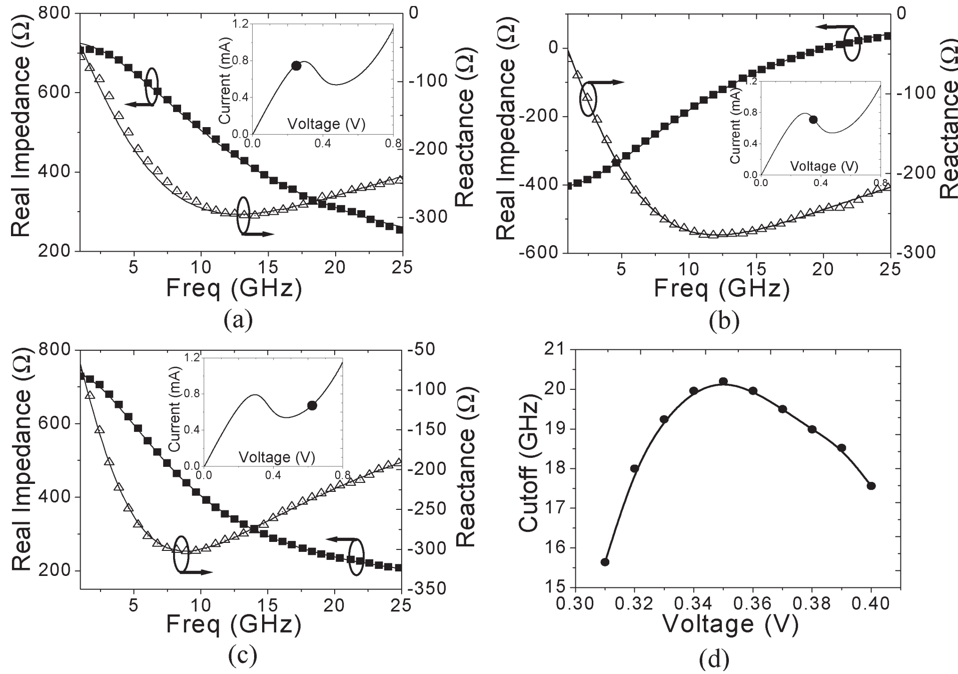

Fig. 3. Measured and modeled impedance of a 0.36-μm^2 RITD are plotted as a function of frequency at (a) 0.25 V, (b) 0.35 V, and (c) 0.62 V, respectively. Inset shows the $I-V$ characteristics of the intrinsic RITD of 0.36 μm^2. (d) Resistive cutoff frequency f_{r0} versus external bias. A resistive cutoff frequency of 20.2 GHz was observed at a 350-mV bias.

self-oscillation-induced steps in the NDR region were observed for the larger device size of 3.13 μm^2, but no evidence of self-oscillations was observed for the smaller sized device with area of 0.36 μm^2. This is because the negative conductance from the smaller device size (0.36 μm^2) is low enough, so that the load-line-induced bistability is eliminated in the NDR region. The PVCR was found to be 1.47 and 1.41 for the devices of areas 0.36 μm^2 and 3.13 μm^2, respectively. The peak voltage shift between the two devices is believed to be due to the different ohmic voltage drop across the two different contact layers created by the 10-fold absolute current difference.

RF measurements of the RITDs were then made, but due to the lack of self-oscillations, the RITD with area of 0.36 μm^2 was examined more completely. The microwave performance of the RITDs was assessed using on-wafer bias-dependent s-parameter measurements from 1 to 25 GHz in the bias voltage range from 0 to 0.62 V in 10- to 50-mV steps. The 50-Ω microwave probe was calibrated by the short-open-load-through method before RF measurements. The signal delivered to the diodes was $\sim$ 10 mV peak-to-peak. The inset in Fig. 2 shows an equivalent small-signal circuit model of the RITD and the probe pads. The probe pad parasitics were determined by fitting the pad circuit model to the measured S11 of an on-wafer open pad test structure using Advanced Design System (ADS) software. C_{p1} and r_p represent the fringe capacitance and resistive substrate loss, respectively. C_{p2} represents the p-n junction capacitance for the signal/ground pad to p-substrate. Then, the de-embedded s-parameters of the RITDs were used to obtain the intrinsic device parameters including series resistance r_s, junction capacitance C_j, and junction conductance g_j by an ADS optimization over the frequency range of 1–25 GHz and at each bias point. The series resistance r_s extracted from RF measurement was independent of bias, with a value of approximately 147 Ω for the device size of 0.36 μm^2, assuming that the contact resistance dominates the series resistance. The estimated specific contact resistivity ρ_c is as low as $5.3 \times 10^{-7}\ \Omega \cdot \mathrm{cm}^2$, which was the result of Ni silicidation through the additional P δ-doped layer. Fig. 2 shows the extracted C_j and g_j as a function of the junction voltage, which was computed by subtracting the voltage drop across r_s from the total external bias voltage such that the junction voltage is equal to the external voltage minus the current times r_s. The I–V characteristic of the intrinsic tunnel diode is then superimposed in Fig. 2 as a solid line along with the calculated g_j obtained by the first derivation of the intrinsic dc I–V characteristics. Very good agreement between the g_j obtained from RF measurements and dc measurements was observed, which suggests that the RITDs are very good in terms of their low-frequency noise mainly stemming from trapping because trapping-involved noise signals, due to its slow physical response, should not correspond to the high-frequency signals.

Fig. 3(a)–(c) shows the measured and modeled impedance of the 0.36-μm^2 RITD consisting of real and imaginary parts as a function of frequency for three different bias points, 250 mV (prepeak region), 350 mV (NDR region), and 620 mV (post-valley region), respectively. The insets in each figure represent three different bias points on the $I-V$ characteristics of the RITD. Good agreement between the measured impedance and the modeled impedance indicates the equivalent circuit model shown in Fig. 2(a), which fully describes the physical processes of signal flow. When the device is biased at the NDR region [Fig. 3(b)], the real part of the impedance is negative at the lower frequencies, resulting in a positive gain

up to the cutoff frequency in the reflected signal $(20\log_{10}\Gamma)$. Bias-dependent f_{r0} for the RITD with a 0.36-μm^2 area is plotted in Fig. 3(d). With a bias of 350 mV, the RITD exhibits an f_{r0} of 20.2 GHz, which is $\sim$ 3.6 times higher than the currently reported values [6]. Compared with [6], this improvement is mainly due to the reduced junction capacitance $(\sim 12\times)$ from the lateral scaling of the device area and increased junction conductance due to the higher current density of an RITD. The reduced specific contact resistivity $(\sim 4\times)$ from Ni silicidation through the P δ-doped layer also contributes to the improved device performance because $\sim 10\times$ smaller device size only results in a $\sim$ 2.4 times increase of r_s. To the authors' knowledge, this is the highest f_{r0} ever reported for any epitaxially grown Si-based tunnel diode. The speed index can be calculated as the quotient of peak current over capacitance, $s = I_p/C_j = 0.79$ mA$/22.06$ fF $= 35.9$ mV/ps, which is also the highest value ever reported for any epitaxially grown Si-based tunnel diode.

IV. Conclusion

In this study, the Si-based RITDs grown by LT-MBE were demonstrated to have a resistive cutoff frequency f_{r0} of 20.2 GHz with a PCD of 218 kA/cm^2, a speed index of 35.9 mV/ps, and a PVCR of 1.47. A specific contact resistivity of $5.3 \times 10^{-7}\ \Omega \cdot \text{cm}^2$ is achieved by inserting a P δ-doped quantum well in the contact layer during the growth followed by an Ni-silicidation process by RTA with 430 °C for 30 s. The resulting devices are very good candidates for RF high-power mixed-signal applications. The device structures presented here are compatible with a standard CMOS or HBT process.

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