P and B doped Si resonant interband tunnel diodes with as-grown negative differential resistance

P.E. Thompson, G.G. Jernigan, S.-Y. Park, R. Yu, R. Anisha, P.R. Berger, D. Pawlik, R. Krom and S.L. Rommel

Robust Si resonant interband tunnel diodes have been designed and tested that demonstrate as-grown negative differential resistance at room temperature with peak-to-valley current ratios (PVCR) up to 2.5 and peak current densities in the order of 1 kA/cm^2. The as-grown Si p^+in^+ structures were synthesised using solid source molecular beam epitaxy, incorporating B and P δ-doped layers. Both structures have shown thermal stability after 1 min post-growth anneals up through 675°C and the PVCR improves to 2.8 for a 575°C 1 min anneal.

Introduction: A driving force in electronic device research has been increased functionality and density with reduced energy losses. One of the techniques proposed for meeting these goals has been the employment of tunnel diodes integrated with conventional transistors to form compact and low-power memory, logic and mixed-signal circuits. Considerable progress has been made in the area of Si-based resonant interband tunnel diodes (RITDs). Discrete RITDs have been reported that have a peak-to-valley current ratio (PVCR) greater than 6 [1], peak current densities (PCD) greater than 218 kA/cm^2 [2], and voltage swings, V_s, greater than 560 mV [3]. All of these devices have features in common: 1) the electron tunnelling occurs between bound states in the valence band and the conduction band created by highly-doped layers formed by δ-doping; 2) a spacer layer between the two δ-doped layers which includes $Si_{1-x}Ge_x$ to reduce the bandgap and reduce the out-diffusion of dopants from the B δ-doped layer; 3) epitaxial growth at low temperature to reduce both the diffusion of dopants and the segregation of constituents during the growth; and 4) a post-growth anneal to reduce the effect of point defects which occur due to the low temperature epitaxial growth.

In particular, room temperature RITD performance has been shown to be sensitive to Ge concentration [4], the width of the spacer layer [5] and to the temperature of the post-growth anneal [1, 3, 4]. In spite of the narrow process windows, SiGe RITDs have been successfully integrated with both complementary metal oxide semiconductor (CMOS) transistors [6] and heterojunction bipolar transistors (HBT) [7] to form elementary logic circuits. The ease of integration of the RITD would be enhanced if they could be fabricated using only Si, without the added complication of the critical thickness constraints and residual strain of SiGe spacers or the requirement of post-growth anneal. In this Letter, we report the formation of discrete Si RITDs that are designed and fabricated so that neither a Ge alloy layer nor a post-growth anneal is required to obtain a Si tunnel diode suitable for integration. In addition, the thermal stability of the Si-RITDs are investigated in the temperature interval 500 to 675°C, since the devices may be exposed to these temperatures during integrated circuit fabrication, such as the formation of ohmic contacts.

Experimental: Two device structures were investigated, shown in Fig. 1. As noted in the Figure, there are many common features including substrate type, growth initiated at 650°C prior to growth of the B-doped buffer layer at 500°C, B δ-doping at 10^{14}/cm^2, P δ-doping at 10^{14}/cm^2, 320°C substrate temperature for the low temperature epitaxial growth, and a 6 nm intrinsic Si tunnel spacer width. The nominal 6 nm spacer width was chosen for ease of electrical testing, with the knowledge that the results could be directly applied to devices with much thinner barriers for RF applications or much wider barriers for memory applications. The n^+ and p^+ doping concentrations were 5×10^{19}/cm^3. The elements differentiating the two structures studied occur after the deposition of the primary P δ-doped layer. In structure 'A' the substrate growth temperature is maintained at 320°C to minimise the P segregation and B diffusion. The top contact layer is comprised of three additional P δ-doped layers separated by 2.5 nm n^+ Si followed by a 17.5 nm n^+ Si layer to minimise the series resistance at the top contact. In structure 'B' the substrate growth temperature is maintained at 320°C while growing 5 nm of nominally undoped Si to trap the segregating P. The substrate temperature is raised to 550°C (without growth for 3 min) and 70 nm of additional undoped Si is grown. This technique exploits the fact that the surface segregation of P increases by more than an order of magnitude in raising the substrate from 320 to 550°C [8], and effectively sweeps the excess P to the growing surface, sharpening the P δ-layer below and providing a low resistance surface contact layer. Devices were fabricated using standard lithographic techniques. Ti/Au dots formed the front contact along with a Ti/Au backside contact. The RITDs were mesa (18 µm diameter) isolated.

'A'	'B'
17.5 nm n^+ Si 320°C	30 nm n^+ Si 550°C
multi-P-δ-doped contact layer	70 nm Si spacer 550°C
100 nm n^+ Si 320°C	5 nm Si spacer 320°C
P δ-doped 10^{14} cm^{-2}	P δ-doped 10^{14} cm^{-2}
6 nm Si spacer 320°C	6 nm Si spacer 320°C
B δ-doped 10^{14} cm^{-2}	B δ-doped 10^{14} cm^{-2}
250 nm p^+ buffer 500°C	250 nm p^+ buffer 500°C
Si p^+ substrate	Si p^+ substrate
a	*b*

Fig. 1 *Schematic diagrams of simplified RITD structures*

RITD 'A' was designed to minimise dopant segregation and diffusion during growth and reduce contact resistance by employment of multiple P δ-doping layers

RITD 'B' was designed to exploit P surface segregation during growth to sharpen P δ-doping and reduce the contact resistance

Results and discussion: The room temperature current–voltage (I–V) characteristics of the as-grown RITDs are presented in Fig. 2. On each sample the device-to-device variation in measured current was less than 20% and the variation in the PVCR was less than 10%. The as-grown RITD 'A' a has a PVCR of 2.1, PCD of 0.92 kA/cm^2, and V_s of 0.5 V, while as-grown RITD 'B' has a PVCR of 2.5, PCD of 1.5 kA/cm^2, and V_s of 0.5 V. This is the first report of an as-grown RITD, using P as the n-type dopant, having negative differential resistance (NDR). It must be noted that Jorke *et al.* [9] in their study of the forward-bias characteristics of Si bipolar junctions observed NDR in an as-grown p^+in^+ mesa diode with a 5 nm intrinsic spacer, where the n^+ Sb-doped emitter layer ($N_{Sb} = 10^{20}$/cm^3) was grown at 325°C. Its room temperature I–V characteristic demonstrated a PVCR of 2.2, PCD of 0.65 kA/cm^2, and V_s of 0.5 V. However, Sb is notoriously difficult to incorporate into the Si lattice, having a surface segregation ratio more than 10× larger than P in this temperature range [8, 10], and so P is more suitable as the n-type dopant for integrated circuit fabrication.

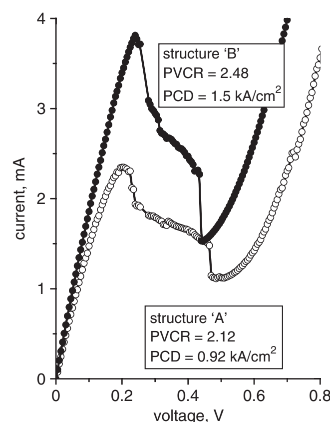

Fig. 2 *I–V characteristics of 18 mm diameter RITD fabricated without post-growth anneal*

Both devices demonstrate NDR

Since the goal of this investigation is to design a Si RITD that can easily be incorporated into an integrated circuit, we have determined the thermal stability of each epitaxial structure by subjecting it to a 1 minute anneal at a temperature, T, which ranged from 500 to 675°C

Authorized licensed use limited to: The Ohio State University. Downloaded on July 13, 2009 at 13:30 from IEEE Xplore. Restrictions apply.

(Fig. 3). Both samples show a maximum PVCR after a 1 min anneal at 575°C with samples 'A' and 'B' reaching 2.7 and 2.8, respectively. The PCD increased steadily with anneal temperature. The increase in the PVCR is due to the reduction of the excess current from the annealing out of some of the point defects. The increase in the PCD of sample 'A' is most likely due to the point defect-assisted diffusion of B, effectively reducing the barrier width. After the 675°C anneal, sample 'A' had a PCD of 3.1 kA/cm^2 and sample 'B' had a PCD of 2.2 kA/cm^2, both had a PVCR > 2. Thus, both RITD designs have a sufficient thermal budget to withstand an integrated circuit fabrication process such as silicide formation, to be performed after the growth.

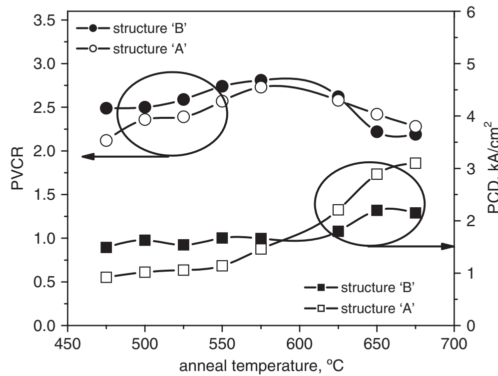

Fig. 3 *PVCR and PCD of RITDs fabricated on epitaxial structures after 1 min anneals*

Conclusion: Two Si $p^{+}in^{+}$ RITDs were designed and fabricated using MBE. The simplified designs of both RITDs do not employ SiGe alloys nor do they require a post-growth anneal. The electrical characteristics of both RITDs are very similar. However, structure 'B', which employs a final growth temperature of 550°C, has a higher PVCR and a PCD that shows less variation with temperature, and hence should be easier to incorporate into an integrated circuit design.

Acknowledgments: The work done at the Ohio State University and the Rochester Institute of Technology was supported by the National Science Foundation. The work performed at the Naval Research Laboratory was supported by the Office of Naval Research.

© The Institution of Engineering and Technology 2009
10 April 2009
doi: 10.1049/el.2009.1007

P.E. Thompson and G.G. Jernigan (*Code 6812, Naval Research Laboratory, Washington, DC 20375, USA*)

E-mail: phillip.thompson@nrl.navy.mil

S.-Y. Park, R. Yu, R. Anisha and P.R. Berger (*Department of Electrical & Computer Engineering, The Ohio State University, Columbus, OH 43210, USA*)

D. Pawlik, R. Krom and S.L. Rommel (*Microelectronic Engineering Department, Rochester Institute of Technology, Rochester, NY 14623, USA*)

P.R. Berger: Also with the Department of Physics, The Ohio State University, Columbus, OH 43210 USA

References

1 Duschl, R., and Eberl, K.: 'Physics and applications of Si/SiGe/Si resonant interband tunneling diodes', *Thin Solid Films*, 2000, **380**, pp. 151–153

2 Chung, S.-Y., Yu, R., Jin, N., Park, S.-Y., Berger, P.R., and Thompson, P.E.: 'Si/SiGe resonant interband tunnel diode with f_T 20.2 GHz and peak current density 218 kA/cm^2 for K-band mixed-signal applications', *IEEE Electron Device Lett.*, 2006, **27**, (5), pp. 364–367

3 Chung, S.-Y., Jin, N., Pavlovicz, R.E., Berger, P.R., Yu, R., and Thompson, P.E.: 'Analysis of the voltage swing for logic and memory applications in Si/SiGe resonant interband tunnel diodes grown by molecular beam epitaxy', *IEEE Trans. Nanotechnol.*, 2007, **6**, (2), pp. 158–163

4 Duschl, R., Schmidt, O.G., Reitemann, G., Kasper, E., and Eberl, K.: 'High room temperature peak-to-valley current ratio in Si based Esaki diodes', *Electron. Lett.*, 1999, **35**, (13), pp. 1111–1112

5 Jin, N., Chung, S.-Y., Yu, R., Heyns, R., Berger, P.R., and Thompson, P.E.: 'The effect of spacer thickness on Si-based resonant interband tunneling diode performance and their applications to low power tunneling diode SRAM circuits', *IEEE Trans. Electron Devices*, 2006, **53**, (9), pp. 2243–2249

6 Sudirgo, S., Nandgaonkar, R.P., Curanovic, B., Hebding, J.L., Saxer, R.L., Islam, S.S.W., Hirschman, H.D., Rommel, S.L., Kurinec, S.K., Thompson, P.E., and Berger, P.R.: 'Monolithically integrated Si/SiGe resonant interband tunnel diode/CMOS logic elements demonstrating low voltage MOBILE operation', *Solid-State Electronics*, 2004, **48**, pp. 1907–1910

7 Chung, S.-Y., Park, S.-Y., Daulton, J., Yu, R., Berger, P.R., and Thompson, P.E.: 'Integration of Si/SiGe HBT and Si-based RITD Demonstrating Controllable Negative Differential Resistance for Wireless Applications', *Solid-State Electron.*, 2006, **50**, (6), pp. 973–978

8 Thompson, P.E., and Jernigan, G.G.: 'Determination of the surface segregation ratio of P in Si(100) during solid-source molecular beam epitaxial growth', *Semicond. Sci. Technol.*, 2007, **22**, S80–S83

9 Jorke, H., Kibbel, H., Strohm, K., and Kasper, E.: 'Forward-bias characteristics of Si bipolar junctions grown by molecular beam epitaxy at low temperatures', *Appl. Phys. Lett.*, 1993, **63**, (17), pp. 2408–2410

10 Hobart, K.D., Godbey, D.J., Twigg, M.E., Fatemi, M., Thompson, P.E., and Simons, D.E.: 'Surface segregation and structure of Sb-doped Si(100) films grown at low temperature by molecular beam epitaxy', *Surf. Sci.*, 1995, **334**, pp. 29–38

Authorized licensed use limited to: The Ohio State University. Downloaded on July 13, 2009 at 13:30 from IEEE Xplore. Restrictions apply.