90 nm 32 × 32 bit Tunneling SRAM Memory Array With 0.5 ns Write Access Time, 1 ns Read Access Time and 0.5 V Operation

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***Abstract*—Functional robustness is one of the primary challenges for embedded memories as voltage levels are scaled below 1 V. A low-power high-speed tunneling SRAM (TSRAM) memory array including sense amplifiers and pre-charge circuit blocks operating at 0.5 V is designed and simulated using available MOSIS CMOS 90 nm product design kit coupled with VerilogA models developed from this group's Si/SiGe resonant interband tunnel diode experimental data. 1 T and 3 T- 2 tunnel diode memory cell configurations were evaluated. The memory array assigns 0.5 V as a logic "1" and 0 V as a logic "0". Dual supply voltages of 1 and 0.5 V and dual threshold voltage design are used to ensure high sensing speed concurrently with low operating and standby power. Read access time of 1 ns and write access time of 2 ns is achieved for the 3 T memory cell. Write access time can be reduced to 0.5 ns for 32 bit write operations not requiring a preceding read operation. Standby power dissipation of 6×10^{-5} mW per cell and dynamic power dissipation of 1.8×10^{-7} mW/MHz per cell is obtained from the TSRAM memory array. This is the first report of TSRAM performance at the array level.**

***Index Terms*—Embedded memory, low power memory, negative differential resistance (NDR), resonant interband tunnel diodes, tunnel diodes, tunnel static random access memory (SRAM).**

I. Introduction

As outlined in the 2007 ITRS roadmap, two key challenges for future IC technology are pushing CMOS beyond its ultimate scaled density and functionality and expanding information processing beyond that attainable by CMOS alone, using new devices and architectural approaches. Quantum tunneling based devices (e.g., resonant tunneling diodes and resonant interband tunnel diodes) are extremely high speed devices with a unique negative differential resistance (NDR) characteristic. NDR circuits generally operate below 0.5 V which is a key goal to reduce power consumption. Power consumption is generally related to the square of the voltage. The folded I-V characteristics of an NDR device pair creates a simple latch that when used in conjunction with transistors enables novel circuit configurations for logic, mixed signal and compact low-power embedded memory [1]–[6].

Ultra-low power operation is the dominant issue for embedded memories with the ever-increasing memory power consumption relative to the rest of the components on chip. Embedded memory is dominated by static random access memory (SRAM). As technology is scaled to improve speed and area, process variations are making functional robustness the primary challenge in memory design [7], [8]. This is further exacerbated by the need to scale voltages to lower power consumption in a growing mobile market.

Both active and standby power reduction needs to be addressed. Recent SRAM memory architectures incorporate a low-power idle state where the power supply voltage is either reduced or the memory arrays are powered down during standby [9]. This lessens the criticality of low standby power. On the other hand, the demand upon active power is increasing as more functionality is built into mobile devices. Voltage scaling enables active power reduction and is also essential to maintain logic compatibility.

A very low power consumption with tunneling based static random access memory (TSRAM) cell was proposed and demonstrated by Van der Wagt *et al.* for a resonant tunnel diode (RTD)/HFET integration using InP-based technology [5]. More recently, the first Si-based TSRAM implementation was realized using a 2 μm CMOS process that integrated nMOS with SiGe resonant interband tunnel diodes with operation below 0.5 V [10]. Other fabricated TSRAM memory cells have also been reported but are restricted to single memory cell implementation [11], [12]. Large scale manufacture of a TSRAM memory in a standard CMOS process flow requires a compatible growth technique. Recently Si/SiGe tunnel diodes fabricated with chemical vapor deposition has been demonstrated which can be used to produce high quality devices over large wafers with batch processing [13]. However extra process steps are required for a full chip fabrication and industry resistance have stymied implementation in a standard CMOS process line. To date, simulation results for TSRAM have been limited to SPICE simulations of single memory cells [11], [14]. To fully evaluate TSRAM performance and robustness to process variations

Manuscript received April 02, 2010; revised July 28, 2010, October 08, 2010, and December 18, 2010; accepted February 03, 2011. Date of publication April 05, 2011; date of current version September 28, 2011. This paper was recommended by Associate Editor M. Anis.

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Digital Object Identifier 10.1109/TCSI.2011.2123630

and make a fair comparison to current embedded memory solutions, post-layout simulation is essential, which should lower the barrier for its commercial adoption.

In this paper a resonant interband tunnel diode (RITD) device is integrated into the Cadence electronic design automation (EDA) tool and a 32 bit × 32 bit tunneling SRAM memory array is simulated using the 90 nm technology design kit provided by MOSIS. The RITD device model is implemented using VerilogA. The process development kit has been modified to include new layers for tunnel diode definition, design rule checks (DRC) and layout versus schematic (LVS) rules to enable parasitic extraction and post layout simulation. Parasitic extraction is done using the Calibre xRC tool, utilizing a distributed resistance-capacitance-coupling capacitance model, to more accurately model bitline and wordline parasitics. The prospects and requirements of NDR devices for TSRAM to be a viable alternate to present embedded memory technology are then determined, and a platform created for insertion of alternate tunnel diode models using different material systems and structures. The nominal supply voltage assumed for this technology is 1 V. However, a dual voltage design was implemented with mixed 0.5 and 1 V operation. Dual threshold voltage, $V_{\rm th}$, technique was used to obtain low sub-threshold leakages in the memory cell (high $V_{\rm th}$) while concurrently allowing faster sensing speed and 0.5 V operation (low $V_{\rm th}$).

This paper is organized as follows. Section II provides details of the RITD device structure, model, and memory cell structure. Section III discusses the cell layout. Section IV describes the memory architecture. Section V presents the memory array performance in terms of speed, power and robustness to process variation. Finally a brief summary and conclusion is provided in Section VI.

II. Device and Memory Cell Structure

A. Device Structure and Model

The device model is based on the highest peak-to-valley current ratio (PVCR) Si/SiGe resonant interband tunnel diode (RITD) reported by this group [15] and similar designs have reported room temperature PVCR of more than 6 [16]. The device structure is shown in Fig. 1(a) and its calculated band diagram is shown in Fig. 1(b). It consists of n-type and p-type δ-doped layers which together with Si/SiGe valence band offsets form two adjacent quantum wells (QW); one QW contains holes while the other QW holds electrons. The tunneling barrier or spacer layer between the two wells consists of a composite of 4 nm Si/4 nm SiGe. This tunneling spacer thickness is one design variable to alter the current density. The SiGe cladding layers surrounding the Boron δ-doped layer suppresses Boron out-diffusion during growth and post-growth anneal [17]. The PVCR of this RITD device was reported as 4.02 at room temperature with a peak current density of 129 A/cm^2. The experimentally obtained dc characteristics are shown in Fig. 1(c).

The RITD is modeled as a capacitor in parallel with a voltage controlled current source as shown in Fig. 2(a). The current source represents the nonlinear dc current of the RITD and is

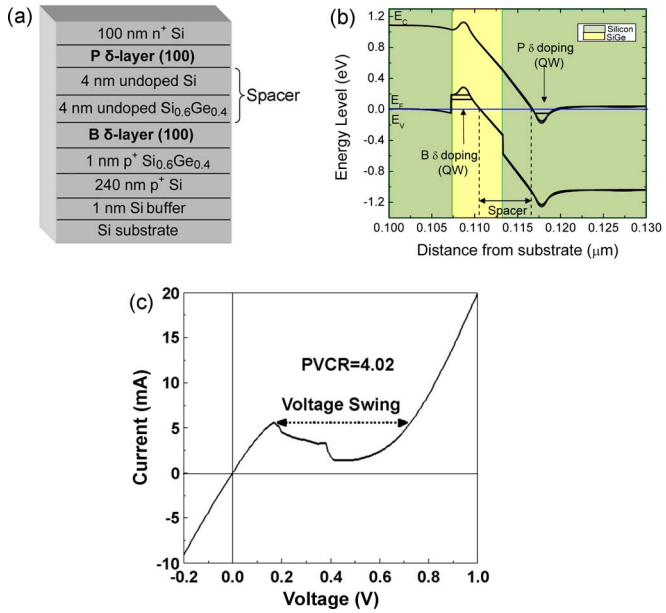


Fig. 1. (a) Schematic diagram of the 4 nm Si/4 nm SiGe RITD test structure. (b) Band-diagram showing the quantum wells formed due to delta doping. (c) I-V characteristics of a representative Si/SiGe RITD.

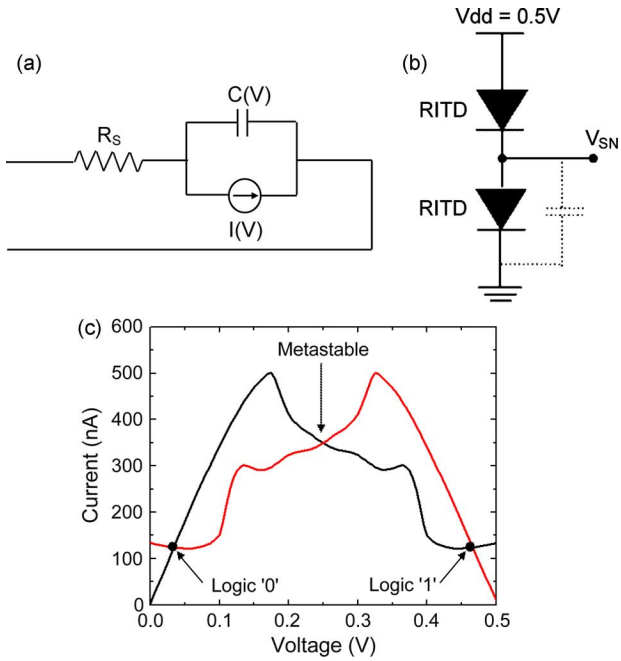


Fig. 2. (a) Small signal AC model of an RITD. (b) Two series connected RITDs and (c) its I-V characteristics showing latching action.

modeled using a polynomial fit to the measured dc I-V characteristics. A junction capacitance of 15.4 fF/μm^2 has been obtained experimentally for a 6 nm spacer thickness RITD based upon a small signal model fit to measured S-parameters [18]. Assuming the capacitance is given simply by a parallel plate capacitor $\varepsilon A/d$ where d is the tunneling spacer thickness, ε is the permittivity and A is the device area, the junction capacitance for an 8 nm spacer thickness would be 11.6 fF/μm^2 approximately, normalized per unit area. The voltage swing, defined as the difference between the peak voltage and the projected peak

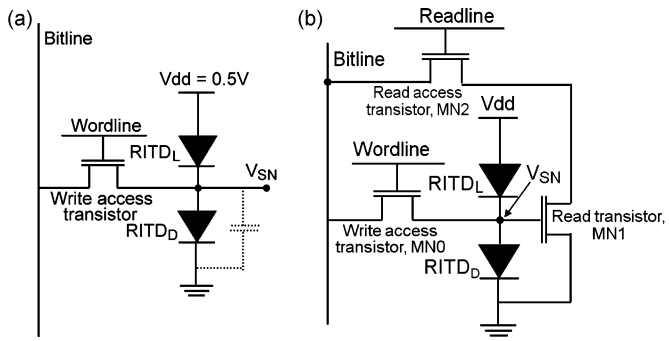


Fig. 3. Possible memory cell configurations for a Tunneling SRAM. (a) 1 T-2 RITD. (b) 3 T-2 RITD memory cell.

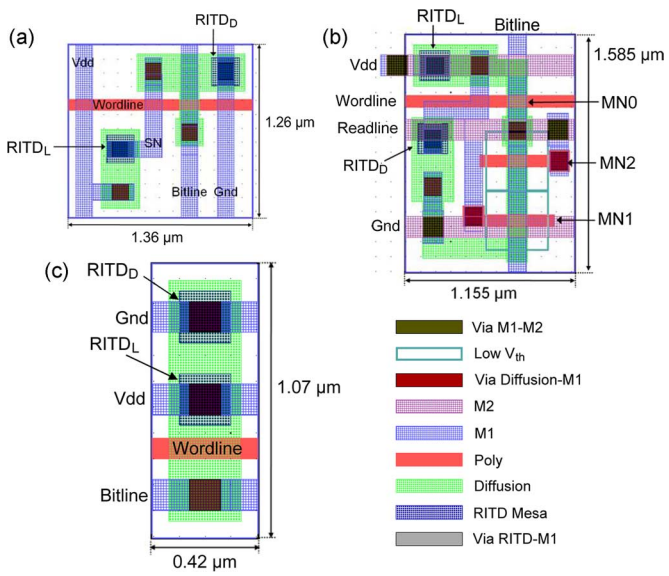


Fig. 4. Layout of (a) 1 T-2RITD memory cell, (b) 3 T-2 RITD memory cell, and (c) 1 T-2RITD memory cell with back to back RITDs.

voltage, is assumed to be invariant with scaling. The model is implemented using VerilogA.

B. Memory Cell Structure

A pair of NDR devices connected in series act as a latch when accessing the central node's voltage $V_{\rm SN}$. Fig. 2(b) shows two serially connected NDR devices and their DC I-V characteristics for a bias voltage $V_{\rm DD}$ of 0.5 V [see Fig. 2(c)]. A bias of 0.5 V is chosen, since it gives the minimum latch current value, resulting in a "1" state corresponding to 0.47 V and "0" state corresponding to 34 mV. A memory cell is realized by adding a pass transistor for cell addressability as shown in Fig. 3(a). TSRAM operation is similar to conventional DRAM with the latching action eliminating the need for a refresh as long as the peak current is larger than the leakage current through the transistor and the valley current.

Two possible memory cell configurations were considered, a 1 T cell and a 3 T cell. The write operation in both cases is similar to DRAM. The data to be written is applied to the bitline and the wordline is activated to select the memory cell to be written. The read operation for the two topologies is described below.

For the 1 T cell, the read operation is also similar to a DRAM. Charge sharing between the storage node capacitance and the bitline capacitance results in a small change in the bitline voltage which is sensed by the sense amplifier. The capacitance at the storage node SN [see Fig. 3(a)] is due to the parasitic capacitance of the two tunnel diodes and the drain-bulk capacitance of the transistor. For a sufficient voltage to develop on the bitline, the node capacitance value should be similar to the storage capacitance in a DRAM cell. 1 T DRAM cell with storage capacitance smaller than 10 fF have been demonstrated [19]. RITD capacitance can be tuned by scaling tunneling spacer thickness [20]. The capacitance can be varied from 15.4 to 65.3 fF/μm^2 for a spacer thickness variation from 6 to 3 nm. However as the transistor and tunnel diode sizes are scaled down, the node capacitance also reduces proportionately. Hence an external capacitor would be required. The read operation is destructive in this case and a writeback after read is required.

The 3 T cell approach avoids the use of this capacitor and provides scalability. The 3 T memory cell is shown in Fig. 3(b). Here a read transistor is added to the memory cell, which is driven by the bit state stored on the cell. A "1" stored in the memory cell turns "ON" the transistor while a "0" stored keeps the read transistor in "OFF" state. The state of the read transistor can be used to detect the bit stored. A third read access transistor is connected between the read transistor and bitline to enable addressability. The read operation is thus non-destructive and does not degrade the voltage stored on the bit cell which is a growing concern for SRAM-based operation. This TSRAM approach is similar to the 8 T SRAM cell design which is being considered as an alternative design to cope with threshold voltage variations as voltage levels are scaled [21].

III. Memory Cell Layout

Fig. 4(a) and (b) show the layout of a 1 and 3 T TSRAM memory cell respectively implemented using the 90-nm technology provided by MOSIS. It should be noted that the layout rules used here are logic design rules, which are conservative as applicable to logic circuits and prevent optimization of area as is generally done for a memory cell. Nevertheless, the cell area for the 1 T configuration is 1.72 μm^2 while for a 3 T TSRAM is 1.83 μm^2 which is slightly larger than that reported for an SRAM cell for the same technology (1.25 μm^2) [22]. To place this in context a cell area of 1.96 μm^2 has been obtained for an SRAM cell using logic design rules [23]. The cell area can be greatly reduced by implementing back-to-back RITD's resulting in symmetric I-V characteristics, eliminating the need of a bottom contact. In this case both the RITD's can be integrated on top of the source/drain for a very compact cell design. Fig. 4(c) shows a 1 T-2RITD implementation using back to back tunnel diodes which has an area of only 0.449 μm^2.

The RITD-CMOS fabrication process is as follows [10]. The entire CMOS process flow is implemented, but fabrication is halted before any metallization. Then n+ active areas are defined where the RITDs will be grown. One extra mask level needs to be added to define the oxide openings where the RITD will be placed. The RITD can then be added into this region via an epitaxial growth using either molecular beam epitaxy (MBE) [10] or chemical vapor deposition (CVD) [13]. To achieve the

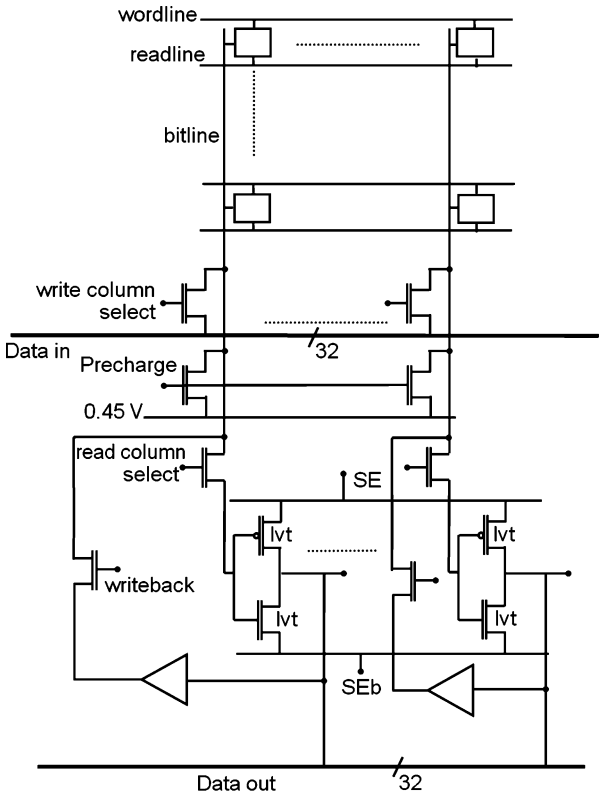


Fig. 5. Memory architecture used for the 32 × 32 memory array using 3 T memory cell configurations showing the sense amplifier (inverter activated by SE and SEb signals) and writeback circuit for read-before-write operation.

narrow δ-doping spikes with degenerate doping neither process is likely to be selective in deposition, but instead will probably lead to polycrystalline material deposited atop an oxide layer in regions where the RITD is undesired. Another mask level is needed to define the RITD mesa. Finally metallization is completed taking care to stay within the thermal budget of the RITD to avoid δ-doping redistribution. Two contacts are defined for the RITD. The top contact is placed on top of the RITD mesa and bottom contact is made to the n+ active area.

The RITD mesa area is 200 nm × 200 nm. This is the minimum area taking into account the via size and tolerance for the chosen technology. To layout the device using Cadence's Virtuoso, two new layers are introduced corresponding to mesa definition and metal 1 contact to the top of the device by modifying the technology file. DRC and LVS rules are also added for the new device.

IV. Memory Architecture

The 32 × 32 bit memory array using 3 T memory cell architecture was designed and simulated. The memory architecture is as shown in Fig. 5. Single ended writing and sensing scheme is used eliminating the need for differential signal generation. With voltage scaling, differential sensing becomes more unreliable with leakage current from unaccessed cells causing variation on the reference bitline. Hence single-ended sensing is utilized here. However a differential sensing scheme can also be used similar to the mid-point sensing used in DRAM. Control signals such as wordline, readline, writeback and column select

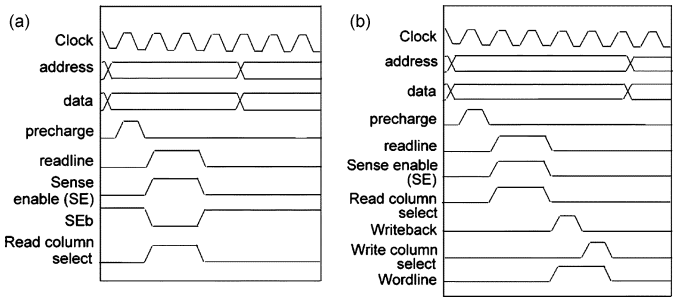


Fig. 6. Timing diagram for (a) read cycle and (b) write cycle.

are 1 V. Since logic "1" corresponds to 0.5 V, NFET transistors can be used efficiently as pass transistors without the need of complementary pass transistor logic or word bootstrapping.

A. Read Cycle

The timing diagram for read cycle is shown in Fig. 6(a). The bitline is precharged to a voltage of 0.45 V. The choice of the precharge voltage is an important design parameter. It should be high enough to be detected as a "1" by the sense amplifier during a read "0" operation. However an upper limit is set by the time required to discharge the bitline during a read "1" operation.

Readline and read-select are activated to select the memory cell to be read. The read transistor is ON/OFF depending on a high/low stored in the memory cell. The bitline is driven low if the read transistor is on and hence a "1" stored on the memory cell and remains at the precharge voltage if the read transistor is off and hence a "0" stored on the memory cell. The bitline drives an inverter that acts as a sense amplifier (SE). The sense amplifier is enabled by applying 0.7 V to SE and 0 V to SEb. Low $V_{\rm th}$ transistors are used to realize the sense amplifier to permit fast sensing. A "0" instead of $V_{\rm dd}$ is chosen to drive the read transistor since the NFET is effective at passing a "0" but charges the output to $V_{\rm SN} - V_{\rm th}$ in case of a high input.

B. Write Cycle

The timing diagram for a write cycle is shown in Fig. 6(b). The write operation is preceded by a read operation to prevent data loss from memory cells along the selected row, but on unselected columns, by being over written when the wordline is enabled. The writeback circuit consists of a buffer that drives the data read out from the sense amplifier onto the bitline, thus precharging the bitline with the data stored in the cells of the selected row before the wordline is activated. Next, the data to be written is inputted from the I/O line by selecting the write column select and the wordline is pulled high to write data into the memory cell.

V. Results

Simulations are performed on the memory core, including the memory cell array, precharge, and sensing circuits which are the primary design issues when using the new TSRAM memory cell architecture and 0.5 V operation. The rest of the memory design would be close to a standard SRAM implementation for the given node and hence is not considered here. Minimum sized NFETs were used for the memory cell. The tunnel diode peak

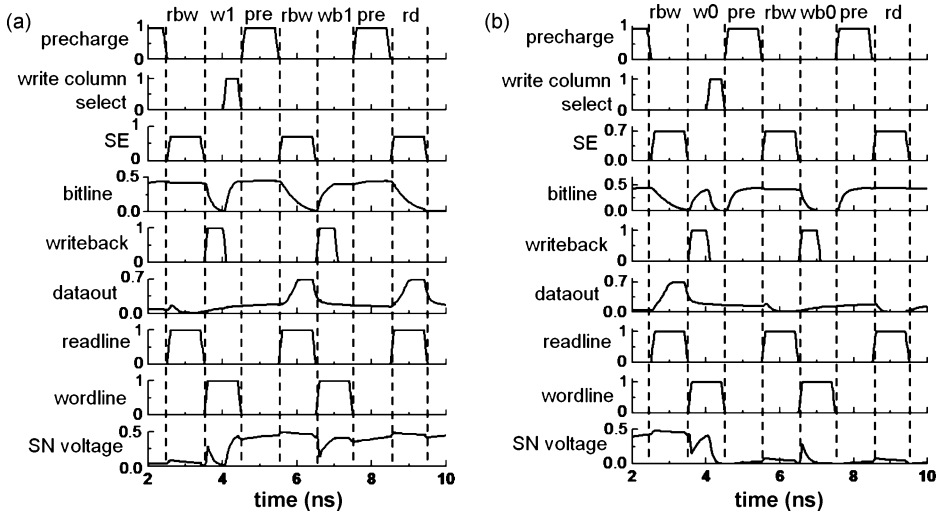


Fig. 7. Simulated waveforms for (a) read/write "1" and (b) read/write "0" operations. rbw = read before write, $\mathrm{w1}$ = write "1", pre = precharge cycle, $\mathrm{wb1}$ = writeback "1", rd = read cycle, $\mathrm{w0}$ = write "0", $\mathrm{wb0}$ = writeback "0".

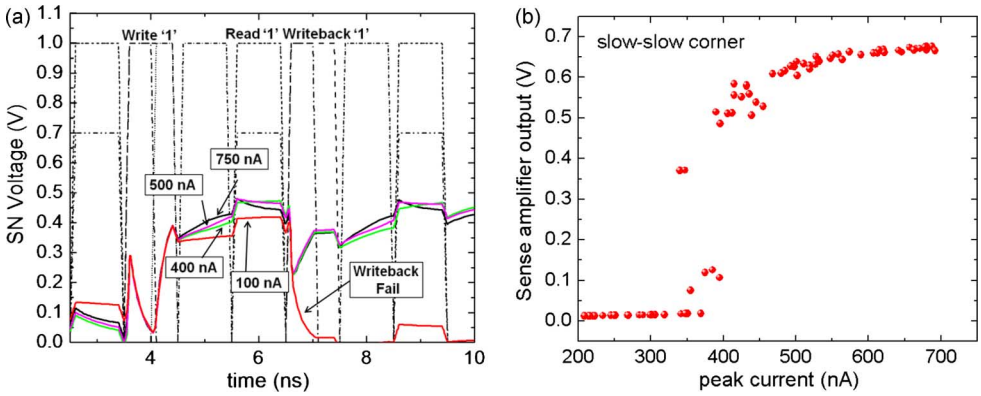


Fig. 8. Simulated waveforms of (a) storage node output voltage for peak current of 750, 500, 400, 100 nA and PVCR of 4.02. Also overlapped are the control signals generated during each clock cycle. (b) sense amplifier output voltage variation with peak current showing read "1" failure below 400 nA.

current is 500 nA with a PVCR of 4. The choice of peak current is discussed in Section V-B.

A. Read/Write Cycle

Read/write operations for typical performance are shown in Fig. 7. Fig. 7(a) illustrates a write "1" operation to a cell previously storing a "0". The bitline is precharged to 0.45 V. A read operation is performed prior to write to facilitate writeback by pulling the readline and column read select high. Next the wordline and writeback signals are activated to writeback the data. The wordline is maintained high while deactivating the writeback and activating the column write select to write data into the cell. A precharge-read-writeback operation is then performed illustrating successful write, read and writeback for logic "1". Fig. 7(b) shows analogous results for a write "0" operation. The write access time, which includes the read, writeback, and write times, is 2 ns. The read access time is 1 ns. For 32 bit word read/write operations the need to writeback is eliminated and the write access time in this case is 0.5 ns.

B. NDR Device Peak Current Requirement

The peak current of a NDR device is inversely proportional to the tunneling barrier thickness for a given device area. For an RITD the tunneling barrier can be varied by tuning the spacer thickness allowing tailorability of peak current [20]. Using empirical fitting, the relation between current density (J_P) and spacer thickness (W) for an RITD was determined to be $J_P = 2.441 \cdot 10^5 \cdot \exp(-0.8081 \cdot W)$. The effect of peak current on circuit performance is shown in Fig. 8. For currents lower than 400 nA a read "1" failure occurs in the slowNFET-slowPFET corner. The reason for the dependence is as discussed below.

Glitches occur at the storage node when the wordline goes low. This is due to charge injection from the access transistor onto the storage node capacitor [24], [25]. This is confirmed by adding a dummy transistor between the access transistor and the storage node as shown in Fig. 9(a). The dummy transistor is an NFET transistor with its area set to half of the access transistor (assuming half of the channel charge moves to source end and half to drain end) with drain and source shorted. The dummy transistor is turned on when the wordline is pulled low (non-overlapping clock) and absorbs the channel charge preventing a change in the storage node charge [see Fig. 9(b)].

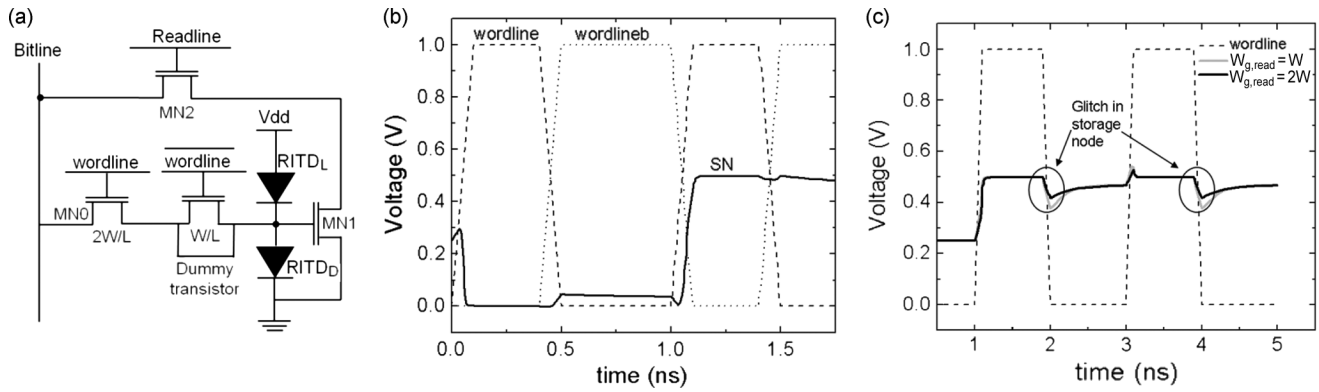


Fig. 9. (a) 1 T-2RITD memory cell with dummy transistor. (b) Simulated waveforms showing no glitch in the data stored at the storage node when wordline is pulled low due to addition of dummy transistor. (c) Effect of doubling the read access transistor gate width on storage node charge.

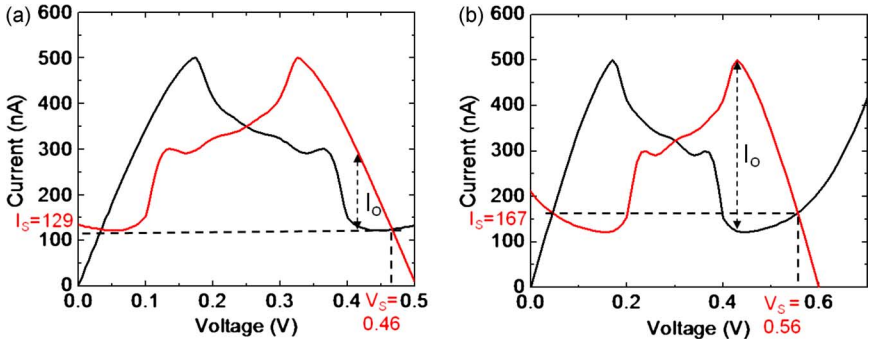


Fig. 10. Current charging the parasitic node capacitance after wordline is turned off for (a) $V_{\rm DD} = 0.5$ V, (b) $V_{\rm DD} = 0.6$ V. Charging current, I_0 is the difference of current through $\rm RITD_L$ and $\rm RITD_D$ and is larger for larger $V_{\rm DD}$. Also shown the standby power consumption given by $V_S \times I_S$.

Two mechanisms contribute to charge injection; channel charge $(Q_{\rm CH})$ and the overlap capacitance $(C_{\rm OV})$ between gate and junction. Thus the total voltage change at the storage node is given by [24]

$$\Delta V = \Delta V_{\rm GS}\frac{C_{\rm OV}}{C_{\rm OV}+c_{\rm SN}} + \frac{1}{2}\frac{Q_{\rm CH}}{C_{\rm SN}} = \Delta V_{\rm GS}\frac{C_{\rm OV}}{C_{\rm OV}+C_{\rm SN}} + \frac{1}{2}\frac{\rm WLC_{ox}(V_{GS}-V_t)}{C_{\rm SN}}. \quad (1)$$

(Assuming channel charge flows equally to source and drain junction).

From Fig. 3(b), the storage node capacitance

$$C_{\rm SN} = C_{\rm TDD} + C_{\rm TDL} + C_{\rm DB,write} + C_{\rm GS,read} \quad (2)$$

here $C_{\rm TDD}, C_{\rm TDL}$ are parasitic capacitances of driver and load tunnel diodes, $C_{\rm DB,write}$ is drain-bulk capacitance of write access transistor and $C_{\rm GS,read}$ is gate-source capacitance of read transistor.

From (1) it can be noted that a larger storage node capacitance results in smaller voltage variation due to injected charge. For example doubling the width of the read transistor doubles $C_{\rm GS,read}(= C_{\rm ox}{\rm WL})$. The resultant voltage change is shown in Fig. 9(c). However, any parasitic capacitance increase comes at the cost of increased cell area as well as slower storage node capacitance charging time which could offset the benefit of a lower injected charge.

The latch action of NDR devices naturally restores the voltage drop due to charge injection. The minimum peak current is set by the current needed to restore the node voltage within a clock interval to a voltage high enough for robust read operation. This simulation platform finally permits some insight as to the speed-power tradeoffs for TSRAM memory cells.

The current charging the parasitic node capacitance is the difference of the current through the load tunnel diode $(\rm RITD_L)$ and the driver tunnel diode $(\rm RITD_D)$, I_0, assuming the leakage current through the transistor is negligible, as shown in Fig. 10(a). If the bias voltage $V_{\rm DD}$ of the series connected tunnel diodes is increased to 0.6 V, the charging current I_0 increases. However, this leads to an increase in the voltage as well as the current of the bistable latch point both of which contribute to an increase in standby power $(\sim\ I_S \times V_S)$. A lower valley voltage could possibly circumvent this problem and result in larger charging currents with smaller bias voltage. The valley voltage depends on the degeneracy level of the QWs for the RITD and also depends on the device structure used to realize the tunnel diode, both of which can be tailored by the device engineer.

It should be noted that the "hump" in the NDR region is a measurement artifact which occurs due to instability in the NDR region, setting up oscillations, and an average current is measured by the parameter analyzer. This leads to a small underestimation of the charging current and possibly an erroneous valley voltage. A setup to get more accurate I-V data is currently being developed and follows reports presented in the sixties and

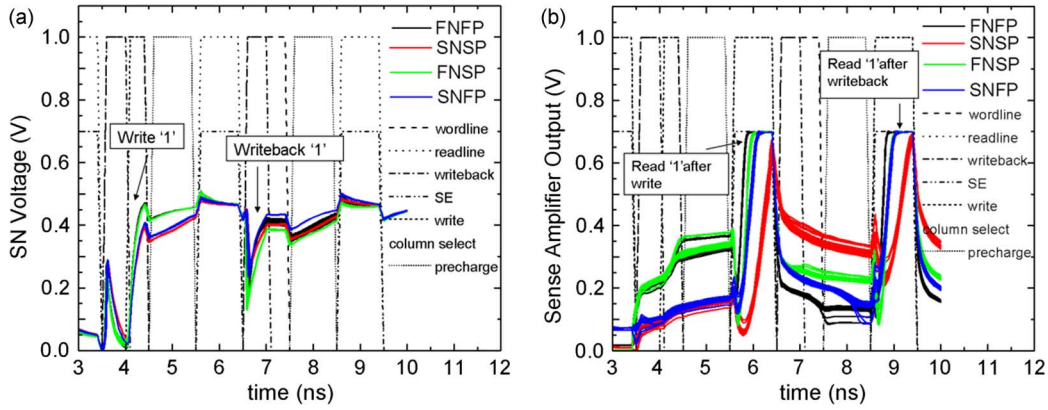


Fig. 11. Read/Write "1" operation showing (a) storage node voltage and (b) voltage read out from the sense amplifiers for all 32 bits along a wordline. The nodes are initially written with a "0". A write "1" operation followed by writeback "1" operation is simulated. Also overlapped are the control signals generated during each clock cycle. FNFP: Fast NFET Fast PFET; SNSP: Slow NFET Slow PFET; FNSP: Fast NFET Slow PFET; SNFP: Slow NFET Fast PFET.

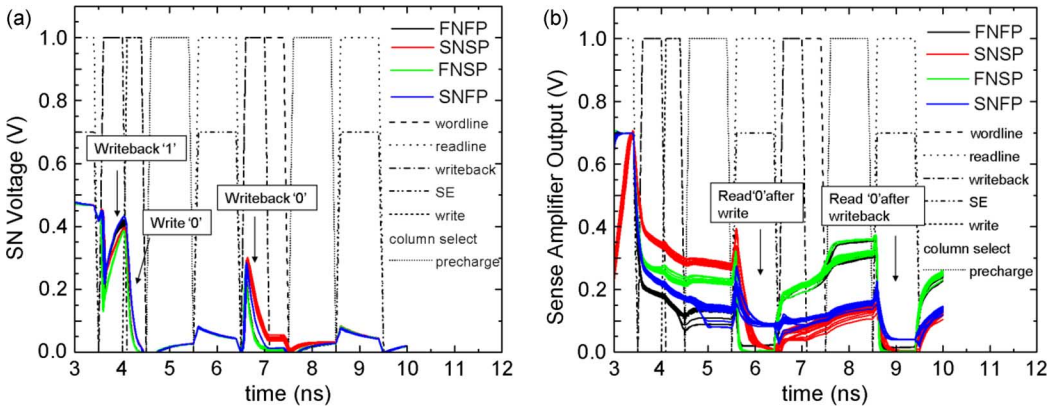


Fig. 12. Read/Write "0" operation showing (a) storage node voltage and (b) voltage read out from the sense amplifiers for all 32 bits along a wordline. The nodes are initially written with a "1". A write "0" operation followed by writeback "0" operation is simulated. Also overlapped are the control signals generated during each clock cycle. FNFP: Fast NFET Fast PFET; SNSP: Slow NFET Slow PFET; FNSP: Fast NFET Slow PFET; SNFP: Slow NFET Fast PFET.

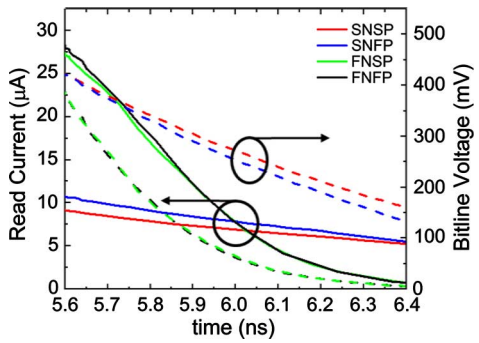


Fig. 13. Cell read current (solid lines) during read "1" operation and reduction in bitline voltage (dashed lines).

later to suppress these RLC oscillations ([26], and the references therein). However the error is not expected to be significant.

The voltage at the node drives the gate of the read transistor and hence a lower gate voltage results in reduced read speed and possibly an erroneous read if too low/high to be recognized as a "1"/"0". The peak current should be as low as possible since its choice also affects the minimum valley current which is related to the cell power consumption as will be discussed later. A higher PVCR device can mitigate this drawback by increasing the charging current I_0 and keeping the valley current low concurrently resulting in smaller standby power consumption.

A peak current of 500 nA was found to be the minimum current for robust circuit operation including variations in the tunnel diode spacer thickness (see Section III). With a device size of 200 nm $\times$ 200 nm, this results in a peak current density of 1.2 kA/cm^2. Although the peak current density of the device used to model the RITD is 129 A/cm^2 current densities from 218 kA/cm^2 to 20 mA/cm^2 for Si/SiGe RITDs have been obtained by varying the spacer thickness from 1.5 nm up to 16 nm [20], [27].

C. Impact of Process Variation

Robustness of the circuit to process variations is critical with extreme device scaling. The transistor model includes process variations due to gate oxide thickness, threshold voltage and transistor dimensions. STI stress and well edge-proximity effects are also included. Figs. 11 and 12 shows four corner simulation results for 32 bit read/write "1" and read/write "0" operation. The cells are not exactly identical due to difference in interconnect parasitics between the cells and writeback/sense amplifier circuits along a row. Figs. 11(a) and 12(a) shows the storage node voltage while Figs. 11(b) and 12(b) show the output of the sense amplifier for the respective read/write operations. A

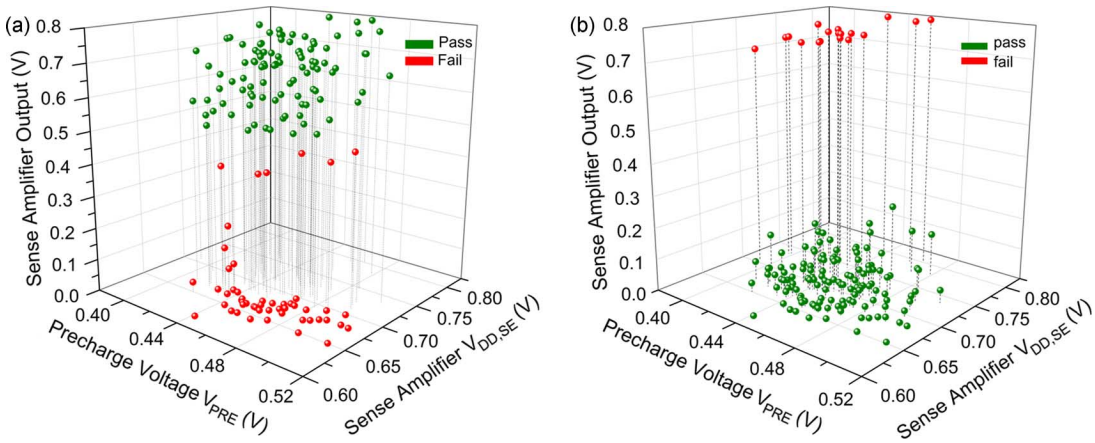


Fig. 14 Effect of variation of precharge voltage and sense amplifier voltage on sense amplifier output for (a) read "1" and (b) read "0" operation. Choice of precharge voltage and sense amplifier V_{DD} restricted by conditions for successful read "0" and "1" operation.

65% drop in cell drive current is observed between fast and slow NFET corners due to a threshold voltage variation of 120 mV (see Fig. 13). This limits the number of cells/bitline.

Sensitivity of the read operation to sense amplifier bias voltage $(V_{\mathrm{DD,SE}})$ and precharge voltage (V_{PRE}) are shown in Fig. 14. The limitations on the two voltages are set by the slow NFET-fast PFET (SNFP) corner for read "0" operation and slow NFET-slow PFET (SNSP) corner for the read "1" operation. The conditions for successful read are

$$V_{\mathrm{DD,SE}} - V_{\mathrm{PRE}} < |V_{\mathrm{tp}}|_{\mathrm{SNFP}} \tag{3}$$

$$V_{\mathrm{PRE}} > V_{\mathrm{tn,SNSP}}. \tag{4}$$

Slow-fast corner shows slightly higher sense amplifier output for logic "0". This is due to a slow NFET and fast PFET. Ideally the NFET should be turned on while PFET should remain off. However a precharge voltage of 0.45 V with a high NFET V_{th} and low PFET V_{th} for this corner, results in both transistors being turned on and a slight increase in the voltage read out.

Robustness to process variations and geometric mismatch is determined by Monte-Carlo simulations. To model tunnel diode current variation due to nonuniform spacer thickness across the wafer, a 0.5 monolayer variation in thickness is assumed. For silicon, this is equal to ∼0.25 nm (Δ). From experimental data [20] peak current density (J_P) and valley current density (J_V) are found to vary exponentially with spacer thickness. Using empirical fitting

$$J_P = 2.441 \cdot 10^5 \cdot \exp(-0.8081 \cdot W) = Ae^{-Bt} \tag{5}$$

$$J_V = 1.138 \cdot 10^5 \cdot \exp(-0.8978 \cdot W). \tag{6}$$

Percentage change in J_P

$$\Delta J_P = \left(\frac{Ae^{-B(t\pm\Delta)} - Ae^{-Bt}}{Ae^{-Bt}}\right) \times 100$$

$$= (e^{-B\times\pm\Delta} - 1) \times 100$$

$$\Delta J_P = (e^{-0.8081\times\pm0.25} - 1) \times 100 \cong \mp 20\%. \tag{7}$$

Peak current is modeled as a Gaussian distribution about 500 nA. with $3\sigma = 100$ nA (= 20% of 500 nA).

To model valley current density variation the relation between peak current and valley current is determined as follows.

From (7)

$$\Delta J_P = (e^{-B\times\Delta} - 1) = (e^{-0.8081\times\Delta} - 1) \tag{8}$$

$$\Delta = \frac{-1}{0.8081}\ln(\Delta J_P + 1)$$

$$= \frac{-1}{0.8081}\ln\left(\frac{I_p - I_{\mathrm{nom}}}{I_{\mathrm{nom}}} + 1\right) \tag{9}$$

where I_P is variation in peak current from its nominal value I_{nom}

$$\Delta J_V = (e^{-0.8978\times\Delta} - 1) \tag{10}$$

$$\Delta J_V = \left(e^{-0.8978\times\frac{-1}{0.8081}\ln\left(\frac{I_p - I_{\mathrm{nom}}}{I_{\mathrm{nom}}}+1\right)} - 1\right)$$

$$= \left(\frac{I_P - I_{\mathrm{nom}}}{I_{\mathrm{nom}}} + 1\right)^{3.04} - 1. \tag{11}$$

The resultant PVCR variation with peak current obtained from Monte Carlo simulation is shown in Fig. 15(a).

RITD capacitance variation with spacer thickness is included in the model by assuming the capacitance to be given by $\varepsilon \mathrm{A}/\mathrm{d}$ where d is the spacer thickness.

Hence, RITD capacitance $= C_{\mathrm{nom}} \cdot t_{\mathrm{nom}}/(t_{\mathrm{nom}} + \Delta)$, where C_{nom} = nominal capacitance for spacer thickness t_{nom} (8 nm).

A maximum mismatch of 20% between the two RITDs in a memory cell is also incorporated. This leads to variation in the bistable latch points which correspond to the logic "1" and logic "0" for the memory cell [see Fig. 15(b) and (c)].

To estimate robustness to process and mismatch variations 1500 Monte Carlo simulations were run with Latin hypercube sampling to get a better spread in sample points. The results are as shown in Figs. 16 and 17. Figs. 16(a) and 17(a) shows the voltage stored in the memory cell at the end of the write cycle for logic "1" and "0", respectively. The restoring action of the

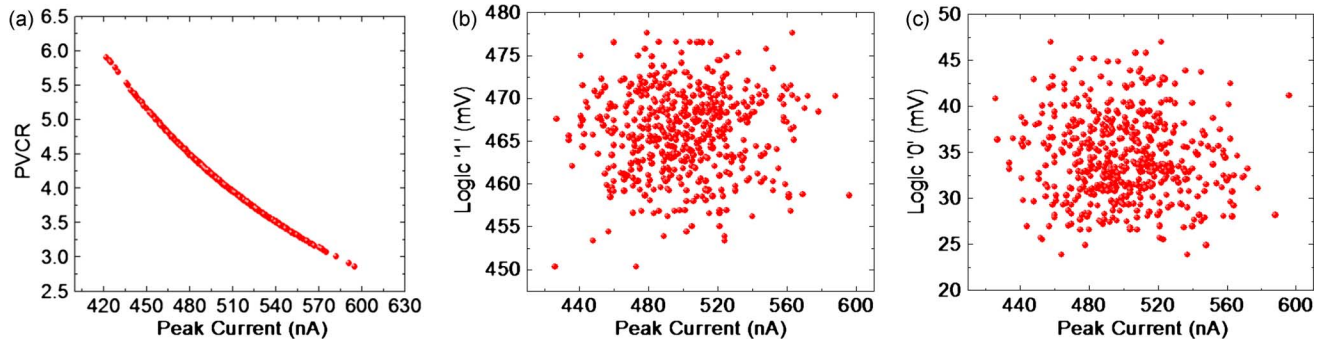


Fig. 15. (a) PVCR variation with peak current implemented in the device model and resulting variation in bistable latch point for (b) logic "1" and (c) logic "0" due to mismatch between the series connected RITDs in the memory cell.

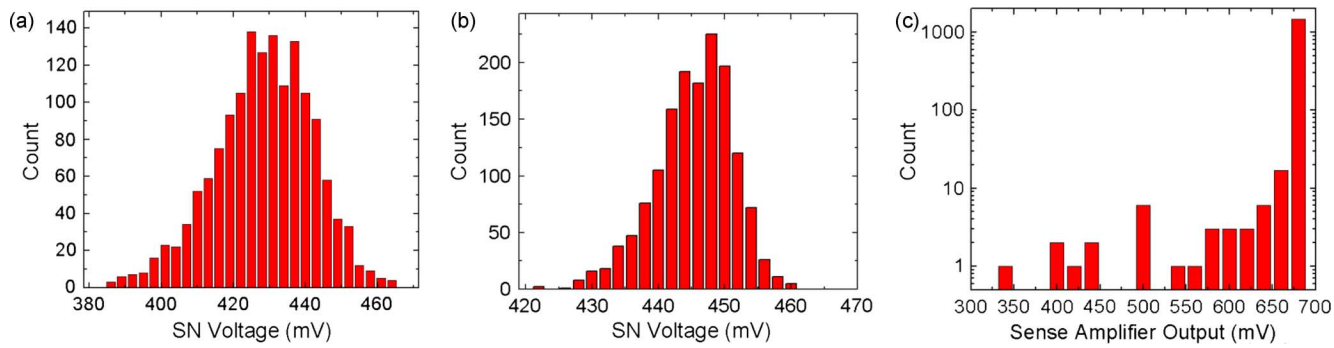


Fig. 16. Monte Carlo simulation results for read/write "1" operation showing (a) variation in voltage written into storage node SN at the end of write cycle, (b) variation in SN voltage 1 ns after wordline is pulled low, showing the restoring action of the RITDs, and (c) variation in output of sense amplifier at the end of read cycle.

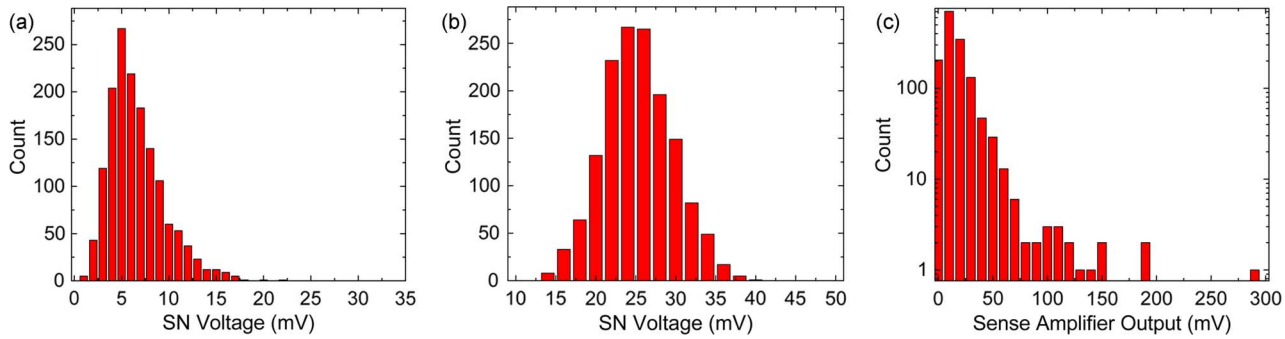


Fig. 17. Monte Carlo simulation results for read/write "0" operation showing (a) variation in voltage written into storage node SN at the end of write cycle, (b) SN voltage 1 ns after wordline is pulled low, showing the restoring action of the RITDs, and (c) variation in output of sense amplifier at the end of read cycle.

RITDs pulls the stored voltage towards the bistable latch point. Storage node voltage 1 ns after the wordline is deactivated is shown in Figs. 16(b) and 17(b). The corresponding sense amplifier output voltage at the end of the read cycle is as shown in Figs. 16(c) and 17(c) showing successful read/write operation with ± 3 sigma of chip mean and across the chip variation.

The failure region corresponding to the worst case cell on the worst case chip was evaluated using Monte Carlo simulations run with the chip mean skewed to a 3 sigma corner and across the chip variations enabled. From the four corner simulations, the slow NFET-slow PFET corner is found critical for write/read "1" operation while the slow NFET-fast PFET corner is critical to the write/read "0" operation. The critical transistor for write operation is MN0 while for read operation is MN1 and sense amplifier PFET (SAMP) and NFET (SAMN). Fig. 18 illustrates the threshold voltage variation for the low $V_{\rm th}$ NFET and PFET along with the number of sigma from mean for the actual and skewed distributions.

The scatter plots in Fig. 19 show the storage node voltage 1 ns after the wordline is pulled low. No failure is observed for both write "1" and "0" operations.

A scatter plot of the sense amplifier output, 1 ns after the readline is turned on, with the three critical transistors involved in read operation is shown in Fig. 20. The read "1" operation has a linear dependence on the read transistor (MN1) threshold voltage, while the read "0" operation has a linear variation with the sense amplifier NFET (SAMN) threshold voltage. The fail boundary is determined from Fig. 21 where a fail for read "1" operation is an output less than 0.3 V and a fail for read "0" operation is an output greater than 0.15 V. The threshold voltage

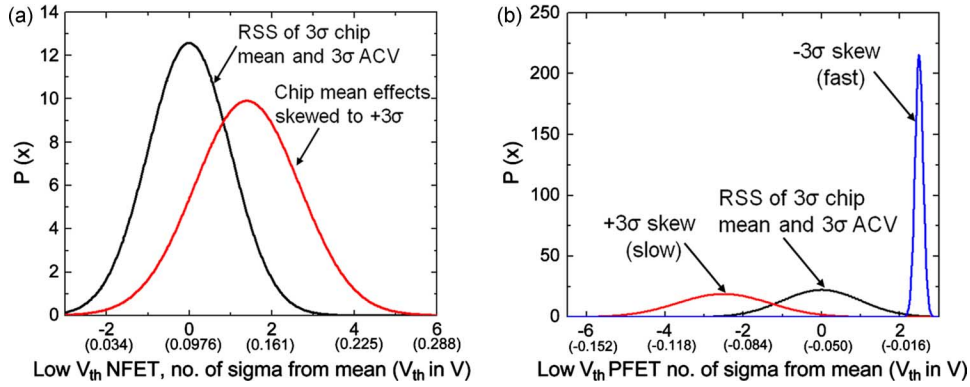


Fig. 18. Threshold voltage variation for low threshold voltage (a) NFET and (b) PFET obtained from Monte Carlo simulations showing actual distribution and distribution with chip mean skewed to a process corner. ACV = across chip variation. RSS = root of sum of squares.

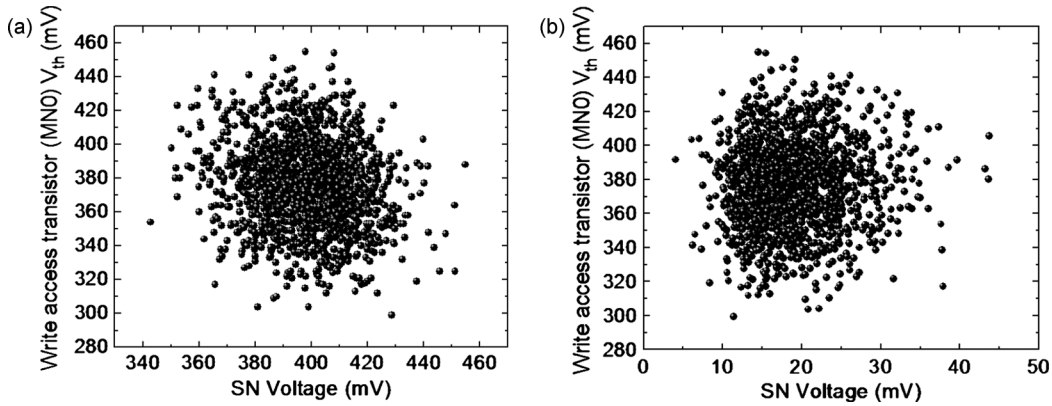


Fig. 19. Storage node voltage variation with across the chip variation for (a) Write "1" operation skewed to slow-slow corner (b) Write "0" operation skewed to slow NFET, fast PFET corner, showing no failure points.

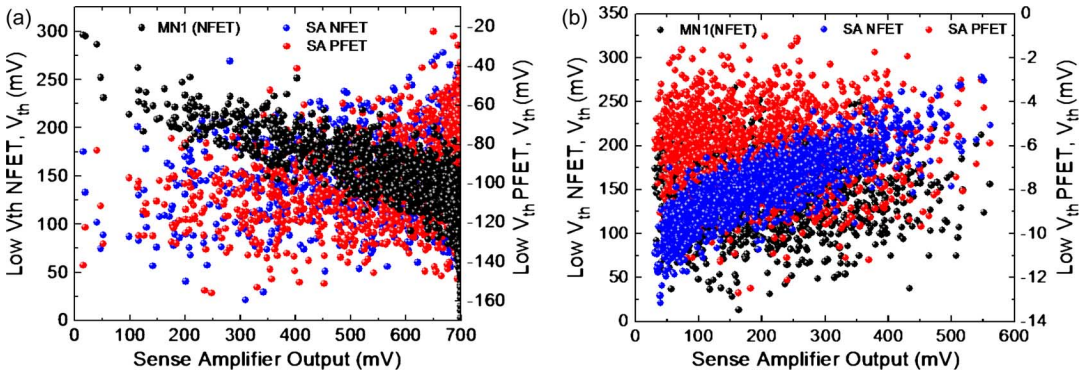


Fig. 20. Scatter plot of sense amplifier output for (a) read "1" operation skewed to slow-slow corner, (b) read "0" operation skewed to slow NFET, fast PFET corner with sense amplifier PFET and NFET and read transistor MN1 SA = Sense Amplifier.

variation is modeled as a Gaussian distribution. From Fig. 21 the cell failure probability during a read "1" operation, assuming the process parameters are uncorrelated, is

$$P\left(V_{\mathrm{th,MN1}} > 0.17\,V, |V_{\mathrm{th,SAMP}}| > 80\ \mathrm{mV}\right) = 5.76 \times 10^{-4}.$$

The read "0" failure probability is

$$P\left(V_{\mathrm{th,SAMN}} > 0.15\ \mathrm{V}, |V_{\mathrm{th,SAMP}}| > 12\ \mathrm{mV}\right) = 5.52 \times 10^{-4}.$$

For small size memories of a few kilobytes the cell failure probability is small enough to ensure good yield. However for large arrays of 1 MB the read access time should be increased and a more judicious choice of precharge and sense amplifier V_{DD} should be made, as discussed in Section V-C, to improve the yield.

D. Power Analysis

The total power consumption for a cell and the power consumed by each device in the cell is shown in Fig. 22(a). When considering power consumption both active and standby power

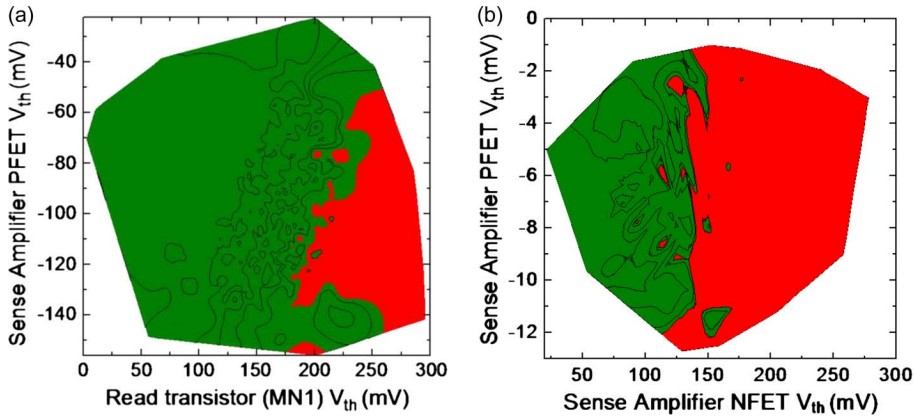


Fig. 21. Fail boundary for (a) read "1" operation skewed to slow-slow corner and (b) read "0" operation skewed to slow NFET, fast PFET corner.

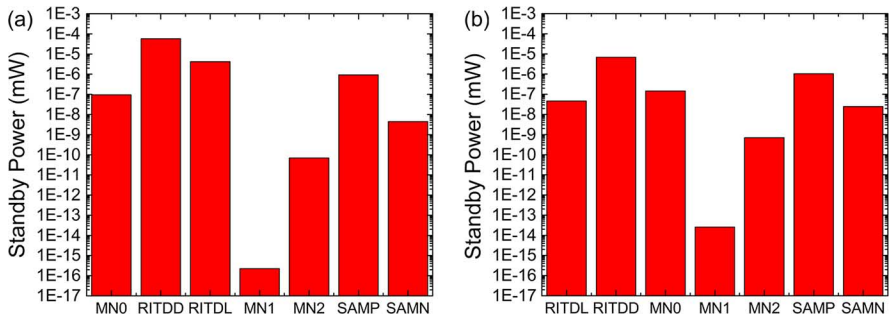


Fig. 22. Standby power consumption of a memory cell and sense amplifier. The power consumption for a (a) PVCR of 4 and (b) PVCR of 144 is compared. SAMP: Sense amplifier PFET, SAMN: Sense amplifier NFET.

is important. The average power during a write "1" operation is 0.45 μW/cell while the read "1" power is 2.6 μW/cell. The read "0" power is 0.15 μW/cell. The dynamic power consumption per cell is 1.8×10^{-7} mW/MHz which is much lower than that of an SRAM (8.5×10^{-7} mW/MHz, ITRS 2006). It is calculated using

$$P_{\mathrm{dyn}} = (V_{\mathrm{dd,WL}} \times C_{\mathrm{WL}}/\mathrm{cell} \times V_{\mathrm{dd,WL}} + 0.8V_{\mathrm{dd,BL}} \times C_{\mathrm{BL}}/\mathrm{cell} \times 0.8V_{\mathrm{dd,BL}}) \times 10^6\ \mathrm{W} \quad (12)$$

where $C_{\mathrm{WL}}/\mathrm{cell} = C_{G,\mathrm{MN0}} = 0.175$ fF, $C_{\mathrm{BL}}/\mathrm{cell} = C_{\mathrm{SB,MN0}} + C_{\mathrm{SB,MN2}} = 66$ aF, $V_{\mathrm{dd,WL}} = 1\,V$ $V_{\mathrm{dd,BL}} = 0.5$ V.

The standby power is 60 nW/cell. The dominant standby power component is the power due to valley current flowing through the tunnel diodes at the latch point. For the same peak current a higher PVCR leads to lower static power consumption. Fig. 22(b) illustrates the power consumption for a PVCR of 144 (The highest PVCR reported for any NDR device [29]). An order of magnitude reduction in standby power is observed (standby power/cell $= 7$ nW). Further lowering of standby power would require a lower peak current or higher PVCR device. The former would result in lower speed of operation as explained in Section V-B thus resulting in a speed-power tradeoff.

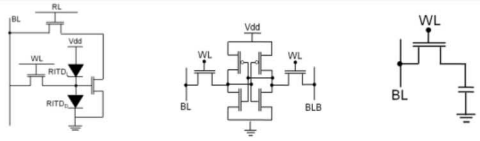
The energy consumed by the 32 cells along a wordline is 2.62 fJ when a "1" is written into all 32 bits, 71 fJ for a 32 bit all one read, and 3.9 fJ for a 32 bit all zero read. The standby energy is 1.3 fJ. The active energy is obtained by integrating the power over the write/read cycle while the standby energy is obtained by integrating the standby power over a clock cycle (0.5 ns).

TABLE I
PERFORMANCE SUMMARY

Technology	90 nm TSRAM
Vdd	(wordline/SA/cell) 1/0.7/0.5
Word length	32 bit
Cell size μm^2	1.83 (logic DRC rules)
Rows/bitline	32
Write cycle time (ns)	0.5
Read cycle time (ns)	1
Dynamic power per cell (mW/MHz)	1.8×10^{-7}
Static Power Dissipation per cell (Standby) (mW)	6×10^{-5}
Mean tunnel diode peak current (nA)	500
Mean tunnel diode PVCR	4.02

A summary of the performance is provided in Table I. A comparison between different embedded memory technologies is

TABLE II
EMBEDDED MEMORY COMPARISON

	3T-2RITD TSRAM	6T-SRAM	1T-1C DRAM
Cell Schematic			
Cell size (μm^2), 90 nm technology	1.83 (logic design rules)	1.13	0.1-0.243
Data storage	Restoring action of tunnel diodes	Feedback action of cross-coupled inverters	Floating capacitor, requires refresh operation
Destructive readout	No	No	Yes
Sensing	Single-ended sensing utilized in this work. Differential sensing can be utilized, similar to DRAM	Differential sensing	Differential sensing
Compatibility with logic	2 additional mask steps	Compatible	4-6 additional mask steps. Requires large cell capacitor; difficult to fabricate with scaling dimensions since cell capacitance needs to be constant
Delay	Small. Limited by time to charge parasitic storage node capacitance	Small. Limited by time for node storing '1' to reduce below trip point of inverter	Large. Limited by time to charge cell capacitor
Voltage scaling	Limited by peak voltage of tunnel diodes. $V_{DD,logic1} > 2 \times V_{peak} \sim$ 0.2V [28] / $V_{th,read}$ $V_{DD,WL} > V_{DD,logic1} + V_{th}$	$V_{DD} \sim 0.7V$ Limited by functional margins due to process variations with dimensional scaling	$V_{DD,WL}$ ~1.5V $V_{DD,logic1} \sim 1V$ to maintain sufficient charge on capacitor

shown in Table II with colorations to indicate severity of each issue.

E. Functional Robustness

Any variation on the storage node voltage is restored by the latching action of the tunnel diodes as long as the noise on the node is not large enough to tip the storage node voltage over the peak voltage into the metastable latch point. The read operation does not cause any cell instability unlike in the case of an SRAM. Voltage scaling is limited only by the limitations in transistor threshold voltage scaling (i.e., increased leakage current issues), e.g. in this design a 1 V was used for wordline however a low $V_{\rm th}$ transistor could be used for the write access transistor, and the wordline voltage reduced to $V_{\rm logic,1} + V_{\rm th,low} = 0.5 + 0.15 = 0.65$ V. However, a regular $V_{\rm th}$ transistor is used to keep the leakage current low. Alternate transistor technologies such as Tunnel FETs with lower subthreshold swing can be considered to replace the MOSFET to overcome this [30]. The lower limit on $V_{\rm logic,1}$ is set by the peak voltage $(V_{\rm peak})$ of the tunnel diode and is approximately equal to $2 \times V_{\rm peak}$. $V_{\rm peak}$ depends on the material system and device structure used for the tunnel diode and can be as low as 0.1 V [28]. The memory cell configuration itself is robust to voltage scaling, unlike in the case of an SRAM where voltage scaling is limited to 0.7 V due to issues with cell transistor sizing inherent to the cell architecture, leading to functional robustness issues such as loss of data during read access. Hence requiring modifications in cell structure such as 7 T and 8 T SRAM cells [8].

VI. CONCLUSION

A 32 bit × 32 bit tunneling SRAM memory array is simulated and the speed-power-area tradeoffs are studied. 1 T-2 Tunnel diode and 3 T-2 Tunnel diode configurations are considered with the 3 T configuration proving to be most suited for high speed operation. The choice of tunnel diode peak current and PVCR provide a speed/power tradeoff with a higher peak current needed for high speed operation which requires a higher PVCR to keep the standby power consumption low. For the technology node simulated, a 0.5 ns write access time, 1 ns read access time is obtained with a standby power consumption of 6×10^{-5} mW/cell and a dynamic power consumption of 1.8×10^{-7} mW/MHz per cell. Robustness to process variations has been shown up to $\pm 6\sigma$ for the write operation and $\pm 3\sigma$ for read operation. For high yield on larger memory array's a larger read access time and a more judicious choice of precharge and sense amplifier voltage are required. Differential sensing will also be investigated.

The primary advantage of TSRAM over SRAM is its robustness to voltage scaling which is essential for reducing active power and maintaining compatibility with logic. In comparison to embedded DRAM, TSRAM does not require fabrication of a large external capacitor, can achieve high-speed operation due to the small storage node capacitance charge/discharge time as well as does not require periodic refresh cycles. This study can be further extended to other NDR devices that can be integrated with CMOS technology.

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