Extending CMOS: Quantum Functional Circuits Using Si-Based Resonant Interband Tunnel Diodes

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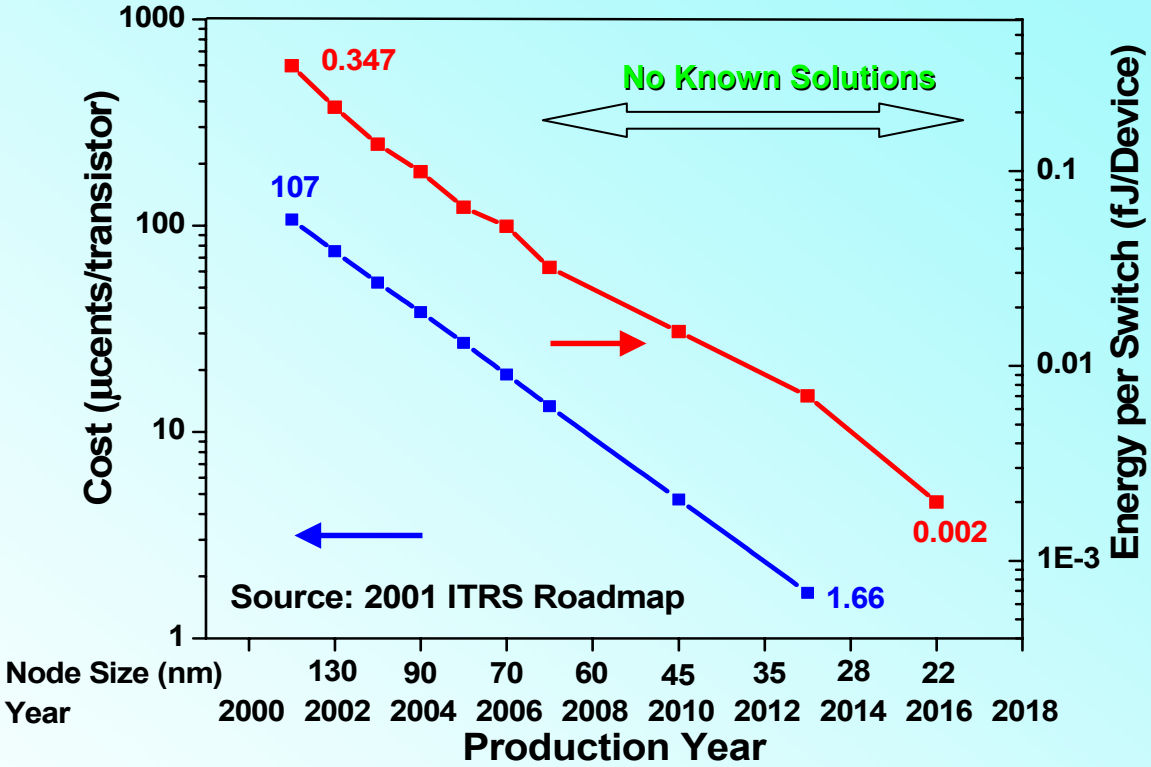
This work is indebted to the MBE sample exchanges by:

Phillip E. Thompson (*Naval Research Laboratory*),

Motivation: Extending CMOS?



- CMOS cannot be scaled indefinitely.
- Solutions: either replace or augment scaled CMOS
- Tunnel diodes married with CMOS offer enhancements

The Limitation of CMOS

- **As CMOS dimensions are reduced, evolutionary changes will stop when quantum effects dominate and alternative revolutionary paradigms will be sought. Examples of CMOS salient issues:**
  - Gate oxide tunneling
  - Dopants fluctuations
  - Channel quantization effect
- **The 2001 ITRS Roadmap expects CMOS can shrink to channel lengths of 20-30nm before a new type of device will replace CMOS.**

ITRS: Emerging Research Devices

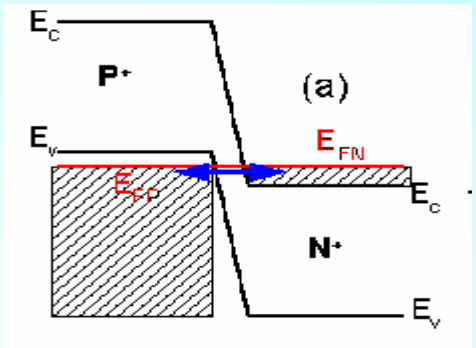
- **Monolithic Integration of Si-based tunnel diodes with Si-based transistors**

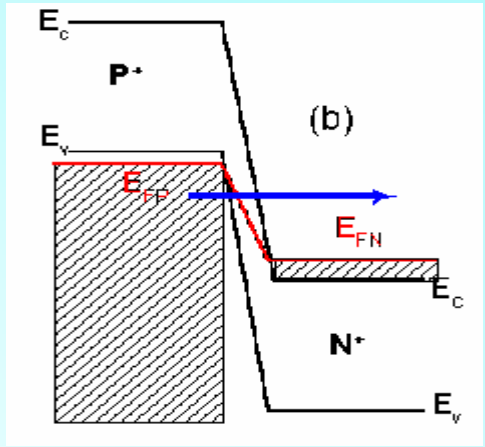
						
Device	*Resonant Tunneling Diode – FET*	*Single Electron Transistor*	*Rapid Single Quantum Flux Logic*	*Quantum Cellular Automata*	*Nanotube Devices*	*Molecular Devices*
Types	3-terminal	3-terminal	Josephson Junction +inductance loop	-Electronic QCA -Magnetic QCA	FET	2-terminal and 3-terminal
Advantages	Density, Performance, RF	Density, Power, Function	High speed, Potentially robust, (insensitive to timing error)	High functional density, No interconnect in signal path, Fast and low power	Density, Power	Identity of individual switches (e.g., size, properties) on sub-nm level. Potential solution to interconnect problem
Challenges	Matching of device properties across wafer	New device and system, Dimensional control (e.g., room temp operation), Noise (offset charge), Lack of drive current	Low temperatures, Fabrication of complex, dense circuitry	Limited fan out, Dimensional control (room temperature operation), Architecture, Feedback from devices, Background charge	New device and system, Difficult route for fabricating complex circuitry	Thermal and environmental stability, Two terminal devices, Need for new architectures
Maturity	Demonstrated	Demonstrated	Demonstrated	Demonstrated	Demonstrated	Demonstrated

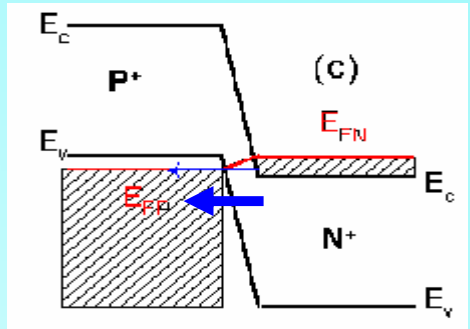
Adopted from 2001 ITRS Roadmap (http://public.itrs.net)

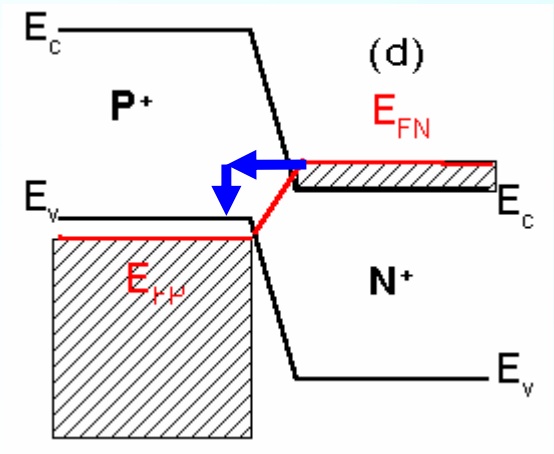
International Technology Roadmap for Semiconductors (ITRS), which is a consortium of international semiconductor manufacturers and semiconductor equipment vendors, annually forecasts future semiconductor technology

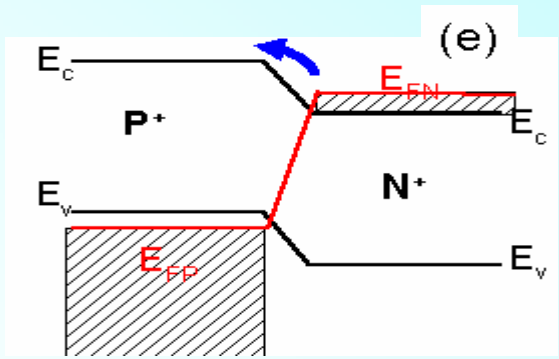
Basic Physics: Esaki Tunnel Diode (Interband)

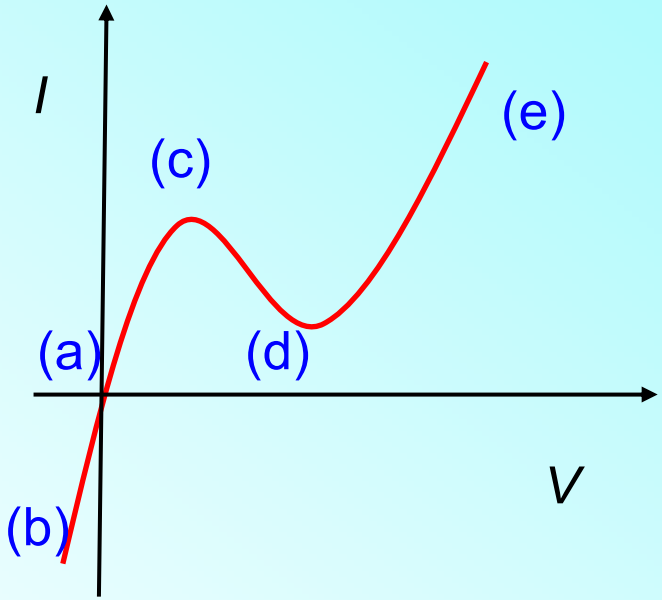








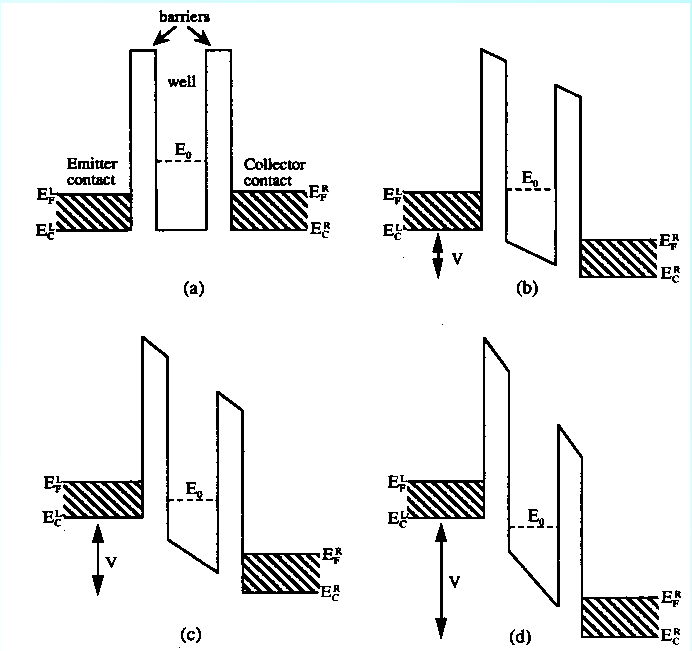


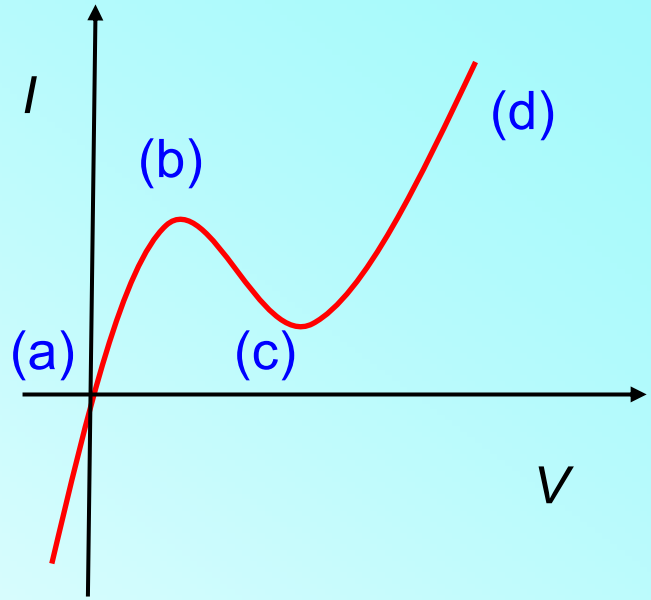


Degenerate Doping Required – Difficult with conventional epitaxy

For more info see L. Esaki, "New phenomenon in narrow Germanium p-n junctions," *Phys. Rev.*, vol. 109, p. 603, 1958.

Basic Physics: Resonant Tunneling Diode (Intraband)





Large Band Offset Required

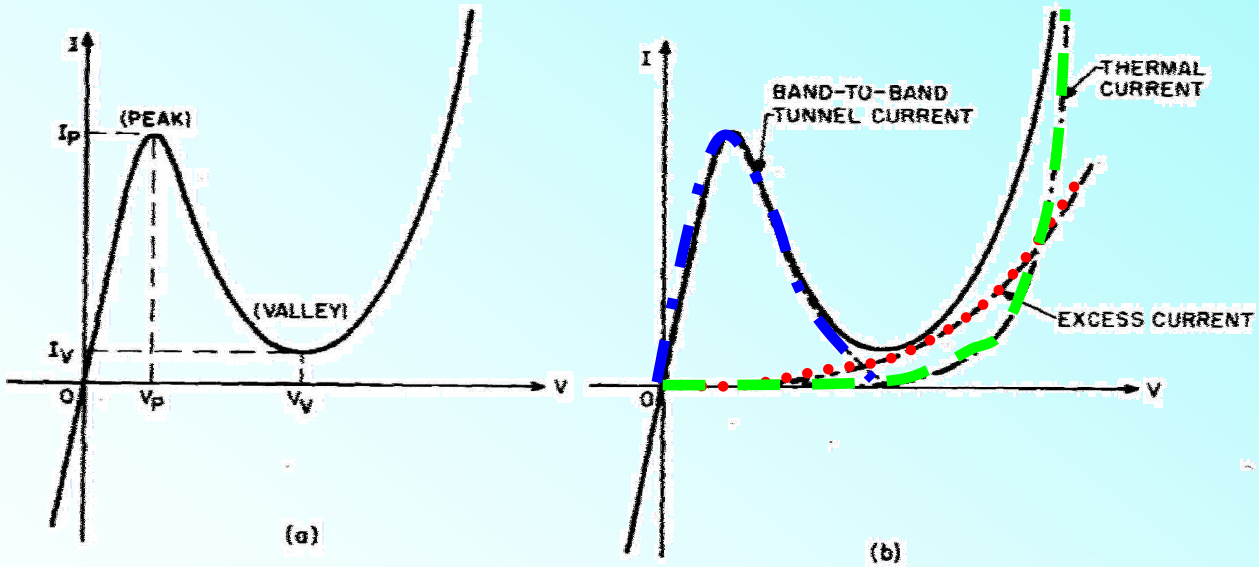
For more info see L. L. Chang, L. Esaki and R. Tsu, "Resonant tunneling in semiconductor double barriers," *Appl. Phys. Lett.*, vol. 24, pp. 593-595, 1974.

Si/SiGe heterojunction has limited band offset without a thick relaxed buffer

Alternative barriers (i.e. SiO_2) present difficult heteroepitaxy of single crystal Si quantum well atop amorphous barrier

Three Interband TD Current Components

From Sze, Physics of Semiconductor Devices, pg. 517 (1981).



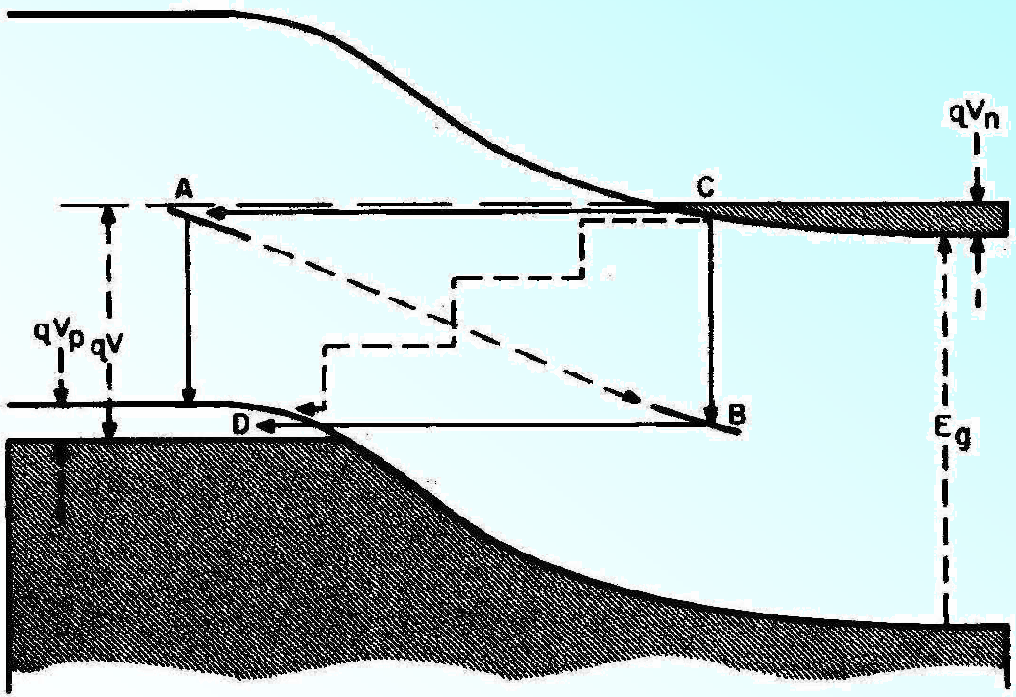
- Desired: optimize structure for efficient quantum mechanical tunneling
- Undesired: excess current comprised partially of defect related tunneling
- Thermal diffusion current eventually takes over at higher biases

Basic TD Figure-of-Merit

- Peak-to-valley current ratio (PVCR) = I_p/I_v
- Peak current density (PCD or J_p)= I_p/A, where A is the diode area

Excess Current of an Esaki Diode

Figure adapted from Sze, Physics of Semiconductor Devices, pg. 528 (1981).

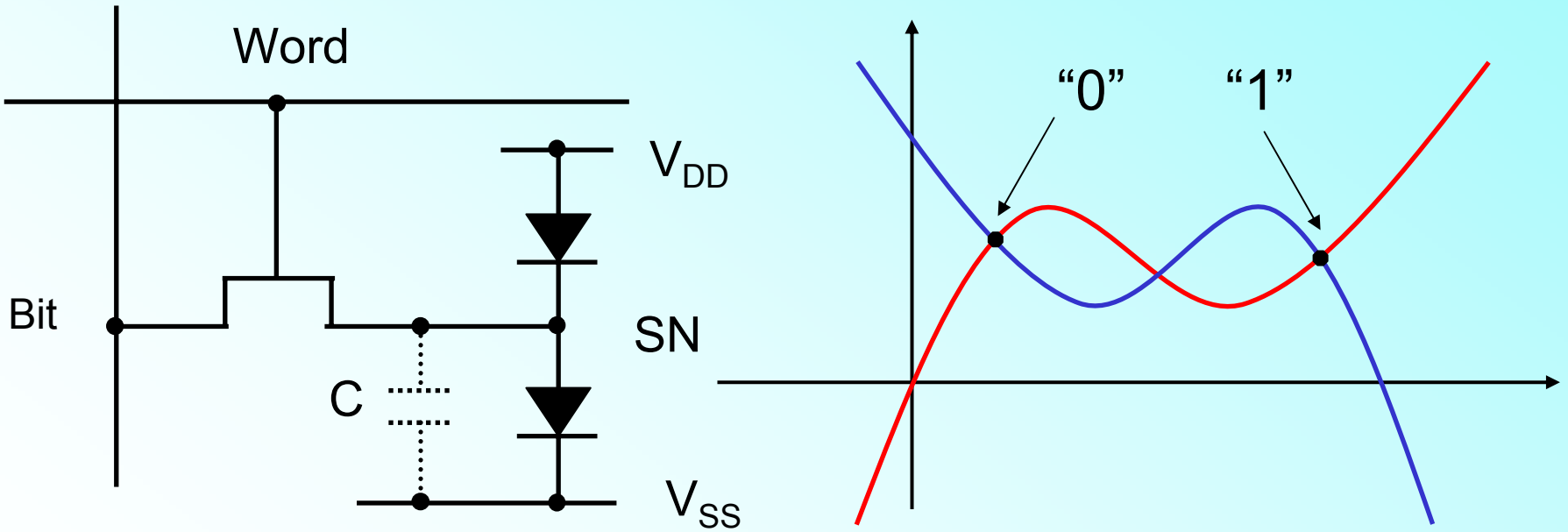


- **Excess current limits PVCR.**
- **Excess current is a tunneling phenomena via defect or midgap states**

For more info see Chynoweth et al., Phys. Rev., vol. 121, p. 684, (1961).

Application: Tunnel Diode Memory

- One Transistor Tunnel Diode SRAM (1T TSRAM)
- Compact replacement for 6 transistor SRAM cell
- Refresh-free – Low Power Consumption

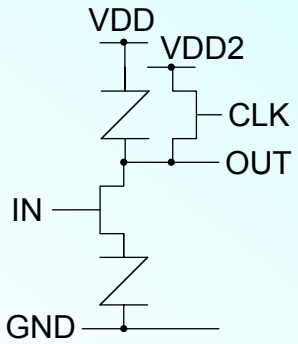


- J. P. A. van der Wagt, A. C. Seabaugh, and E. A. Beam, III, "RTD/HFET low standby power SRAM gain cell," *IEEE Electron Dev. Lett.* **19**, pp. 7-9 (1998).
- J. P. A. van der Wagt, "Tunneling-Based SRAM," *Proc. of IEEE*, 87, pp. 571-595 (1999).

LATCHED COMPARATOR 25 GHz DESIGN
(Courtesy A. Seabaugh, formerly Raytheon Systems)

Quantum

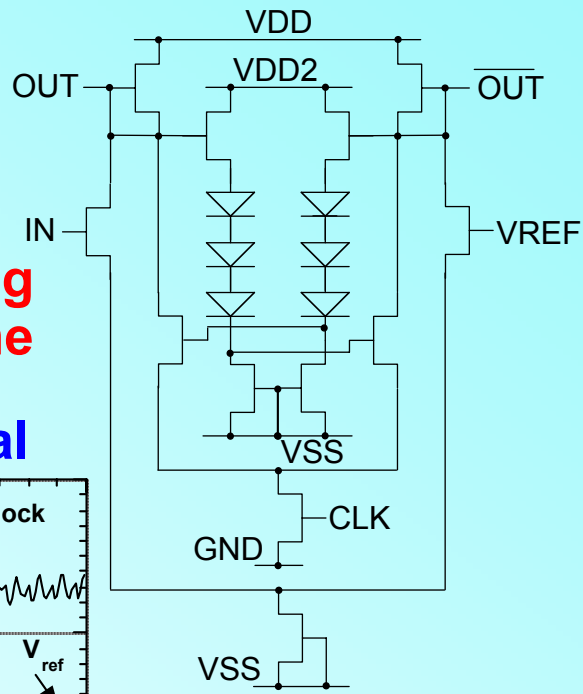
- Latching behavior is inherent to RTD
- Settling time is determined by RTD switching speed



- Regenerative feedback gives latching
- Feedback loop has long settling time

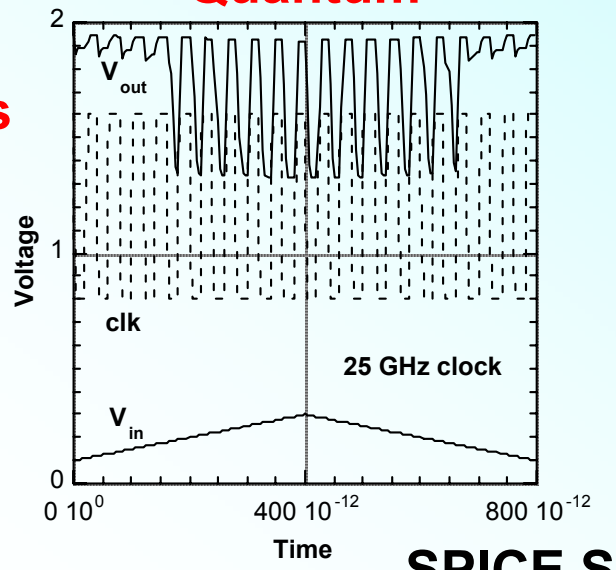
2 RTDs
2 HFETs
Area=1

Conventional

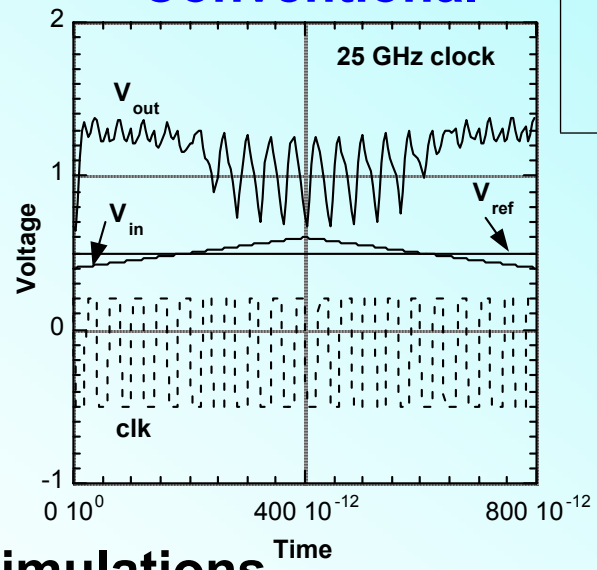


12 HFETs
6 Schottky Diodes
Area=6

Quantum



Conventional



SPICE Simulations

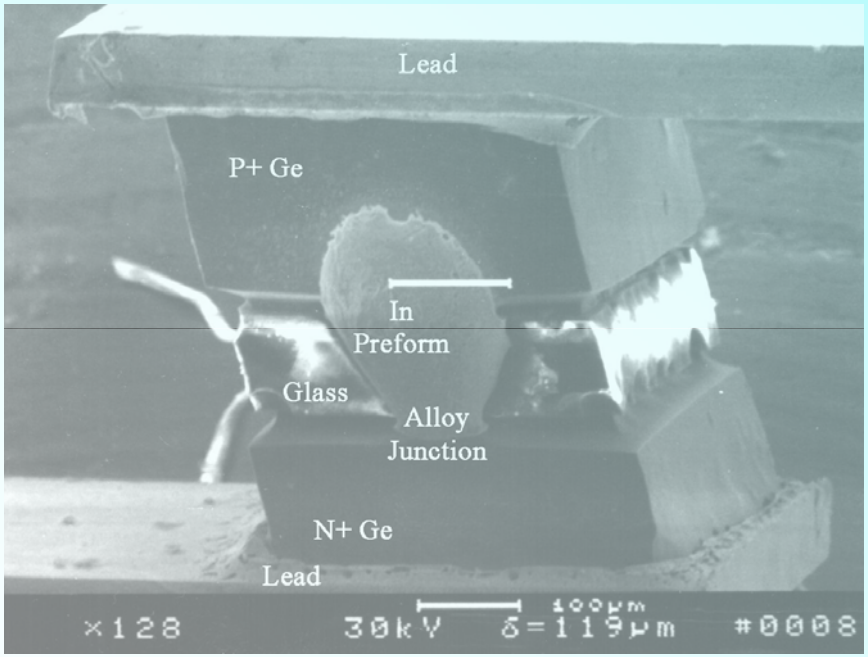
The Payoff: TDs Integrated with Transistors

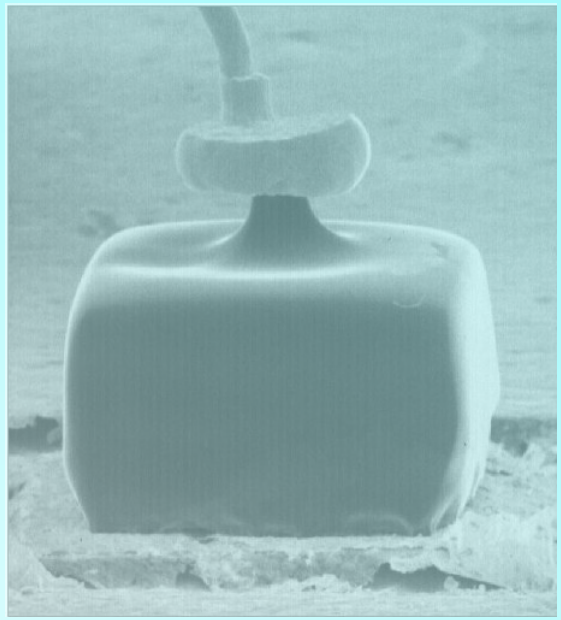
More computational power per unit area

- ✓ Fewer devices required
- ✓ Faster circuits and systems
- ✓ Reduced power consumption

Result: Extension of CMOS if a Si-Based TD is available that is compatible with CMOS!

Prior Art: Lack of Si-Based TDs that can be Monolithically Integrated with Si transistors





Ge Esaki Diode

Si Esaki Diode

- Vintage 1960's alloy technology prevents large-scale batch processing
- Discrete Esaki diodes are ideal for niche applications.
- However the alloy process does not lend itself to an integrated circuit.

First Si-Based Resonant Interband Tunnel Diodes

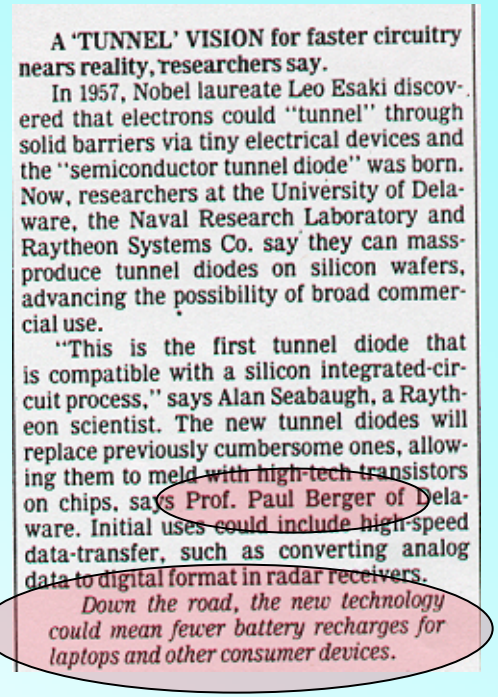
Approach	ΔE_C (eV)	Upper Barrier Crystalline	Quantum Well Crystalline	Lower Barrier Crystalline	Production Potential	Status
SiO_2/a-Si/SiO_2	3.2	No	No	No	High	Abandoned - High scattering in quantum, no room temperature PVR
CaF_2/Si/CaF_2	2	Yes	Yes	Yes	Low	Abandoned - Tendency for island growth, defect-assisted transport below 10 nm
ZnS/Si/ZnS	1	Yes	Yes	Yes	Med.	ZnS on Si growth established, Si quantum well growth under study
SiO_2/Si/SiO_2 Lateral overgrowth	3.2	No	Yes	No	Med.	Process for forming oxide islands established, overgrowth process under development
ZnS/Si/ZnS Lateral overgrowth	1	Yes	Yes	Yes	Med.	ZnS islands have been prepared for first overgrowth experiments
SiO_2/SiGe(C)/SiO_2 Lateral overgrowth	3.2	No	Yes	No	Med.	Oxide islands have been prepared for first overgrowth experiments
Si/SiGe resonant interband tunnel diode	-	-	-	-	High	World's first demonstration on Si; room temperature peak-to-valley current ratio of 1.6

980505

A paradigm shift from other approaches was spearheaded by a team of researchers lead by Berger (then at the University of Delaware), Naval Research Laboratory and Raytheon Systems.

- DARPA Award of Excellence (1998)
- Late News at International Electron Devices Meeting.
- Best Science/Engineering Dissertation
- Special Invitation to 2003 ITRS Meeting

Front page of the Wall Street Journal (October 1, 1998).



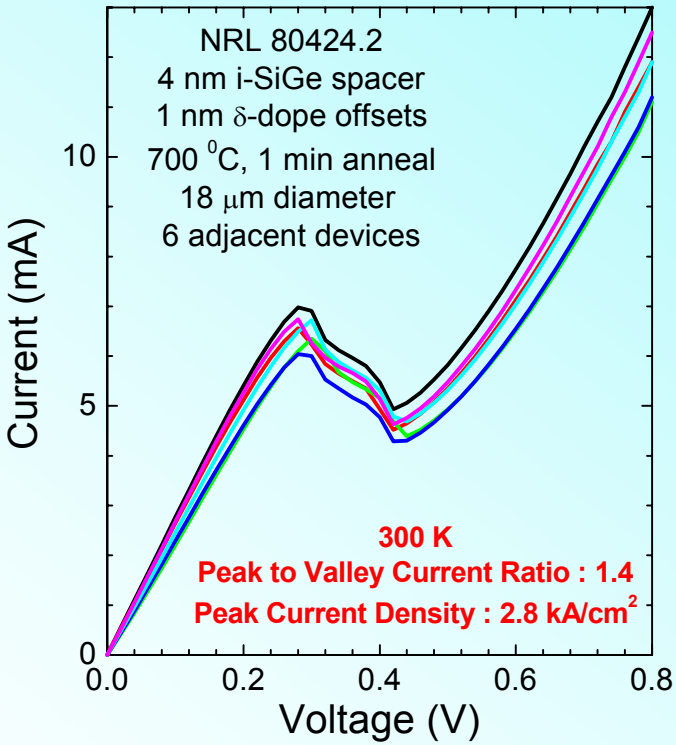
A 'TUNNEL' VISION for faster circuitry nears reality, researchers say.

In 1957, Nobel laureate Leo Esaki discovered that electrons could "tunnel" through solid barriers via tiny electrical devices and the "semiconductor tunnel diode" was born. Now, researchers at the University of Delaware, the Naval Research Laboratory and Raytheon Systems Co. say they can mass-produce tunnel diodes on silicon wafers, advancing the possibility of broad commercial use.

"This is the first tunnel diode that is compatible with a silicon integrated-circuit process," says Alan Seabaugh, a Raytheon scientist. The new tunnel diodes will replace previously cumbersome ones, allowing them to meld with high-tech transistors on chips, says Prof. Paul Berger of Delaware. Initial uses could include high-speed data-transfer, such as converting analog data to digital format in radar receivers.

Down the road, the new technology could mean fewer battery recharges for laptops and other consumer devices.

World's First Si-Based Resonant Interband Tunnel Diode (1998)



- Low growth temperature (320 °C)
- CMOS process compatibility

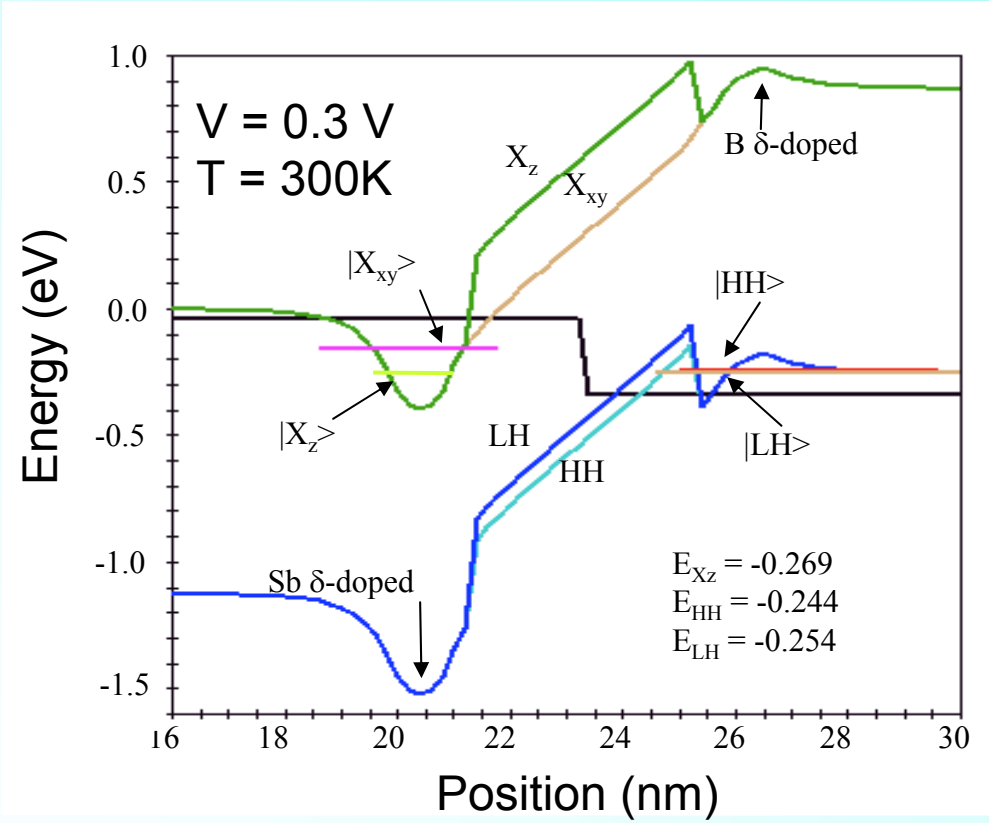
100 nm n+ Si
Sb-delta doping plane
1 nm undoped Si
4 nm undoped $Si_{0.5}Ge_{0.5}$
1 nm undoped Si
B-delta doping plane
100 nm p+Si
p+ Si substrate

"Room Temperature Operation of Epitaxially Grown $Si/Si_{0.5}Ge_{0.5}/Si$ Resonant Interband Tunneling Diodes," Sean L. Rommel, Thomas E. Dillon, M. W. Dashiell, H. Feng, J. Kolodzey, Paul R. Berger, Phillip E. Thompson, Karl D. Hobart, Roger Lake, Alan C. Seabaugh, Gerhard Klimeck, and Daniel K. Blanks, *Appl. Phys. Lett.*, **73**, pp. 2191-2193 (1998).

MBE Heterostructure

Modeling of First RITD Band Diagram

Roger Lake, now at UC Riverside



- 33% of dopants are assumed active
- Calculated by solving the effective mass Schrödinger equation and iterating to converge with Poisson's equation.
- 0.3 V taken to be the peak voltage

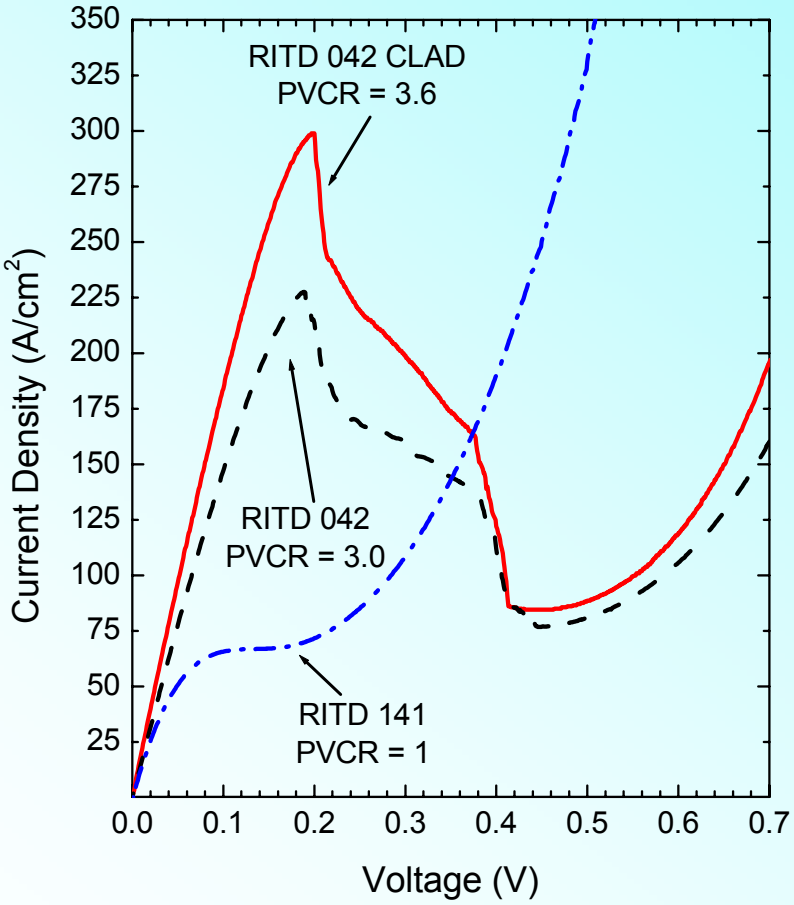
- **δ-doping allows degeneracy condition to be satisfied**
- **δ-doping can provide QWs that allow resonant interband tunneling**

5 Key Features of the Original RITD Design

- An **intrinsic layer** is used as the central tunneling spacer, which reduces carrier scattering. Both Si and $Si/Si_{1-x}Ge_x$ composite spacers have been explored. The addition of Ge provides greater momentum mixing and therefore higher current densities.
- A pair of **δ-doping planes of B and P (or Sb)** provide highly degenerate doping levels which can confine quantum states in potential energy wells. The gap between δ-doping planes is assumed the tunneling distance.
- Fixed **offsets between the δ-doping planes and the tunneling spacer** were introduced in some SiGe designs to minimize the outdiffusion of dopants and impurity accumulation into the central tunneling spacer.
- Samples were epitaxially grown by **low-temperature molecular beam epitaxy (LT-MBE)** to allow for greater dopant incorporation and abrupt interfaces minimizing segregation and diffusion.
- Short post growth **rapid thermal annealing (RTA) heat treatments** were introduced to reduce the point defect density associated with low temperature growth. Diffusion during annealing may decrease the spacer thickness and reduce as-grown δ-doping levels.

- "Si-Based Resonant Interband Tunneling Diodes," Paul R. Berger, Sean L. Rommel, Phillip E. Thompson, Karl D. Hobart, and Roger Lake, [Issued on October 12, 2004, U. S. Patent #6,803,598].
- "Method of Making Interband Tunneling Diodes," Paul R. Berger, Sean L. Rommel, Phillip E. Thompson, Karl D. Hobart, and Roger Lake, (USPTO Application #20030049894, Filed on August 21, 2001).

Isothermal Annealing Effects with Cladding

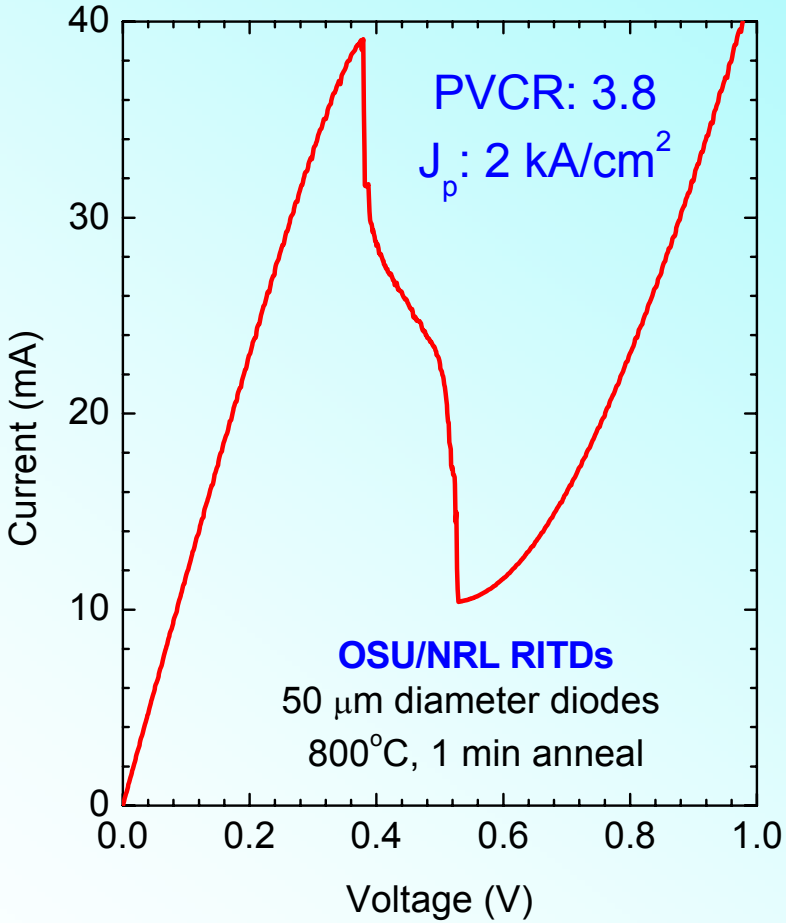


Diffusion barrier cladding surrounding the δ-doping spike raises the process thermal budget and allows for greater defect annihilation before interdiffusion becomes serious

"Diffusion Barrier Cladding in Si/SiGe Resonant Interband Tunneling Diodes And Their Patterned Growth on PMOS Source/Drain Regions," Niu Jin, Sung-Yong Chung, Anthony T. Rice, Paul R. Berger, Phillip E. Thompson, Cristian Rivas, Roger Lake, Stephen Sudirgo, Jeremy J. Kempisty, Branislav Curanovic, Sean L. Rommel, Karl D. Hirschman, Santosh K. Kurinec, Peter H. Chi and David S. Simons, *Special Issue on "Nanoelectronics" in IEEE Trans. Elect. Dev.*, ***vol. 50****, pp. 1876-1884 (September 2003).*

Annealed 825 °C for 1 minute

High Peak-to-Valley Current Ratios



$Si/Si_{0.6}Ge_{0.4}/Si$ RITDs Grown at 320 °C

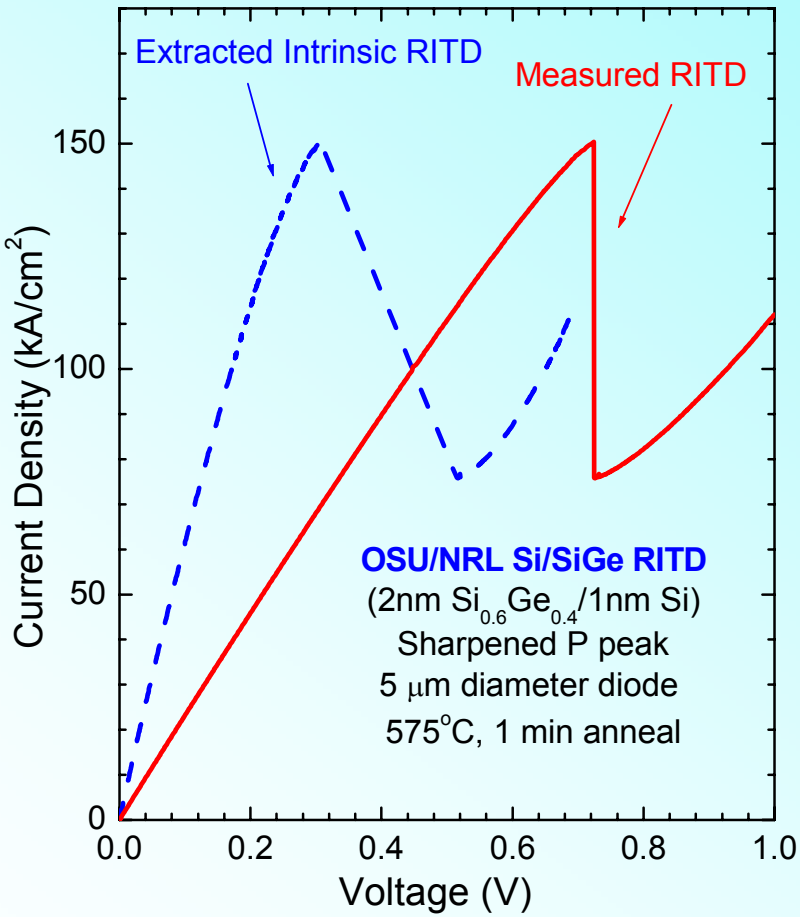
100 nm n+ Si
P δ-doping plane
2 nm undoped Si
4 nm undoped $Si_{0.6}Ge_{0.4}$
B δ-doping plane
1 nm undoped $Si_{0.6}Ge_{0.4}$
100 nm p+ Si
p+ Si substrate

Tunnel Barrier

MBE Heterostructure

Greater defect annihilation leads to less excess current in valley region and therefore higher PVCRs

Very High Peak Current Densities



$Si/Si_{0.6}Ge_{0.4}/Si$ RITDs Grown at 320 °C

Tunnel Barrier

100 nm n+ Si
P δ-doping plane
1 nm undoped Si
2 nm undoped $Si_{0.6}Ge_{0.4}$
B δ-doping plane
1 nm undoped $Si_{0.6}Ge_{0.4}$
100 nm p+ Si
p+ Si substrate

*"151 kA/cm² Peak Current Densities in Si/SiGe Resonant Interband Tunneling Diodes for High-Power Mixed-Signal Applications," Niu Jin, Sung-Yong Chung, Anthony T. Rice, Paul R. Berger, Ronghua Yu, Phillip E. Thompson, and Roger Lake., Appl. Phys. Lett., **83**, 3308 (2003).*

By reducing tunnel barrier, over 150 kA/cm² current density!

High current densities valuable for fast switching and RF Mixed Signals

National Science Foundation Celebrating 50 Years

NSF Press Release on High J_p RITDs

News Tip

January 15, 2004

For more information on these science news and feature story tips, contact the public information officer listed at (703) 292-8070. Editor: **Josh Chamot**

Contents of this News Tip:

Researchers Break Electronics Speed Record
New diode may lead to new generation of faster, cheaper, smaller electronics

Engineers have fused a 1950s concept with modern semiconductor processing and design to create a diode that can move electrical current at record-breaking rates.

At room temperature, the diode (a device that behaves like a valve for electricity traveling within a circuit) can transmit current equivalent to 151,000 amps per square centimeter, three times the rate of its closest competitors. For comparison, standard wiring in a home carries a maximum current density of only 700 amps per square centimeter.

Known in the research community as a "resonant interband tunneling diode," the silicon-based semiconductor has applications in computers and other electronic devices, and may eventually boost cellular phone signals to reach communications towers now beyond their range.

Paul Berger, Niu Jin (lead author) and their colleagues at Ohio State University in Columbus, Phillip Thompson at the Naval Research Laboratory in Washington, D.C., and Roger Lake at the University of California at Riverside announced their world current record in the journal *Applied Physics Letters*.

The researchers developed the diode with the support of the National Science Foundation (NSF), the independent federal agency that supports fundamental research and education across all fields of science and engineering.

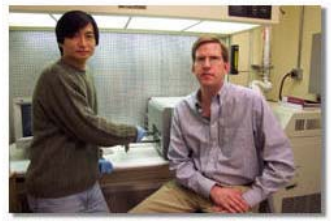
Tunneling diodes have been around since the late 1950's when Leo Esaki, then at Sony Corp. in Japan, discovered that a property called tunneling can increase a diode's output current. Esaki later won the Nobel Prize, in part for this work.

Tunneling is a process that takes place at the level of the atom, in the realm of quantum physics. At that scale, the familiar rules of classical physics that guide rocket design, snowfall and baseball give way to less intuitive rules based on probability, waves and energy packets.

Under the rules of quantum physics, an electron on one side of a barrier can travel through to the other side, "which would be like a tennis ball coming out the other side of a brick wall," says Berger. The property is called tunneling, and while somewhat mysterious, researchers have been taking advantage of the phenomenon for years, although only in niche applications.

By tweaking the properties of semiconductors, researchers can create materials that increase the chances that tunneling will occur. Berger and his team have optimized the diode design and the process for creating the device with few imperfections. The researchers also developed a manufacturing process to create tunneling diodes that, in addition to being incredibly fast, are silicon-based and easy to mass produce.

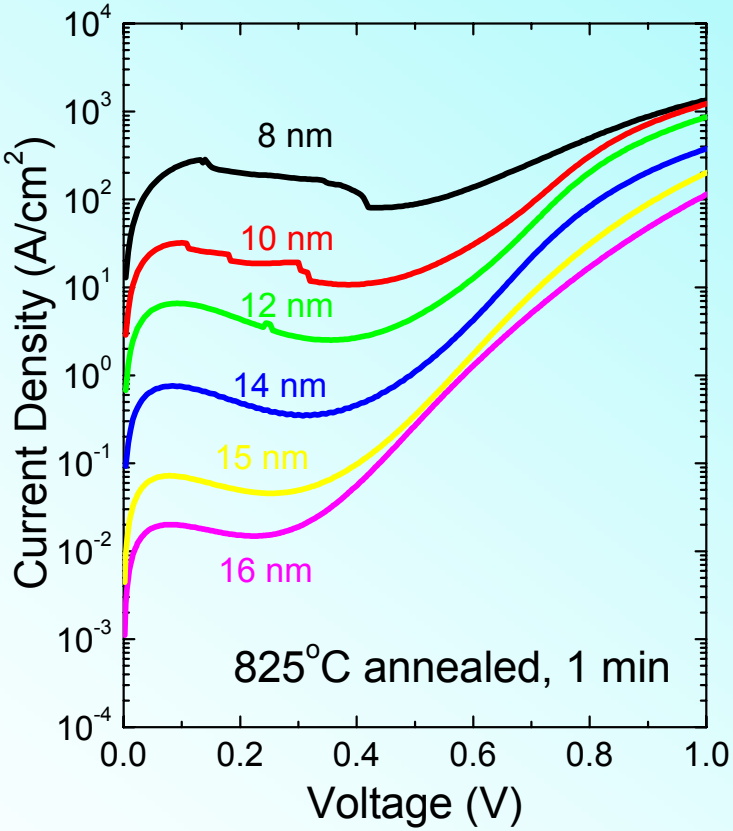
The original tunnel diodes were difficult to mass produce and were not compatible with the silicon-based microchips that run



Niu Jin and Paul Berger next to the rapid thermal annealing system used in their research.
Credit: Paul Berger, Ohio State University, NSF
Select image for larger version
(Size: 956KB)

Dr. Phillip E. Thompson of the Naval Research Laboratory next to his molecular beam epitaxy system.
Credit: Phillip E. Thompson, Naval Research Laboratory
Select image for larger version
(Size: 729KB)

Very Low Peak Current Densities



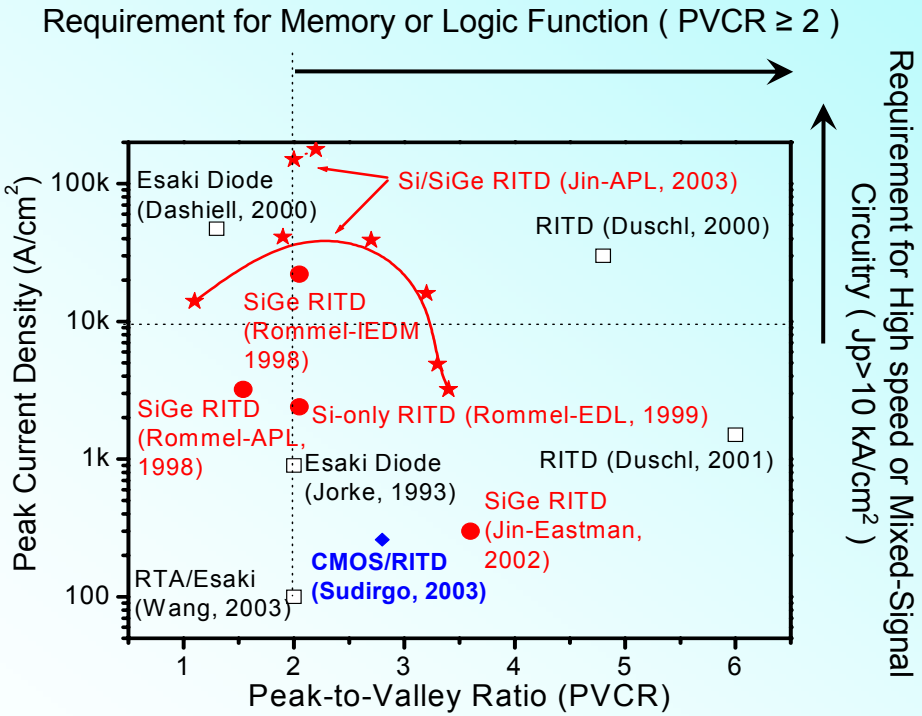
Current densities can be engineered over ~7 orders of magnitude by controlling RITD spacer thickness between the δ-doping pair from 1 nm up to 16 nm.

By widening spacer, below 20 mA/cm^2 current density!

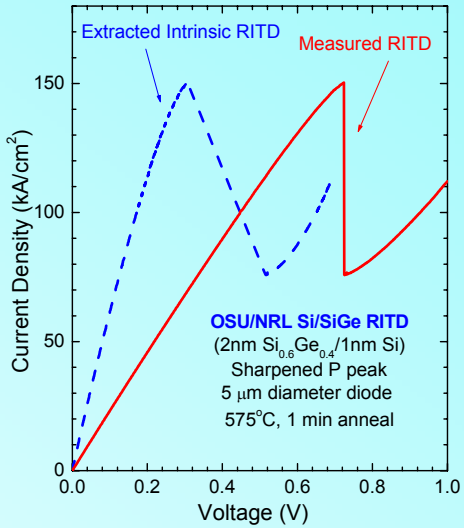
Low current densities valuable for memory and low power consumption

RF Mixed Signal Applications Enabled

Results highlighted here demonstrate the highest reported peak current density for Si-based interband tunnel diodes that is 3 times larger than the previous world record. A high current density is needed to generate large amounts of microwave power output for radio transmission in small distributed sensor networks

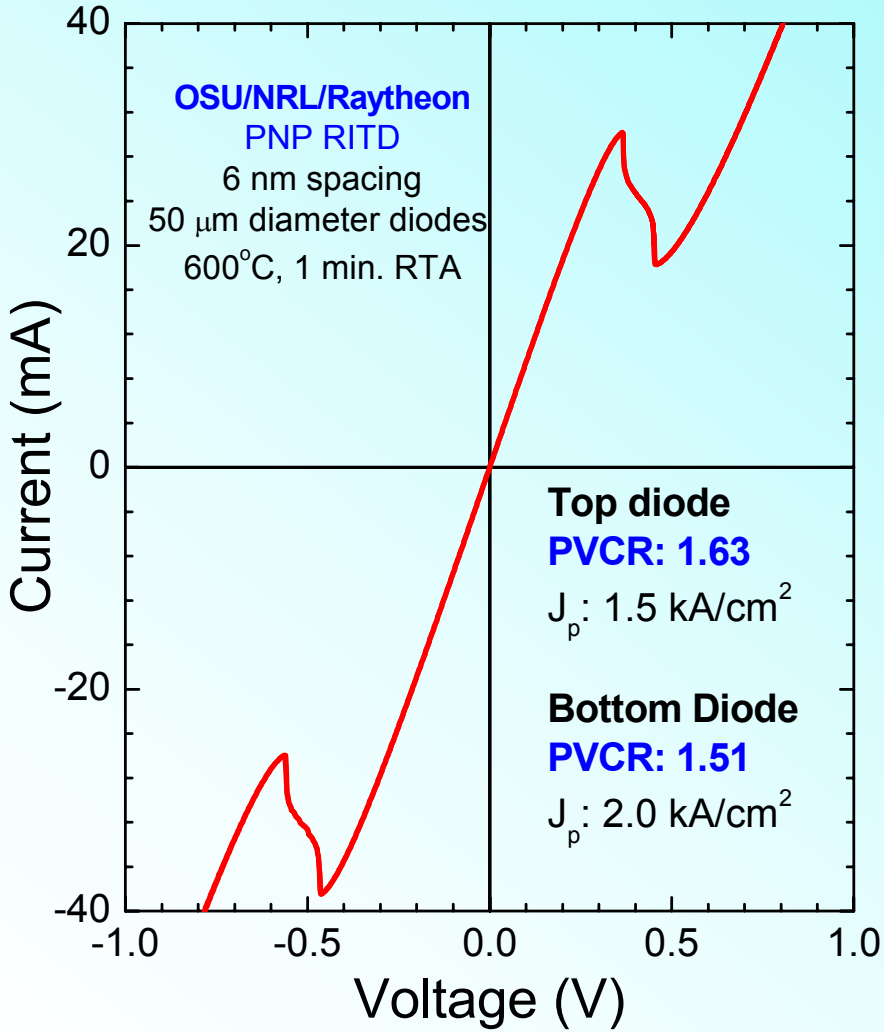


Solid circles (●) indicate prior work by Berger group, open squares (□) indicate prior work by other groups, and stars (*) indicate recent work by Berger group.

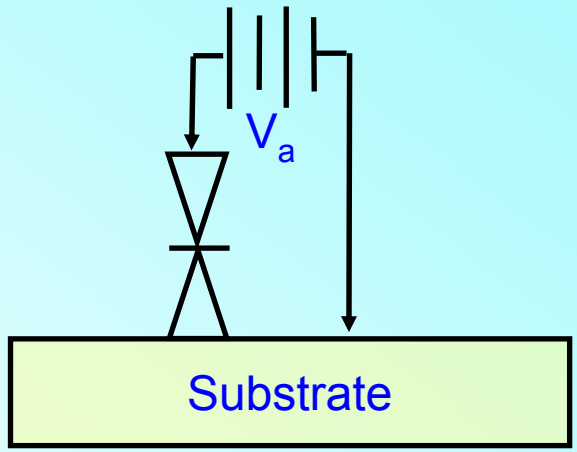


*"151 kA/cm² Peak Current Densities in Si/SiGe Resonant Interband Tunneling Diodes for High-Power Mixed-Signal Applications," Niu Jin, Sung-Yong Chung, Anthony T. Rice, Paul R. Berger, Ronghua Yu, Phillip E. Thompson, and Roger Lake., Appl. Phys. Lett., **83**, 3308 (2003).*

Back-to-back RITDs provide symmetric NDR

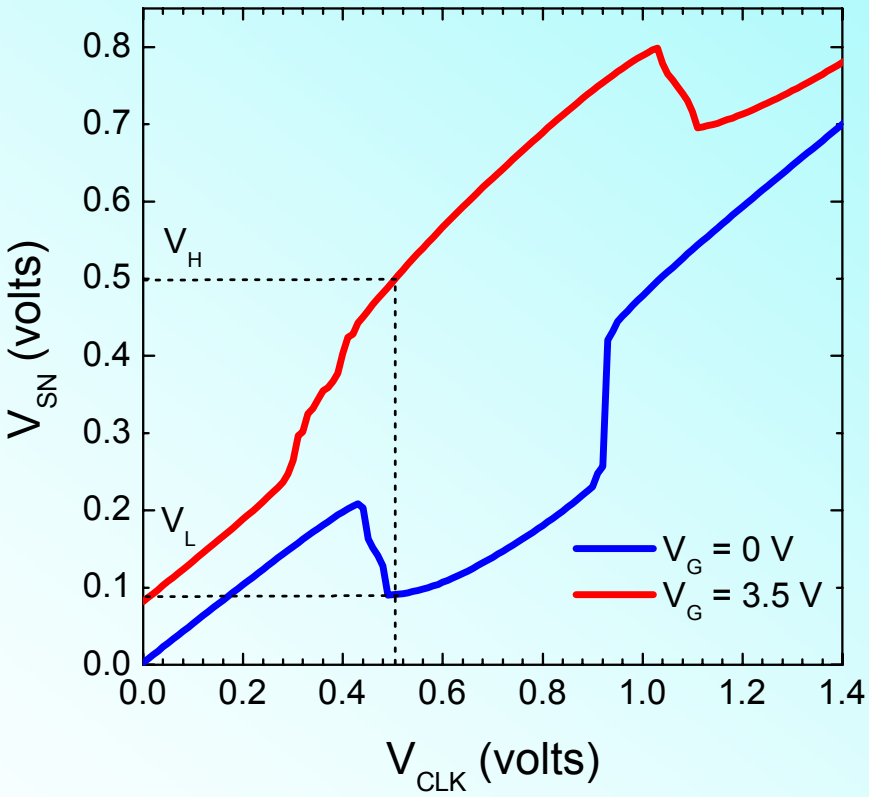


Two NDR regions are achieved by vertically stacking 2 RITDs, being careful to minimize dopant segregation into top RITD



*"A PNP Si Resonant Interband Tunnel Diode with Symmetrical NDR," Niu Jin, Paul R. Berger, Sean L. Rommel, Phillip E. Thompson, and Karl D. Hobart, Electronics Letters, **37**, pp. 1412-1414 (2001).*

Monolithic Integration of RITDs with CMOS



- In cooperation with Rochester Institute of Technology (RIT), RIT reports the first Si/SiGe RITDs are monolithically integrated with Si CMOS.
- Functional MOBILE latches are also realized.

*"Monolithically Integrated Si/SiGe Resonant Interband Tunnel Diode/CMOS Demonstrating Low Voltage MOBILE Operation," S. Sudirgo, R.P. Nandgaonkar, B. Curanovic, J.L. Hebding, R.L. Saxer, S.S. Islam, K.D. Hirschman, S.L. Rommel, S.K. Kurinec, P.E. Thompson, N. Jin, and P.R. Berger, Solid State Electronics, **48**, pp. 1907-1910 (2004).*

Low Voltage Operation to Reduce Power Consumption

Voltage at sense node vs. applied clock voltage of a NMOS-RITDs MOBILE latch with 84% voltage swing of the applied V_{CLK} at 0.5 V.

National Science Foundation Celebrating 50 Years

Integration of RITDs with SiGe HBTs

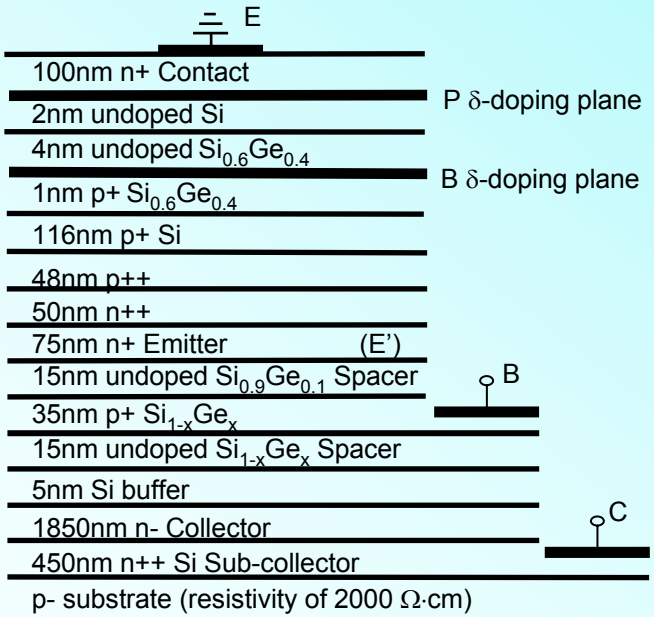


Fig 1. Layer structure of the SiGe RITD with SiGe HBT.

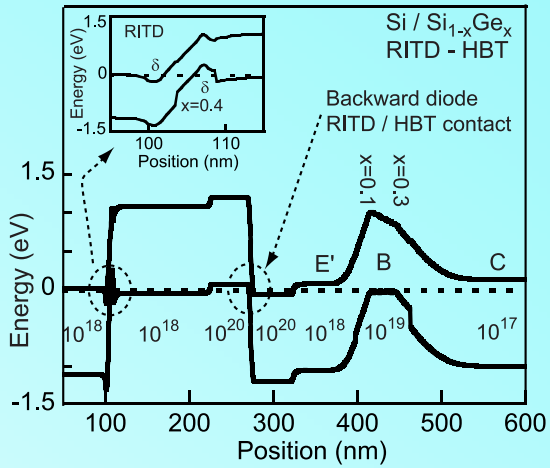


Fig 2. Band diagram of RITD / HBT.

"3-Terminal Si-Based Negative Differential Resistance Circuit Element with Adjustable Peak-To-Valley Current Ratios Using a Monolithic Vertical Integration," Sung-Yong Chung, Niu Jin, Paul R. Berger, Ronghua Yu, Phillip E. Thompson, Roger Lake, Sean L. Rommel and Santosh K. Kurinec, *Applied Physics Letters*, **84**, pp. 2688-2690 (2004).

- The first Si/SiGe RITDs are monolithically integrated with SiGe heterojunction bipolar transistors (HBT) by vertically stacking the RITD atop the HBT.

HBT-RITD: Three Terminal NDR Device Provides Adjustable PVCR

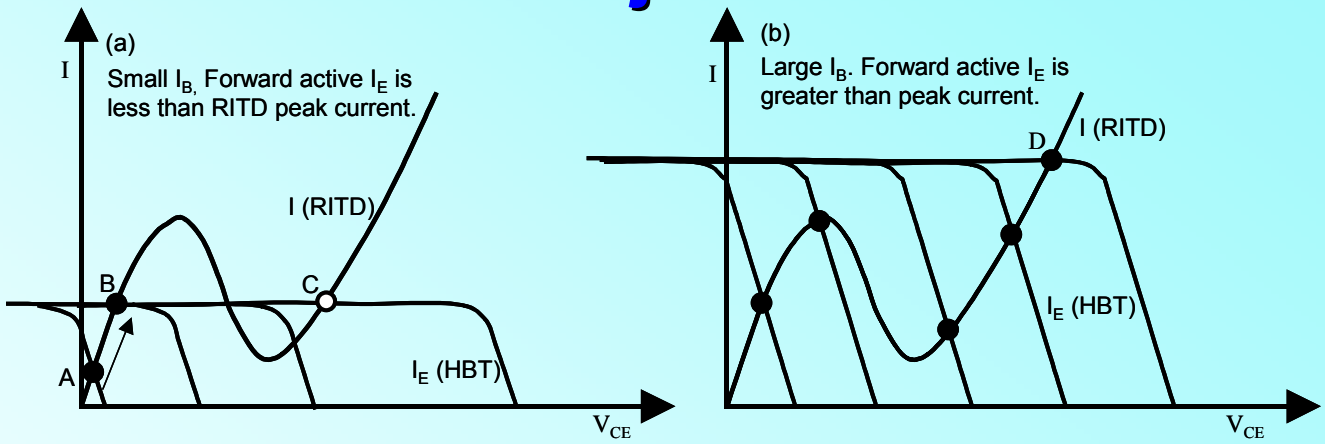
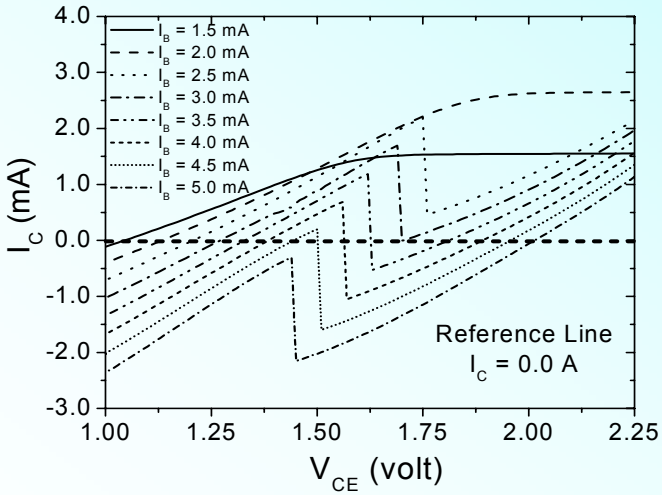


Fig. 3. RITD and HBT emitter current load lines for fixed base current, I_B. (a) Low I_B with bistable latching behavior. (b) Large I_B with infinite PVCR in I_C.

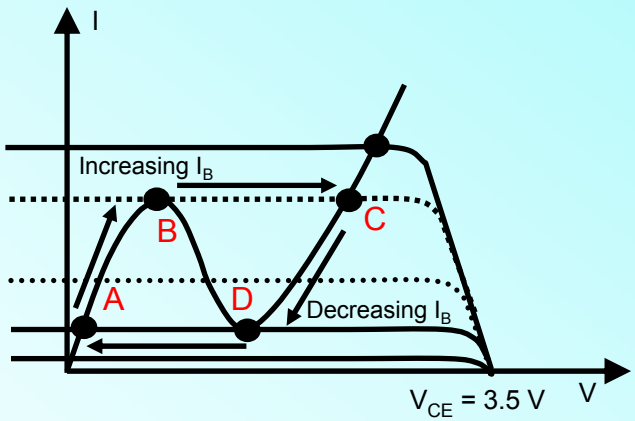


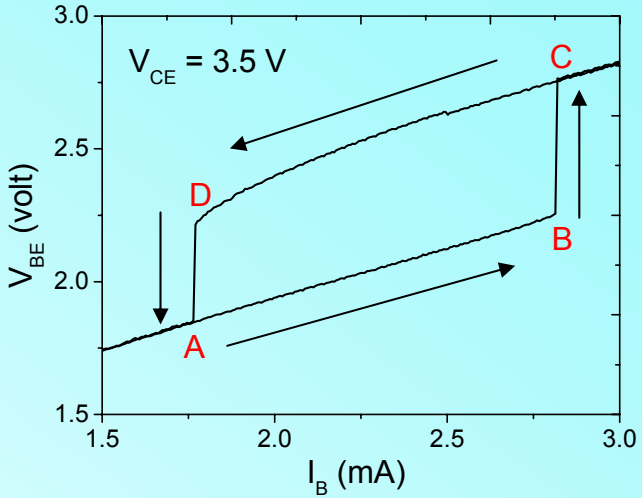
"Monolithic Vertical Integration of Si/SiGe HBT and Si-Based Resonant Interband Tunneling Diode Demonstrating Latching Operation and Adjustable Peak-To-Valley Current Ratios," Sung-Yong Chung, Niu Jin, Ronghua Yu, Paul R. Berger, Phillip E. Thompson, Roger Lake, Sean L. Rommel and Santosh K. Kurinec, *2003 Int. Elect. Dev. Meet. Tech. Dig., pp. 296-299.*

Finalist for Best Student Paper Award!

Fig 4. I-V characteristics measured demonstrate PVCR, PCD and even the voltage span can be controlled.

HBT-RITD: Latching Properties





Latch property: Bi-stability with I_B between I_{PEAK} and I_{VALLEY} of RITD

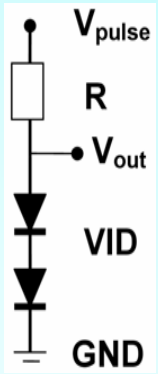
"3-Terminal Si-Based Negative Differential Resistance Circuit Element with Adjustable Peak-To-Valley Current Ratios Using a Monolithic Vertical Integration," Sung-Yong Chung, Niu Jin, Paul R. Berger, Ronghua Yu, Phillip E. Thompson, Roger Lake, Sean L. Rommel and Santosh K. Kurinec, *Applied Physics Letters*, **84**, pp. 2688-2690 (2004).

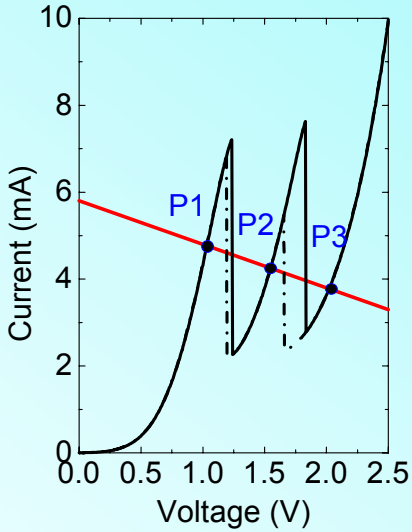
Switching operation:

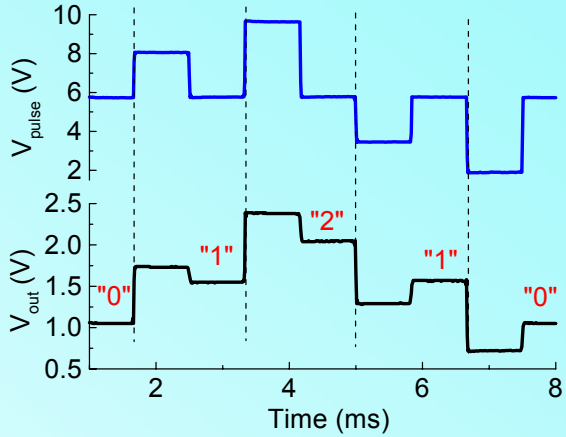
Low (B) → High (C) with the increase of I_B

High (D) → Low (A) with the decrease of I_B

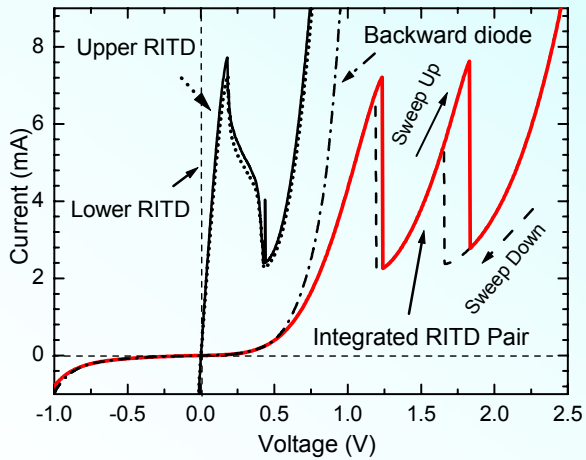
Multi-valued Quantum Logic For Compact and Energy Efficient Circuitry







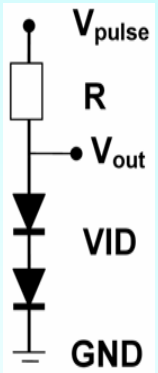
Reduced device count potential.

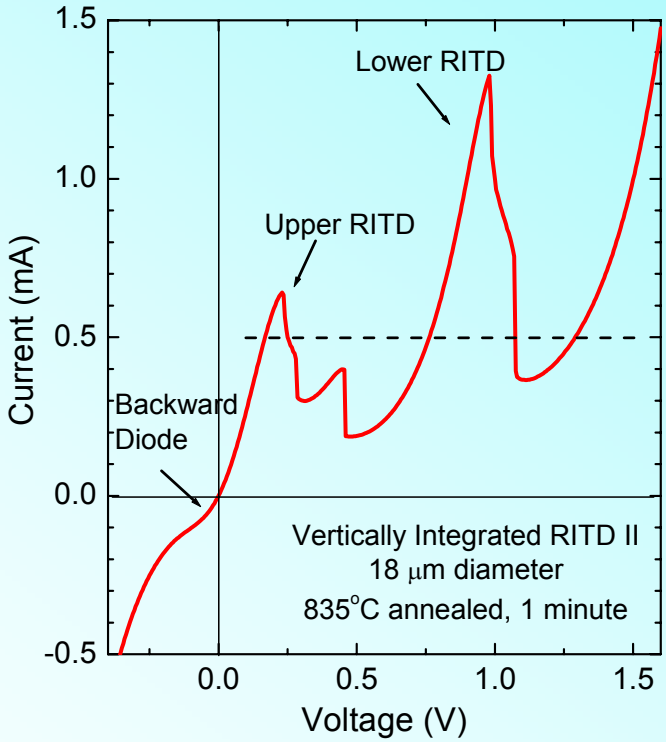


However, there is a large series resistance created by the vertical stacking and a lower noise margin from P2 → P3 than P1 → P2

"Tri-State Logic Using Vertically Integrated Si Resonant Interband Tunneling Diodes with Double NDR," Niu Jin, Sung-Yong Chung, Roux M. Heyns, Paul R. Berger, Ronghua Yu, Phillip E. Thompson, and Sean L. Rommel, *IEEE Elect. Dev. Lett.*, **25**, pp. 646-648 (September 2004).

Multi-valued Quantum Logic For Compact and Energy Efficient Circuitry





- The large peak voltage shift observed earlier in vertically integrated RITD pairs is now greatly reduced. No hysteresis was observed in the NDR region.
- Large peak current and valley current differences were observed, which makes the modified RITD pair more suitable for circuit implementation using a constant-current-source load.
- The upper diode shows a PVCR of 3.5 with J_p of 155 A/cm^2, and the lower diode shows a PVCR of 3.6 with J_p of 515 A/cm^2.

Improved operational voltage and increased noise margin

"Improved Vertically Stacked and Serially Connected Si/SiGe Resonant Interband Tunneling Diode Pair Showing Small Peak Shift and Unequal Peak Currents," Niu Jin, Sung-Yong Chung, Ronghua Yu, Paul R. Berger, and Phillip E. Thompson, *Electronics Letters*, **40**, pp. 1548-1549 (November 25, 2004).

Key Results of Our Effort

- Demonstration of **room temperature NDR** in **epitaxially grown** families of Si-based tunnel diodes.

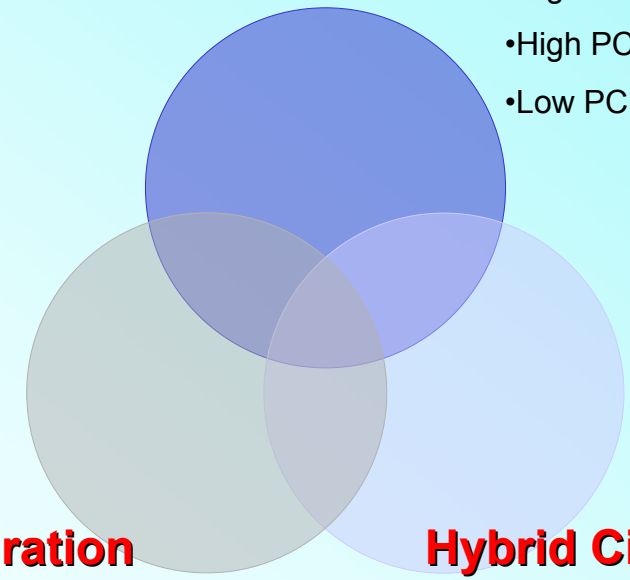
- Devices have shown **PVCRs up to 3.8** and the peak current density can be engineered from **high current densities ($\geq$150 kA/cm^2) to low current densities ($\leq$20 mA/cm^2)**.

- **Si-based RITDs have been monolithically integrated with CMOS and SiGe HBT processing for efficient and low power consumption circuitry.**

Si-Based RITD Results Summary

Device Optimization

- High PVCR (3.8)
- High PCD (≥ 150 kA/cm^2)
- Low PCD (≤ 20 mA/cm2)



Device Integration

- Monolithic integration with CMOS
- Monolithic Integration with SiGe HBTs

Hybrid Circuit Prototyping

- Vertically stacked back-to-back RITDs for symmetric NDR
- Tri-state logic with vertically stacked RITDs
- Low voltage MOBILE latches (CMOS-RITD)
- Adjustable PVCR (HBT-RITD)

For Further Reading

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