Ideal Digital to Analog Conversion

- The analog output signal, $\mathbf{V_{out}}$, is related to the digital signal, $\mathbf{B_{in}}$, through an analog reference signal, $\mathbf{V_{ref}}$.

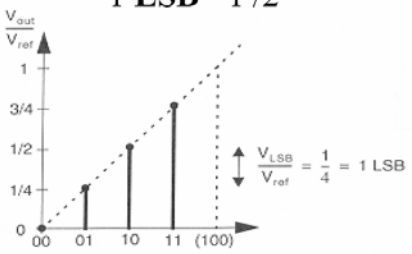
$$\mathbf{V_{out}} = \mathbf{V_{ref}}\,(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}) = \mathbf{V_{ref}}\,\mathbf{B_{in}}$$

- $\mathbf{V_{LSB}}$ is defined to be the voltage change when one LSB changes.

$$\mathbf{V_{LSB}} \equiv \mathbf{V_{ref}} / \mathbf{2^N}$$

- The definition of **LSB** units:

$$1\ \mathbf{LSB} = 1/2^N$$



- Maximum value of $\mathbf{V_{out}}$

$$\mathbf{V_{out}} = \mathbf{V_{ref}}\,(1 - 2^{-N})$$

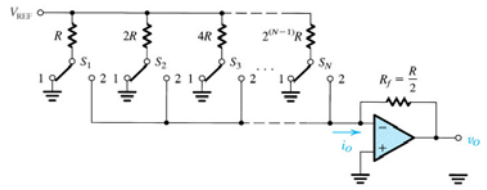
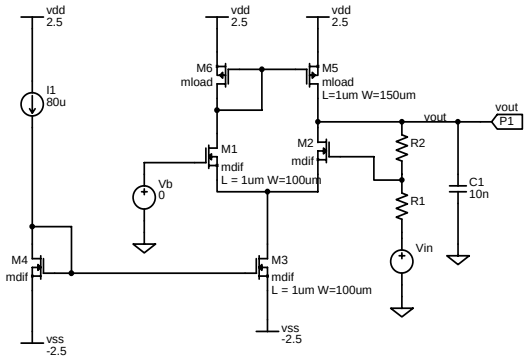
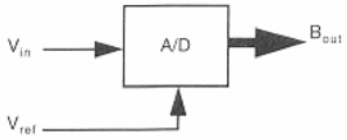


Figure 9.39 An *N*-bit D/A converter using a binary-weighted resistive ladder network.



Ideal A/D Converter

- $\mathbf{B_{out}}$ is defined to be the digital output word.
- $\mathbf{V_{in}}$ and $\mathbf{V_{ref}}$ are the analog input and reference signal respectively.

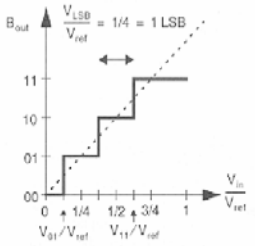


- For A/D converter:

$$\mathbf{V_{ref}}\,(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}) = \mathbf{V_{in}} \pm \mathbf{V_x}$$

where

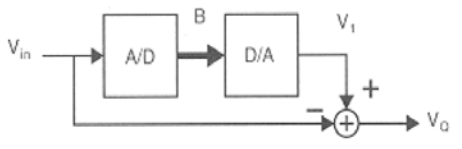
$$-\frac{1}{2}V_{LSB} \le V_X \le \frac{1}{2}V_{LSB}$$



Quantization noise

The quantized signal, V_1, can be modelled as the input signal, V_{in}, plus some additive quantization noise signal, V_Q.

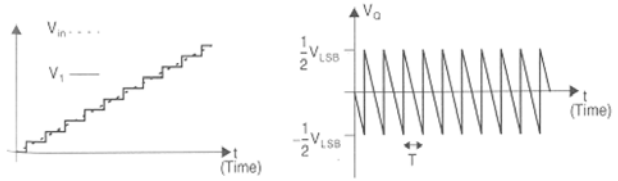
$$V_1 = V_{in} + V_Q$$



Quantization noise

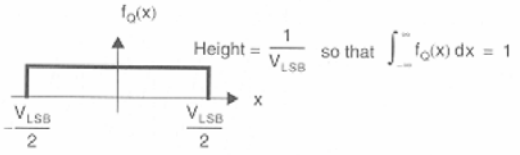
$$V_{Q(rms)} = \left[\frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} V_Q{}^2\,dt\right]^{1/2} = \left[\frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} V^2{}_{LSB}\left(\frac{-t}{T}\right)^2 dt\right]^{1/2}$$

$$= \left[\frac{V^2{}_{LSB}}{T^3}\left(\frac{t^3}{3}\Big|_{\frac{-T}{2}}^{\frac{T}{2}}\right)\right]^{1/2}$$



Stochastic approach

The probability density function for an error signal, $f_Q(x)$, will be constant value, as shown below:



- The average value of the quantization error, $V_{Q(avg)}$, is found to be zero as follows:

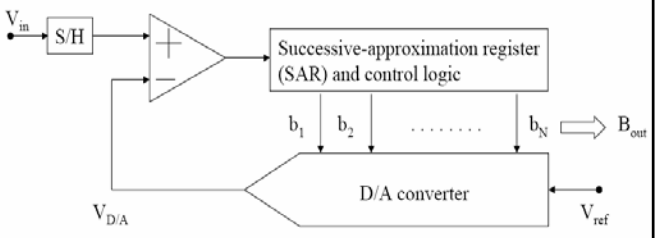
$$V_{Q(avg)} = \int_{-\infty}^{\infty} x\, f_Q(x)dx = \frac{1}{V_{LSB}}\left(\int_{-V_{LSB}/2}^{V_{LSB}/2} x\, dx \right) = 0$$

- In a similar fashion, the rms value of the quantization error is given by:

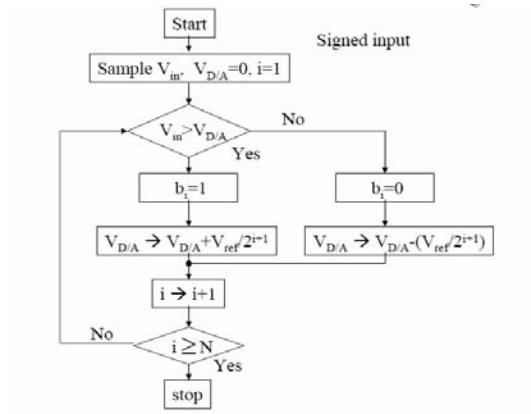
$$V_{Q(avg)} = \left(\int_{-\infty}^{\infty} x^2\, f_e(x)dx \right)^{1/2} = \frac{V_{LSB}}{\sqrt{12}}$$

Table 11.1 Some 4-bit signed digital representations

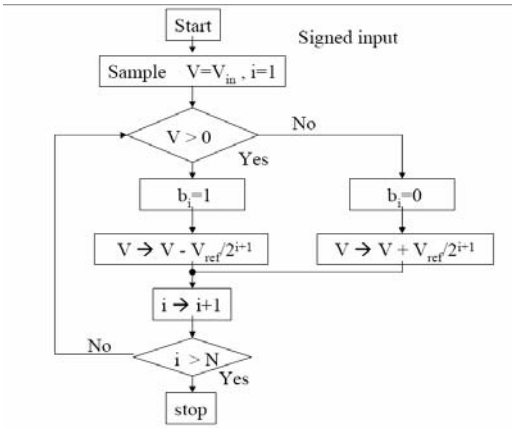
Number	Normalized number	Sign magnitude	1's complement	Offset binary	2's complement
+7	+7/8	0111	0111	1111	0111
+6	+6/8	0110	0110	1110	0110
+5	+5/8	0101	0101	1101	0101
+4	+4/8	0100	0100	1100	0100
+3	+3/8	0011	0011	1011	0011
+2	+2/8	0010	0010	1010	0010
+1	+1/8	0001	0001	1001	0001
+0	+0	0000	0000	1000	0000
(−0)	(−0)	(1000)	(1111)		
−1	−1/8	1001	1110	0111	1111
−2	−2/8	1010	1101	0110	1110
−3	−3/8	1011	1100	0101	1101
−4	−4/8	1100	1011	0100	1100
−5	−5/8	1101	1010	0011	1011
−6	−6/8	1110	1001	0010	1010
−7	−7/8	1111	1000	0001	1001
−8	−8/8			0000	1000

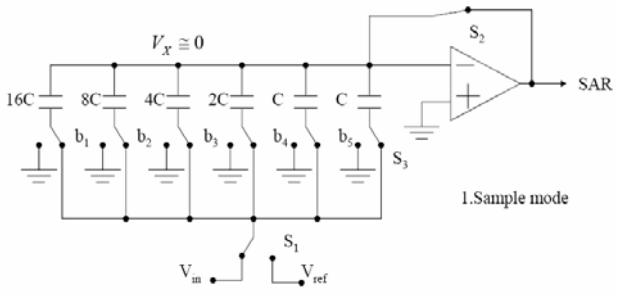


D/A converter-based successive-approximation converter

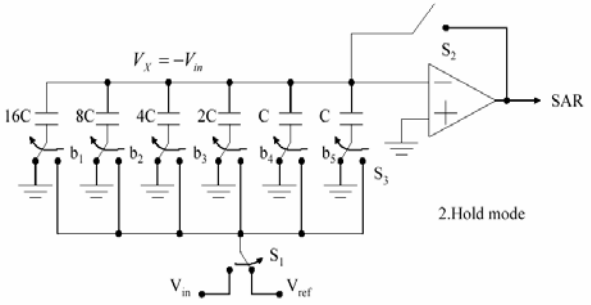


Flow graph for the successive-approximation approach

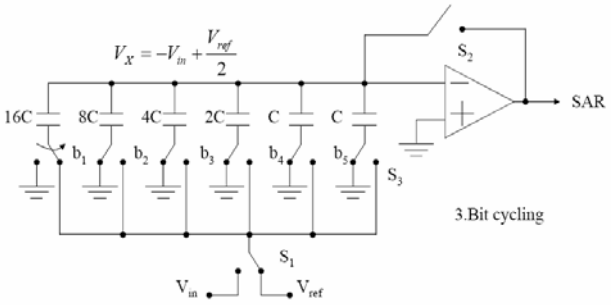




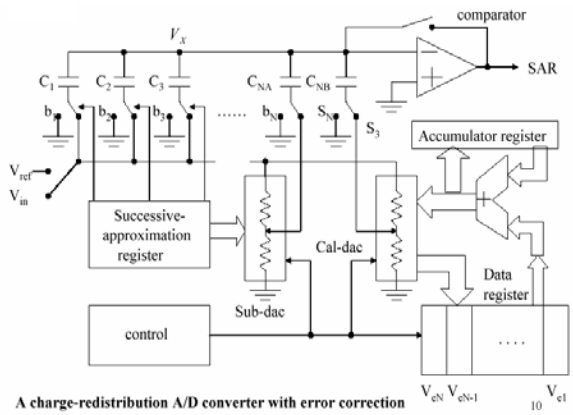
A 5-bit unipolar charge-redistribution A/D converter



A 5-bit unipolar charge-redistribution A/D converter



A 5-bit unipolar charge-redistribution A/D converter



A charge-redistribution A/D converter with error correction

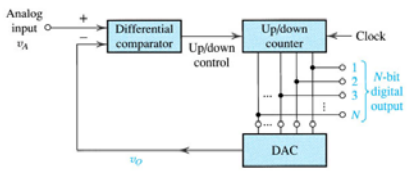
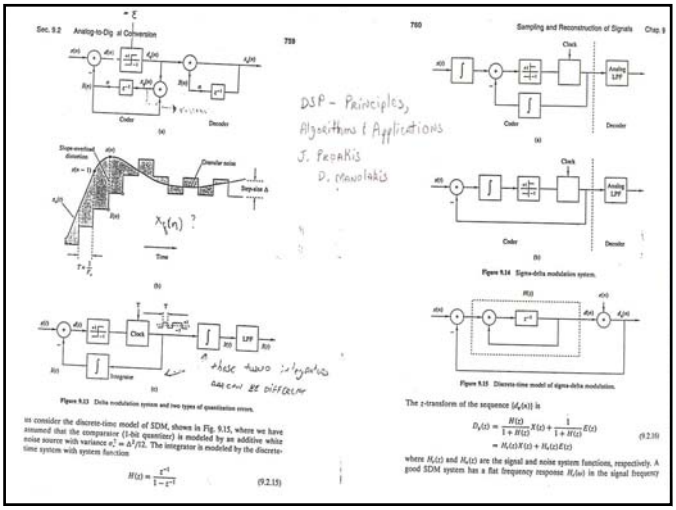


Figure 9.43 A simple feedback-type A/D converter.



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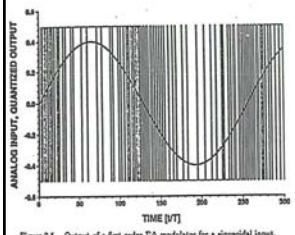

Figure 2.5. Output of a first-order ΣΔ modulator for a sinusoidal input.

A/D converters is a function of ratio of the sampling rate to the bandwidth of the converter. Unlike the case for Nyquist rate converters, the resolution of oversampled A/Ds can be improved without increasing the number of levels of the quantizer.

2.3 Modulators for Oversampled A/D Conversion

2.3.1 Classification

The quantizer in an A/D converter replaces the analog input signal by the closest of a set of discrete reference levels r_i (Figure 2.6). The quantization error e is defined as the difference between the quantizer input, u, and the value of the output, v, and is a measure of the quantizer's precision. The modulator in an oversampled A/D

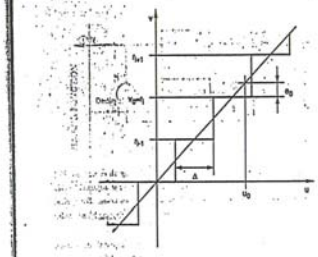

Figure 2.6. Quantizer input-output relationship. The output value v_0 and error e for a sample input u_0 are indicated in the plot.

converter reduces the quantization noise within the signal baseband, for a quantizer with given resolution, through use of feedback and sampling at a rate higher than the Nyquist frequency. Two general approaches can be used to achieve this goal: prediction or noise shaping. Predictive modulators spectrally shape the signal as well as quantize it. Noise shaping modulators simply shape the spectrum of the noise without altering the signal spectrum.

The block diagram in Figure 2.7 illustrates the basic architecture of a predictive modulator. The predictor can be realized as an analog or digital circuit. In either case, a D/A converter is required; it either follows or precedes the predictor and has been omitted in the block diagram of Figure 2.7. Predictive modulators reduc

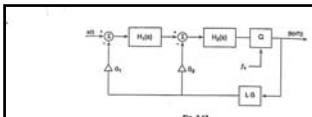

Fig. 8.18
Splitting H(s) to obtain a double-loop ΔΣM

8.4 ΔΣM STRUCTURES

8.4.1 A Typical ΔΣM Circuit

One of the nice features of a ΔΣM is its simplicity of implementation. A first-order ΔΣM is shown in Fig. 8.19.

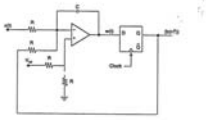

Fig. 8.19
A simple ΔΣM circuit

A single-bit ΔΣM can be constructed using a simple D-type edge-triggered flip-flop, an op-amp and a few discrete components. The comparator and level generator functions are implemented by the flip-flop itself. Note that the "level generator" provides levels of $+V_{ref}$ and 0 rather than +B and –B. This asymmetry is automatically compensated for by the closed-loop nature of the ΔΣM. With an actual flip-flop, such as a conventional 74HC74 device, the high and low voltages will not be quite +5 V and 0 V but the ΔΣM will self-bias itself such that the "zero-input" voltage at the op-amp output will be (nominally) 2.5 V, the decision threshold of the logic device. The input voltage range will be, nominally, [0, 5] volts. Because of the variability

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from device to device, the circuit in Fig. 8.19 is not used as is if the performance specifications and tolerance limits are stringent, but the circuit is very simple to construct and, apart from being a good demonstration of the ΔΣM concept, is surprisingly very good. For observing the behavior of the conversion process and examining the spectra of the noise, etc., a simple demodulator (lowpass filter) is shown in Fig. 8.20.

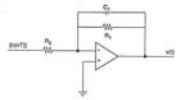

Fig. 8.20
A lowpass filter circuit to reconstruct the ΔΣM output in analog form

The output v(t) in of the circuit in Fig. 8.20 will contain a DC component because the input signal {b(nT)} is a logic level signal between $+V_{ref}$ and 0 V, but at other frequencies v(t) is representative of the analog equivalent of the digital representation, {b(nT)}, of the signal x(t). It is especially useful to observe v(t) in the frequency domain using a spectrum analyzer. Assuming that x(t) is a sinewave, the simplest form of test signal available in a laboratory environment, the spectrum of v(t) viewed on a spectral analyzer takes the form shown in Fig. 8.21.

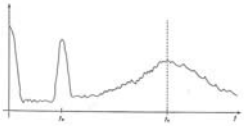

Fig. 8.21
Typical spectrum of a sinusoidal signal at frequency f_x using ΔΣM depicted in Fig. 8.19