The first comparator macro-model we consider is intended to model **a bipolar comparator**. Given the base emitter diode equation of the bipolar transistor, the current of the differential front end, can be described by the hyperbolic tangent equation 2.2. The resulting Spice model we propose is based on this simple equation and is shown in the figure 2 - 3.

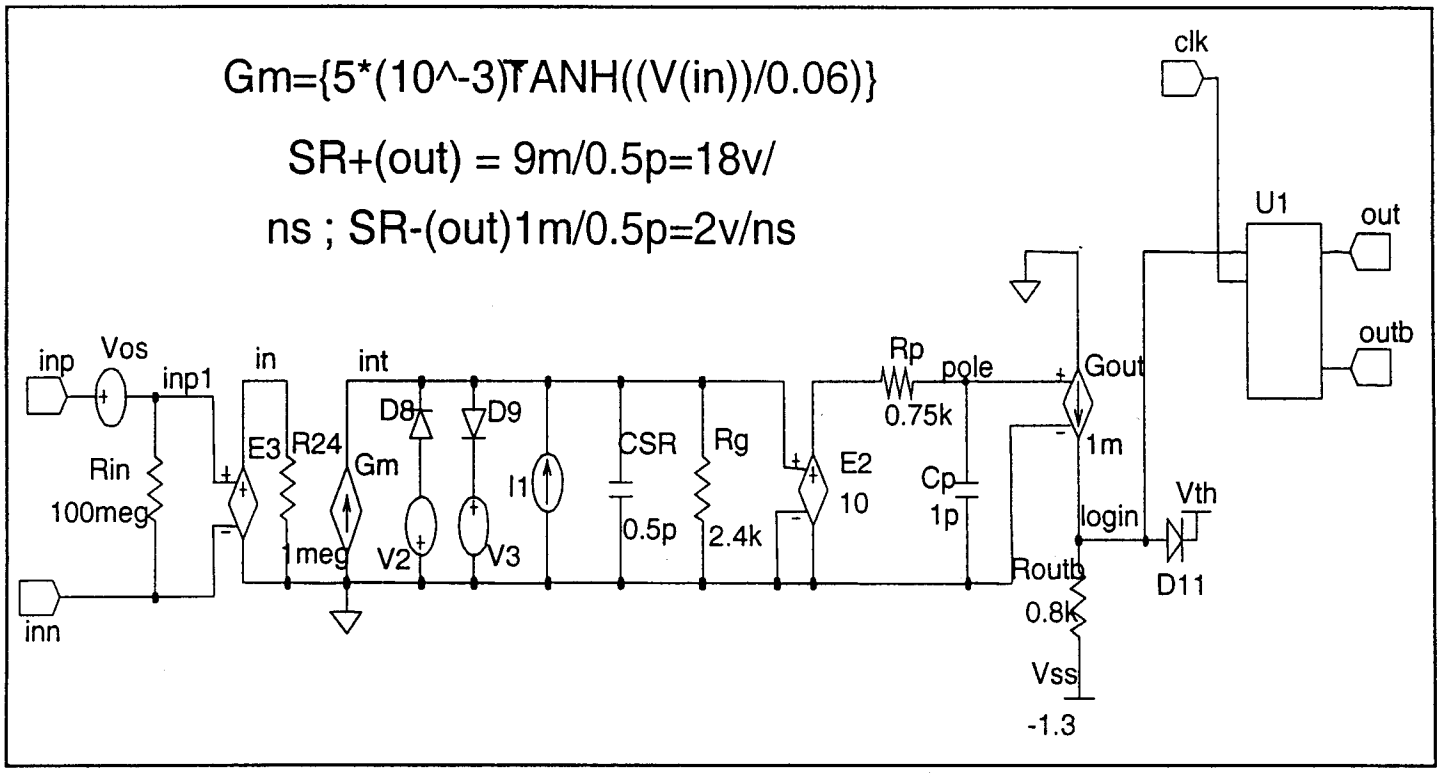

Figure 2-3. The suggested comparator - SPICE model

The reason for using this equation is twofold:

- this is a "well-behaved" equation in the sense of being smooth and having continuous derivatives
- Spice can use this functional description and portray the actual physical device behavior.

The model components are:

- The self-limiting function of a differential pair is obtained by

Appendix A

COMP8A_S

```
.SUBCKT comp8a_s  inp inn outb out
.model DV D
R11 inp inn 100k
R19 0 inp 100MEG
R20 inn 0 100MEG
G2 0 int value {5*(10^-3)*TANH((V(in))/0.06)}
E2 1 0 int 0 1
Rp 1 pole 0.75k
Cp pole 0 1p
CSR int 0 0.4p
D8 2 int DV
D9 int 3 DV
V2 3 0 0
V3 0 2 0
Rg int 0 24k
E3 in 0 inp inn 1
R24 in 0 1meg
D10 outb Vth D
D11 out Vth D
Gout outb out pole 0 1m
Routb out Vss 0.8k
Rout Vss outb 0.8k
* Power rail voltage sources
Vss Vss 0 -1.3
Vth Vth 0 0
.ENDS comp8a_s
```

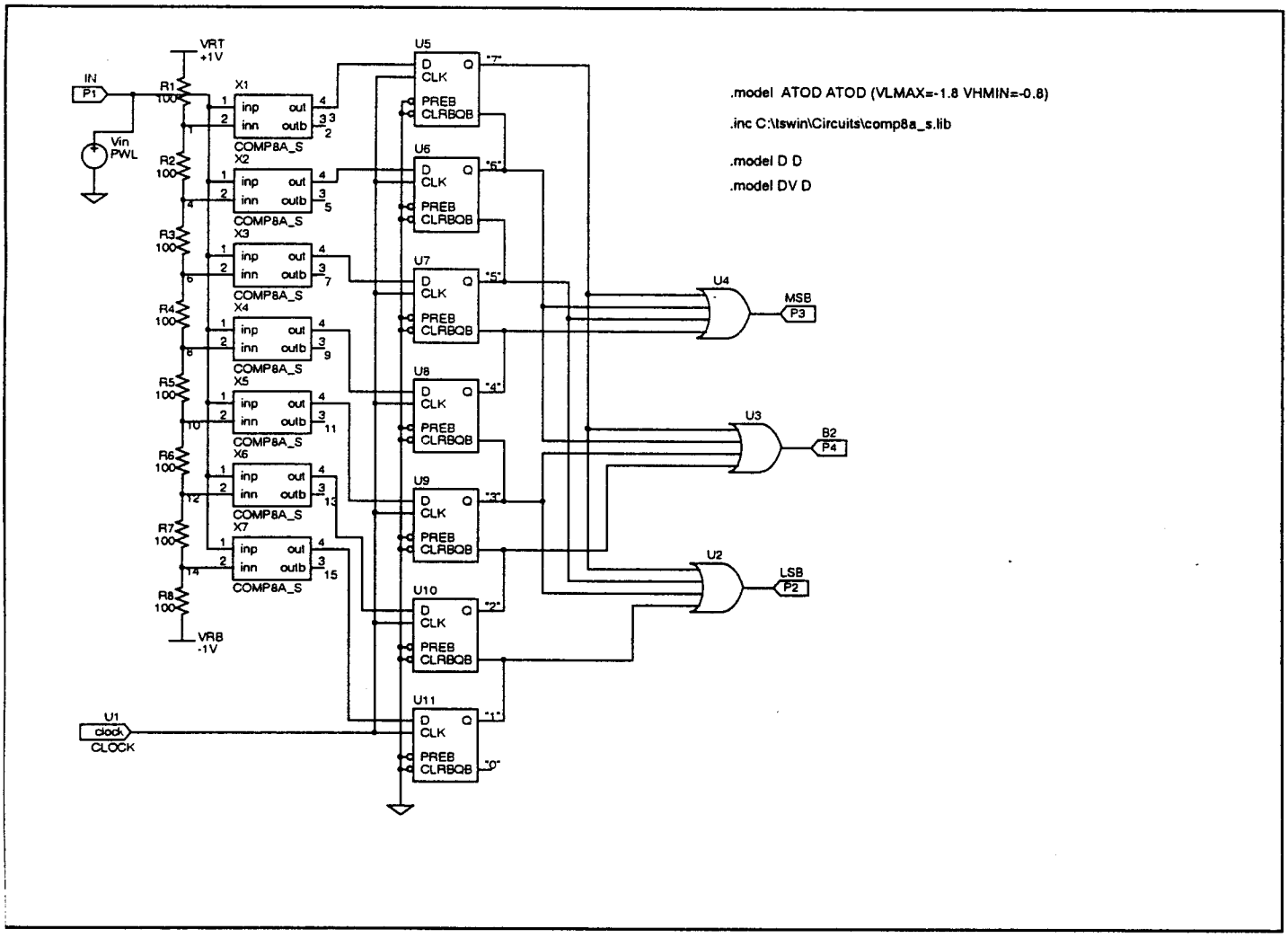

Figure 3-3. 3-bit flash converter

By employing a low resistance ladder, the comparator reference is not affected by either static input currents or dynamic perturbations of the input currents. Since the current gain β is reduced as the frequencies increase, the dynamic base currents increase creating a variable load that changes with frequency. This effect can be modeled by adding a capacitor across the comparator-input terminals. The comparator array used to analyze the converter' operation is similar to the device examined in chapter 2.

The differential input impedance of each comparator is 100 KΩ contributing to an error of one part in one thousand (0.1% = 100Ω / 100 kΩ) which is

```
R3 4 7 100
R4 7 10 100
R5 10 13 100
R6 13 16 100
R7 16 19 100
R8 19 VRB 100
U1 CLOCK 22 clock TPER=8n (0,-1.8) (4n ,-0.8)
U2 OR(4) LSB 23 24 25 26  TPCLKLH=1e-12,TPCLKHL=1e-12
U3 OR(4) B2 23 27 25 28  TPCLKLH=1e-12,TPCLKHL=1e-12
U4 OR(4) MSB 23 27 24 29  TPCLKLH=1e-12,TPCLKHL=1e-12
Vin IN 0 PWL
+ 0,-1
+ 1E-06,1
U5 DFF 23 27 $D_HI $D_HI 22 3  TPCLKLH=1e-12,TPCLKHL=1e-12 IS=0 ECLFF
U6 DFF 27 24 $D_HI $D_HI 22 6  TPCLKLH=1e-12,TPCLKHL=1e-12 IS=0 ECLFF
U7 DFF 24 29 $D_HI $D_HI 22 9  TPCLKLH=1e-12,TPCLKHL=1e-12 IS=0 ECLFF
U8 DFF 29 25 $D_HI $D_HI 22 12  TPCLKLH=1e-12,TPCLKHL=1e-12 IS=0 ECLFF
U9 DFF 25 28 $D_HI $D_HI 22 15  TPCLKLH=1e-12,TPCLKHL=1e-12 IS=0 ECLFF
U10 DFF 28 26 $D_HI $D_HI 22 18  TPCLKLH=1e-12,TPCLKHL=1e-12 IS=0 ECLFF
U11 DFF 26 30 $D_HI $D_HI 22 21  TPCLKLH=1e-12,TPCLKHL=1e-12 IS=0 ECLFF
* Power rail voltage sources
VRT VRT 0 +1V
VRB VRB 0 -1V
.INC 3BFLASH.CMD
```

16COMPS

```
.SUBCKT 16comps  RT RT_1 AIN clk RB "D" A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
A12 A13 A14 A15 "U"
*            1 2   3  4  5 6 7  8 9 10 11 12 13 14 15  16  17  18  19  20 21  22
* 16comps
.model  OR UGATE (TPLH=1p TPHL=1p)
.model  ATOD ATOD (VLMAX=-1.295 VHMIN=-1.305)
.inc C:\data\topspice\Circuits\c_lat1.lib
R8 1 2 5
R7 2 3 5
R6 3 4 5
R5 4 5 5
R1 RT RT_1 5
R2 RT_1 6 5
R3 6 7 5
R4 7 5 5
R16 8 9 5
R15 9 10 5
R14 10 11 5
R13 11 12 5
R9 1 13 5
```



```
R10 13 14 5
R11 14 15 5
R12 15 12 5
X1 AIN RT_1 clk "U" A15 C_LAT1
X2 AIN 6 clk A15 A14 C_LAT1
X3 AIN 7 clk A14 A13 C_LAT1
X4 AIN 5 clk A13 A12 C_LAT1
X5 AIN 4 clk A12 A11 C_LAT1
X6 AIN 3 clk A11 A10 C_LAT1
X7 AIN 2 clk A10 A9 C_LAT1
X8 AIN 1 clk A9 A8 C_LAT1
X9 AIN 13 clk A8 A7 C_LAT1
X10 AIN 14 clk A7 A6 C_LAT1
X11 AIN 15 clk A6 A5 C_LAT1
X12 AIN 12 clk A5 A4 C_LAT1
X13 AIN 11 clk A4 A3 C_LAT1
X14 AIN 10 clk A3 A2 C_LAT1
R17 RB 8 5
X15 AIN 9 clk A2 A1 C_LAT1
X16 AIN 8 clk A1 "D" C_LAT1
.ENDS 16comps
```

6BADA

```
6bada
.model  OR UGATE (TPLH=1p TPHL=1p)
.inc C:\data\converter\spice_models\flash\16comps.lib
.OPTIONS     ACCT ITL1=500   ITL2=200  ITL4=40     ITL5=0  LIMPTS=10000
.model  ATOD ATOD (VLMAX=-1.295 VHMIN=-1.305)
.model  DTOA  DTOA (TSW0=1p TSW1=1p TSWX=1p TSWZ=1p)
X3 RT RT 1 2 ref1 t48 t49 t50 t51 t52 t53 t54 t55 t56 t57 t58 t59 t60 t61 t62
+ t63 t64 16COMPS
X4 ref1 ref1 3 2 ref2 t32 t33 t34 t35 t36 t37 t38 t39 t40 t41 t42 t43 t44 t45
+ t46 t47 t48 16COMPS
X5 ref2 ref2 4 2 ref3 t16 t17 t18 t19 t20 t21 t22 t23 t24 t25 t26 t27 t28 t29
+ t30 t31 t32 16COMPS
X6 ref3 ref3 5 2 RB 6 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15 t16
+ 16COMPS
Vin 1 0 PWL
+ 0,0
+ 1.6E-07,1.6
U1 OR(32) lsb t63 t61 t59 t57 t55 t53 t51 t49 t47 t45 t43 t41 t39 t37 t35 t33
+ t31 t29 t27 t25 t23 t21 t19 t17 t15 t13 t11 t9 t7 t5 t3 t1
U2 OR(32) b5 t63 t62 t59 t58 t55 t54 t51 t50 t47 t46 t43 t42 t39 t38 t35 t34
+ t31 t30 t27 t26 t23 t22 t19 t18 t15 t14 t11 t10 t7 t6 t3 t2
U3 OR(32) b4 t63 t62 t61 t60 t55 t54 t53 t52 t47 t46 t45 t44 t39 t38 t37 t36
+ t31 t30 t29 t28 t23 t22 t21 t20 t15 t14 t13 t12 t7 t6 t5 t4
U4 OR(32) b3 t63 t62 t61 t60 t59 t58 t57 t56 t47 t46 t45 t44 t43 t42 t41 t40
```

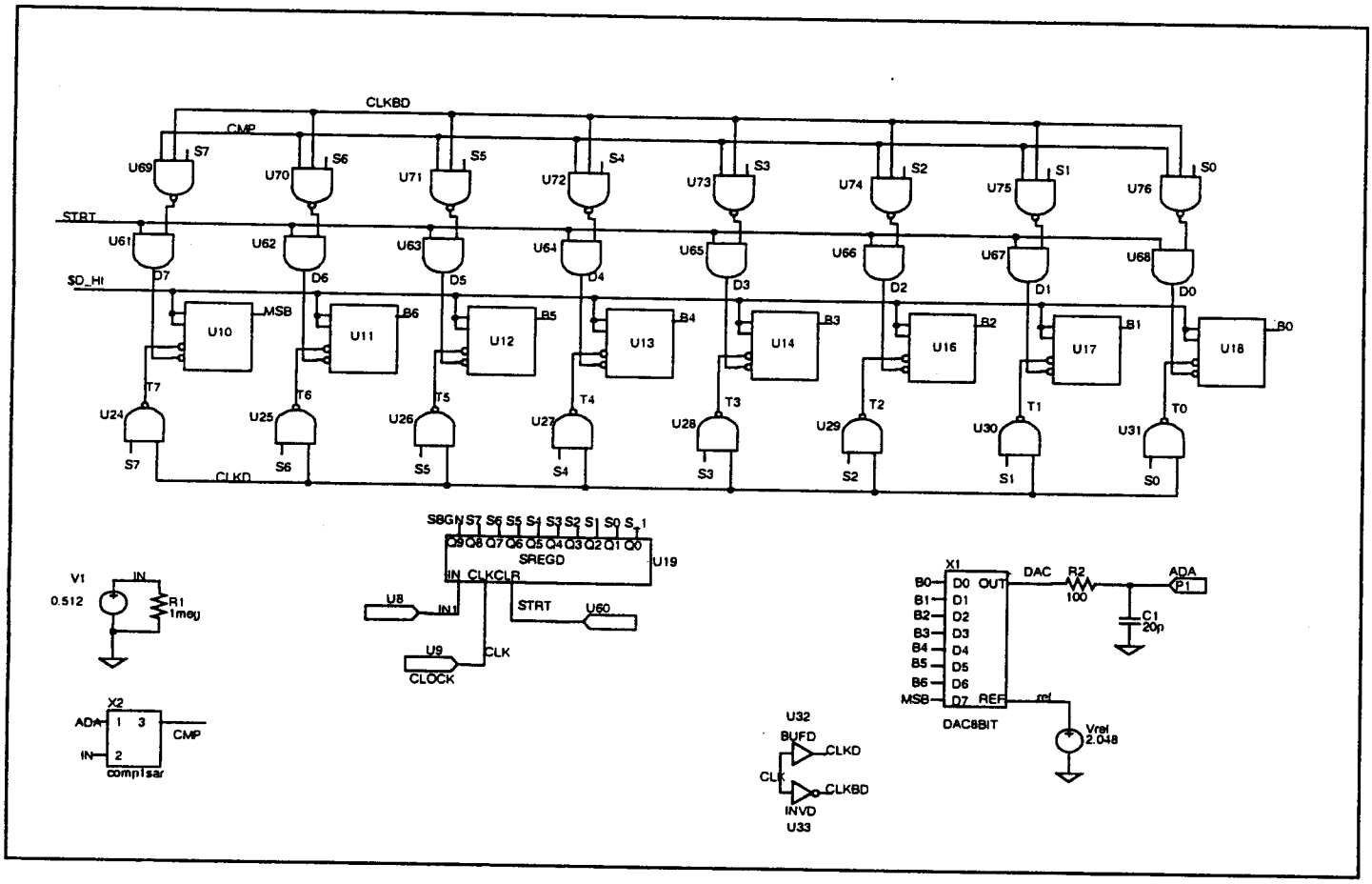

Figure 5-5. Testing the dynamic limitation of the SAR A/D loop

The devices in figure 5 – 5 are the following:

- X1 is the voltage D/A that can respond instantaneously
- R2 and C1 control the D/A voltage output time constant, making it a more realistic device. With the component values used the time constant of the D/A is τ_{DAC}= 2 nsec (=$R_2 \cdot C_1$=100Ω · 20 pF).
- X2 is the comparator modeled below in figure 5 – 6
- U19 is the serial register who's function is to propagate a pulse in a serial fashion from latch to latch such that each bit is tested sequentially as explained above
- The AND gates U24 through U31 allow the latches U10 through U18 to exercise the D/A bits in the sequence provided by U19
- U61 through U76 supply the logic to the latches U10 to U18 to keep or discard the state of each bit trial based on the comparator' decision

```
D9 0 int DV
D10 int 0 DV
R14 int 0 4.5k
E4 in 0 inp inn 1
R25 in 0 1meg
E5 anout 0 TABLE {V(pole)*10} -2,0V 2,4V
U20 BUF logout anout
.ENDS comp1sar
```

MACRO_SAR

```
.SUBCKT macro_sar  ADA IN CLK IN1
* 8 BIT ADC SAR a
.inc C:\data\converter\sar\comp1sar.lib
.MODEL SREGD USREG TPLH=2n TPHL=2n
.MODEL  NANDD UGATE (TPLH=2n TPHL=2n)
.MODEL  BUFD UGATE (TPLH=2n TPHL=2n)
.MODEL  INVD UGATE (TPLH=2n TPHL=2n)
U10 DFF MSB 1 T7 D7 $D_HI $D_HI  TPCLKLH=2n  TPCLKHL=2n
U11 DFF B6 2 T6 D6 $D_HI $D_HI  TPCLKLH=2n  TPCLKHL=2n
U12 DFF B5 3 T5 D5 $D_HI $D_HI  TPCLKLH=2n  TPCLKHL=2n
U13 DFF B4 4 T4 D4 $D_HI $D_HI  TPCLKLH=2n  TPCLKHL=2n
U14 DFF B3 5 T3 D3 $D_HI $D_HI  TPCLKLH=2n  TPCLKHL=2n
U16 DFF B2 6 T2 D2 $D_HI $D_HI  TPCLKLH=2n  TPCLKHL=2n
U17 DFF B1 7 T1 D1 $D_HI $D_HI  TPCLKLH=2n  TPCLKHL=2n
U18 DFF B0 8 T0 D0 $D_HI $D_HI  TPCLKLH=2n  TPCLKHL=2n
X1 B0 B1 B2 B3 B4 B5 B6 MSB ref DAC DAC8BIT
Vref ref 0 2.048
R1 IN 0 1meg
R2 DAC ADA 100
C1 ADA 0 20p
X2 ADA IN CMP comp1sar
U19 SREG(10) SBGN S7 S6 S5 S4 S3 S2 S1 S0 S_1 CLRCMD CLK 9 SREGD
U24 NAND T7 S7 CLKD
U25 NAND T6 S6 CLKD
U26 NAND T5 S5 CLKD
U27 NAND T4 S4 CLKD
U28 NAND T3 S3 CLKD
U29 NAND T2 S2 CLKD
U30 NAND T1 S1 CLKD
U31 NAND T0 S0 CLKD
U32 BUF CLKD CLK BUFD
U33 INV CLKBD CLK INVD
U61 AND D7 CLRCMD 10
U62 AND D6 CLRCMD 11
U63 AND D5 CLRCMD 12
U64 AND D4 CLRCMD 13
U65 AND D3 CLRCMD 14
```



```
U66 AND D2 CLRCMD 15
U67 AND D1 CLRCMD 16
U68 AND D0 CLRCMD 17
U69 NAND(3) 10 CMP CLKBD S7
U70 NAND(3) 11 CMP CLKBD S6
U71 NAND(3) 12 CMP CLKBD S5
U72 NAND(3) 13 CMP CLKBD S4
U73 NAND(3) 14 CMP CLKBD S3
U74 NAND(3) 15 CMP CLKBD S2
U75 NAND(3) 16 CMP CLKBD S1
U76 NAND(3) 17 CMP CLKBD S0
U77 NAND 18 S_1 CLKD
U78 DELAY CLRCMD 18
U79 AND 19 CLKBD IN1
U80 DELAY 9 19
.ENDS macro_sar
```

DAC8NL

```
.SUBCKT DAC8NL_LSB D0 D1 D2 D3 D4 D5 D6 D7 REF OUT   PARAMS:
TDELAY=1ns
* 8-bit DAC (digital-to-analog converter).
* The digital inputs D0 thru D7 MUST be logic signals - they must be
* connected to U digital device outputs.  If you want to apply analog voltages
* insert  U BUF elements between the signals and inputs.
V1 1 0 1V
O0 DTOA A0 0 1 D0 DACMODDA
R0 A0 0 1G
O1 DTOA A1 0 1 D1 DACMODDA
R1 A1 0 1G
O2 DTOA A2 0 1 D2 DACMODDA
R2 A2 0 1G
O3 DTOA A3 0 1 D3 DACMODDA
R3 A3 0 1G
O4 DTOA A4 0 1 D4 DACMODDA
R4 A4 0 1G
O5 DTOA A5 0 1 D5 DACMODDA
R5 A5 0 1G
O6 DTOA A6 0 1 D6 DACMODDA
R6 A6 0 1G
O7 DTOA A7 0 1 D7 DACMODDA
R7 A7 0 1G
E1 OUT 0 VALUE
+ {(V(A7)*12.8+V(A6)*6.4+V(A5)*3.2+V(A4)*1.6+V(A3)*.8+V(A2)*.4+V(A1)*.2+
+ V(A0)*0.2)/25.6*V(REF)}
ROUT OUT 0 1G
.MODEL DACMODDA DTOA (RLO0=200 RHI0=10MEG RLO1=10MEG RHI1=200
+  RLOX=10MEG RHIX=10MEG RLOZ=10MEG RHIZ=10MEG
```

```
.SUBCKT DAC8BIT D0 D1 D2 D3 D4 D5 D6 D7 REF OUT  PARAMS: TDELAY=1ns
* 8-bit DAC (digital-to-analog converter).
*
* The digital inputs D0 thru D7 MUST be logic signals - they must be
* connected to U digital device outputs.  If you want to apply analog
voltages
* insert . U BUF elements between the signals and inputs.
*
V1 1 0 1V
O0 DTOA A0 0 1 D0 DACMODDA
R0 A0 0 1G
O1 DTOA A1 0 1 D1 DACMODDA
R1 A1 0 1G
O2 DTOA A2 0 1 D2 DACMODDA
R2 A2 0 1G
O3 DTOA A3 0 1 D3 DACMODDA
R3 A3 0 1G
O4 DTOA A4 0 1 D4 DACMODDA
R4 A4 0 1G
O5 DTOA A5 0 1 D5 DACMODDA
R5 A5 0 1G
O6 DTOA A6 0 1 D6 DACMODDA
R6 A6 0 1G
O7 DTOA A7 0 1 D7 DACMODDA
R7 A7 0 1G

E1 OUT 0 VALUE
+ {(V(A7)*12.8+V(A6)*6.4+V(A5)*3.2+V(A4)*1.6+V(A3)*.8+V(A2)*.4+V(A1)*.2+
+ V(A0)*0.1)/25.5*V(REF)}
ROUT OUT 0 1G

.MODEL DACMODDA DTOA (RLO0=200 RHI0=10MEG RLO1=10MEG RHI1=200
+  RLOX=10MEG RHIX=10MEG RLOZ=10MEG RHIZ=10MEG
+  TSW0={TDELAY} TSW1={TDELAY} TSWX={TDELAY} TSWZ={TDELAY})
.ENDS DAC8BIT



.SUBCKT DAC8NL D0 D1 D2 D3 D4 D5 D6 D7 REF OUT  PARAMS: TDELAY=1ns
* 8-bit DAC (digital-to-analog converter) with nonlinearity modeling.
*
* Same Netlist as linear DAC8BIT above.   Same D0 to D7 logic signals

E1 SUM 0 TABLE {(V(A7)*12.8+V(A6)*6.4+V(A5)*3.2+V(A4)*1.6+V(A3)*.8+V(A2)
*.4+
+ V(A1)*.2+V(A0)*0.1)/25.5}
* Nonlinearity data table normalized to full range of 0 to 1V
+ (0,0.02) (0.2,0.2) (0.8,0.8) (1,0.98)

E2 OUT 0 POLY(2) SUM 0 REF 0  0 0 0 0 1
ROUT OUT 0 1G

.MODEL DACMODDA DTOA (RLO0=200 RHI0=10MEG RLO1=10MEG RHI1=200
+  RLOX=10MEG RHIX=10MEG RLOZ=10MEG RHIZ=10MEG
+  TSW0={TDELAY} TSW1={TDELAY} TSWX={TDELAY} TSWZ={TDELAY})
.ENDS DAC8NL
```

converter by allowing the coarse A/D to start a new conversion as soon as THA#2 sampled the residue voltage. While the coarse converter output "goes through the pipe" the fine converter completes its previous conversion.

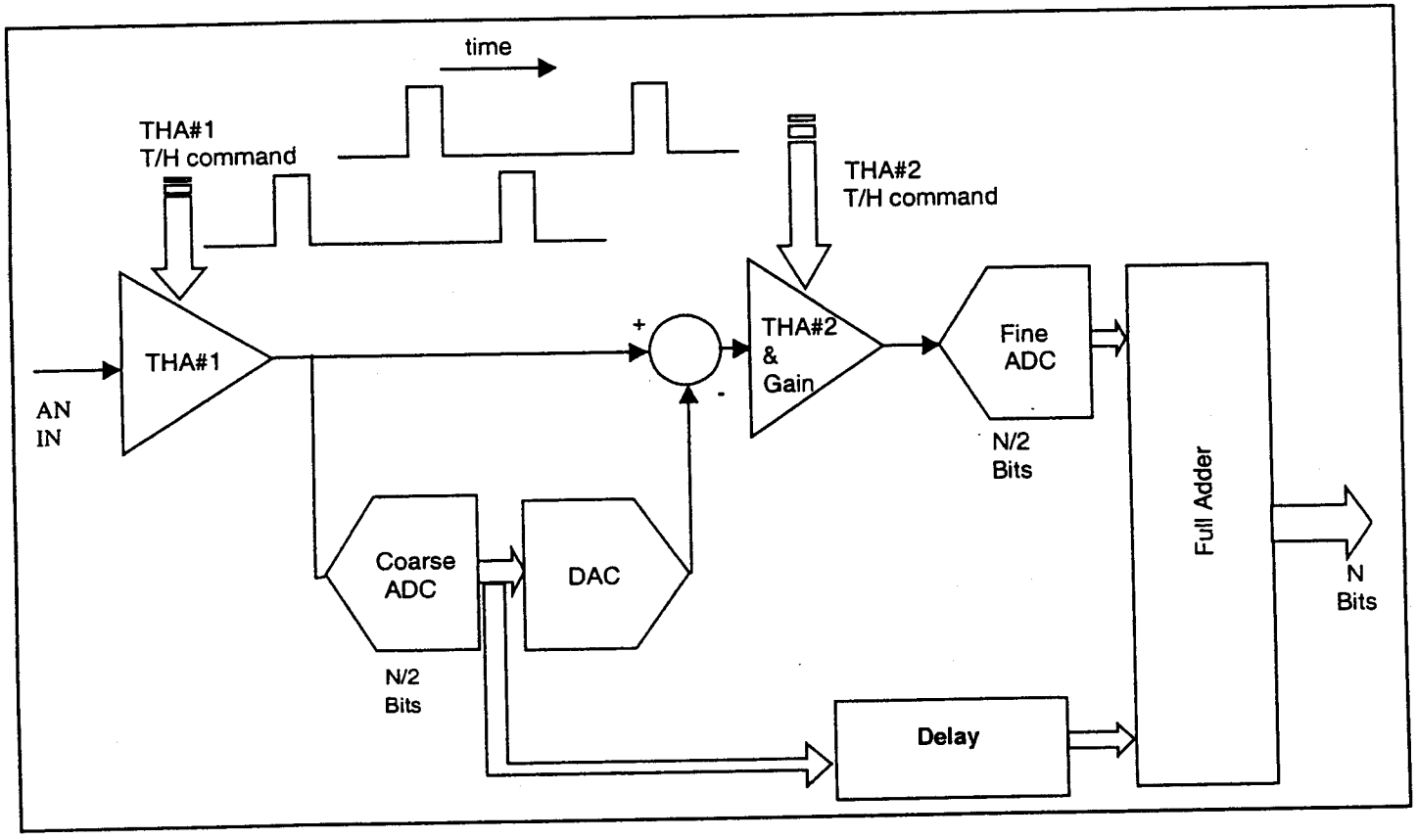

Figure 7-1. Pipeline A/D converter - general topology

THA#1 in figure 7 – 1 samples the analog input, followed by a coarse A/D converter. The coarse converter obtains the first N/2 bits and its output is converted back into an analog (quantized) signal using a D/A. The D/A required for the operation has only N/2 bits of resolution but N bits accuracy. The quantized signal is then subtracted from the THA#1 output and passed along to THA#2. After THA#2 completes its acquisition, THA#1 begins to acquire a new input signal, and the residue is converted simultaneously by the fine A/D, completing the conversion process with the next N/2 bits. The digital code from the coarse converter is delayed by the delay unit for a period equivalent to the time required for the residue signal to be processed by the difference amplifier, THA#2 and the fine A/D. After the time alignment the coarse and fine digital codes are combined in the

```
Rbw res_gain an_in_fine 100
Cbw an_in_fine 0 2.5pF
X11 s0 s1 s2 s3 s4 s5 s6 s7 ada_top ADA_OUT DAC8BIT PARAMS: TDELAY=1p
S1 SHOUT1 IN TH1 0 SW
S2 SHOUT2 3 TH2 0 SW
C1 SHOUT1 0 5p
C2 SHOUT2 0 5p
U15 CLOCK TH1  TPER=10n (0,0)  (1n,1) (4n,0)
U18 ADD(8) q7 q6 q5 q4 q3 q2 q1 q0 co DD3 DD2 DD1 DD0 $D_LO $D_LO $D_LO
$D_LO
+ $D_LO $D_LO $D_LO DDF4 DDF3 DDF2 DDF1 DDF0 $D_LO ADD
X12 fine_ref_t an_in_fine FN fine_ref_b DF0 DF1 DF2 DF3 DF4 5B_FLASH
Vos_top rtop fine_ref_t 640m
Vos_bot rbot fine_ref_b 640m
U20 OR s7 q7 co
U21 OR s6 q6 co
U22 OR s5 q5 co
U23 OR s4 q4 co
U24 OR s3 q3 co
U25 OR s2 q2 co
U26 OR s1 q1 co
U27 OR s0 q0 co
RDAC 2 C_DAC 300
CDAC C_DAC 0 1.5pF.
Edac 3 0 SHOUT1 C_DAC 1
U29 PSREG(9) DDF4 DDF3 DDF2 DDF1 DDF0 DD3 DD2 DD1 DD0 $D_HI $D_HI
$D_HI 4
+ $D_LO $D_LO DF4 DF3 DF2 DF1 DF0 5 6 7 8 PSREG
U31 PSREG 5 6 7 8 $D_HI $D_HI $D_HI 9 $D_LO $D_LO D3 D2 D1 D0 PSREG
U40 CLOCK CRS  TPER=10n (0,0)  (4n,1) (4.5n,0)
U41 CLOCK TH2  TPER=10n (0,0)  (4.5n,1) (9n,0)
U42 CLOCK 9  TPER=10n (0,0)  (4.5n,1) (5n,0)
U43 CLOCK FN  TPER=10n (0,0)  (9n,1) (9.5n,0)
U44 CLOCK 4  TPER=10n (0,0)  (9.5n,1) (10n,0)
Vos 1 rtop 0
* Power rail voltage sources
Vada_top ada_top 0 2.56
.END
```

4B_FLASH

```
.SUBCKT 4B_flash  Ref_top Ref_bot AN_IN clk  MSB B2 B3 LSB
.model  OR UGATE (TPLH=1p TPHL=1p)
.inc C:\data\converter\pipeline\16comps2.lib
.options acct lvltim=1 numdgt=6 chgtol=1e-16
.model  ATOD ATOD (VLMAX=-1.295 VHMIN=-1.305)
.model  DTOA  DTOA (TSW0=1p TSW1=1p TSWX=1p TSWZ=1p)
X4 Ref_top Ref_top AN_IN clk Ref_bot 1 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12
```



```
+ t13 t14 t15 t16 16COMPS2
U9 OR(8) 2 t15 t14 t13 t12 t11 t10 t9 t8
U10 OR(8) 3 t15 t14 t13 t12 t7 t6 t5 t4
U11 OR(8) 4 t15 t14 t11 t10 t7 t6 t3 t2
U12 OR(8) 5 t15 t13 t11 t9 t7 t5 t3 t1
U14 OR MSB t16 2
U15 OR B2 t16 3
U16 OR B3 t16 4
U17 OR LSB t16 5
.ENDS 4B_flash
```

5B_FLASH

```
.SUBCKT 5B_FLASH  ref_top AN_IN clk refb lsb b4 b3 b2 msb
* 5bada
.model  OR UGATE (TPLH=1p TPHL=1p)
.inc C:\data\converter\pipeline\16comps2.lib
.options acct lvltim=1 numdgt=6 chgtol=1e-16
.model  ATOD ATOD (VLMAX=-1.295 VHMIN=-1.305)
.model  DTOA  DTOA (TSW0=1p TSW1=1p TSWX=1p TSWZ=1p)
X5 ref_top ref_top AN_IN clk ref3 t16 t17 t18 t19 t20 t21 t22 t23 t24 t25 t26
+ t27 t28 t29 t30 t31 t32 16COMPS2
X6 ref3 ref3 AN_IN clk refb 1 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14
+ t15 t16 16COMPS2
U15 OR(17) b3 t32 t31 t30 t29 t28 t23 t22 t21 t20 t15 t14 t13 t12 t7 t6 t5 t4
+ OR
U16 OR(17) b2 t32 t31 t30 t29 t28 t27 t26 t25 t24 t15 t14 t13 t12 t11 t10 t9
+ t8 OR
U17 OR(17) msb t32 t31 t30 t29 t28 t27 t26 t25 t24 t23 t22 t21 t20 t19 t18 t17
+ t16 OR
U18 OR(17) lsb t32 t31 t29 t27 t25 t23 t21 t19 t17 t15 t13 t11 t9 t7 t5 t3 t1
+ OR
U19 OR(17) b4 t32 t31 t30 t27 t26 t23 t22 t19 t18 t15 t14 t11 t10 t7 t6 t3 t2
+ OR
.ENDS 5B_FLASH
```

CHAPTER 8

1P5B8

```
.MODEL SW VSWITCH (VON=2 VOFF=1.995 RON=100 ROFF=1000G)
.OPTION OPTS NUMDGT=7 FILOUT METHOD=GEAR  LVLTIM=1 PIVREL=1e-6
.include  c:\data\converter\spice_models\1p5\sub_mdac.lib
.model dff1 ueff (tpclkhl=1p tpclklh=1p)
```

```
.model inv2 ugate (tphl=1p tplh=1p)
.model add1 ualu (tphl=1p tplh=1p)
.model and1 ugate (tphl=1p tplh=1p)
Vp refp cm 0.25
Vn cm refn 0.25
VPOS cm VNEG 1
VNEG VPOS cm 1
Vcm cm 0 2.5
U2 CLOCK ph1 CLOCK TPER=10n (0,0) (0.5n ,1) (5n,0)
U3 CLOCK ph2 CLOCK TPER=10n (0,0) (5.5n ,1) (10n,0)
U7 CLOCK ph1a CLOCK TPER=10n (0,0) (0.5n ,1) (4n,0)
U11 CLOCK ph2a CLOCK TPER=10n (0,0) (5.5n ,1) (9n,0)
X1 1 2 cm refp refn VNEG VPOS b0 b1 ph1a ph1 ph2 out outb SUB_MDAC
Vinp 1 0 PWL
+ 0,1.988
+ 4E-06,3.012
Vinn 2 0 PWL
+ 0,3.012
+ 4E-06,1.988 .
X2 outb out cm refp refn VNEG VPOS b2 b3 ph2a ph2 ph1 out2 out2b SUB_MDAC
X3 out2b out2 cm refp refn VNEG VPOS b4 b5 ph1a ph1 ph2 out3 out3b SUB_MDAC
X4 out3b out3 cm refp refn VNEG VPOS b6 b7 ph2a ph2 ph1 out4 out4b SUB_MDAC
X5 out4b out4 cm refp refn VNEG VPOS b8 b9 ph1a ph1 ph2 out5 out5b SUB_MDAC
U12 DFF 3 4 $D_HI $D_HI clk1 b1 dff1
U13 DFF 5 6 $D_HI $D_HI clk1 b0 dff1
U14 DFF 7 8 $D_HI $D_HI clk2 3 dff1
U15 DFF 9 10 $D_HI $D_HI clk2 5 dff1
U16 DFF 11 12 $D_HI $D_HI clk1 7 dff1
U17 DFF 13 14 $D_HI $D_HI clk1 9 dff1
U18 DFF 15 16 $D_HI $D_HI clk2 11 dff1
U19 DFF 17 18 $D_HI $D_HI clk2 13 dff1
U20 DFF 19 20 $D_HI $D_HI clk2 b3 dff1
U21 DFF 21 22 $D_HI $D_HI clk2 b2 dff1
U22 DFF 23 24 $D_HI $D_HI clk1 19 dff1
U23 DFF 25 26 $D_HI $D_HI clk1 21 dff1
U24 DFF 27 28 $D_HI $D_HI clk2 23 dff1
U25 DFF 29 30 $D_HI $D_HI clk2 25 dff1
U26 DFF 31 32 $D_HI $D_HI clk1 b5 dff1
U27 DFF 33 34 $D_HI $D_HI clk1 b4 dff1
U28 DFF 35 36 $D_HI $D_HI clk2 31 dff1
U29 DFF 37 38 $D_HI $D_HI clk2 33 dff1
U30 DFF 39 40 $D_HI $D_HI clk2 b7 dff1
U31 DFF 41 42 $D_HI $D_HI clk2 b6 dff1
U39 DFF 43 44 $D_HI $D_HI clk1 15 dff1
U40 DFF 45 46 $D_HI $D_HI clk1 17 dff1
U41 DFF 47 48 $D_HI $D_HI clk1 27 dff1
U42 DFF 49 50 $D_HI $D_HI clk1 29 dff1
U43 DFF 51 52 $D_HI $D_HI clk1 35 dff1
U44 DFF 53 54 $D_HI $D_HI clk1 37 dff1
U45 DFF 55 56 $D_HI $D_HI clk1 39 dff1
```



```
U46 DFF 57 58 $D_HI $D_HI clk1 41 dff1
U47 DFF 59 60 $D_HI $D_HI clk1 b9 dff1
U48 DFF 61 62 $D_HI $D_HI clk1 b8 dff1
U49 ADD(1) BT5 63 i h 64 add1
U50 ADD(1) BT4 65 g f 63 add1
U51 ADD(1) BT3 66 e d 65 add1
U52 ADD(1) BT2 67 c b 66 add1
U53 ADD(1) MSB 68 $D_LO a 67 add1
E10 69 70 out7b cm 1e4
V5 70 0 1.6
U54 DFF 71 72 $D_HI $D_HI clk1 69 dff1
U55 DFF lsb 73 $D_HI $D_HI clk2 74 dff1
U56 ADD(1) BT6 64 k j 75 add1
U57 AND 74 ph1 71 and1
U58 CLOCK clk1  TPER=10n (0,1) (3n ,0) (8n,1)
U59 INV clk2 clk1 inv2
X6 out5b out5 cm refp refn VNEG VPOS b10 b11 ph2a ph2 ph1 out6 out6b SUB_MDAC
X7 out6b out6 cm refp refn VNEG VPOS b12 b13 ph1a ph1 ph2 out7 out7b SUB_MDAC
U60 DFF 76 77 $D_HI $D_HI clk2 43 dff1
U61 DFF 78 79 $D_HI $D_HI clk2 45 dff1
U62 DFF 80 81 $D_HI $D_HI clk2 47 dff1
U63 DFF 82 83 $D_HI $D_HI clk2 49 dff1
U64 DFF 84 85 $D_HI $D_HI clk2 51 dff1
U65 DFF 86 87 $D_HI $D_HI clk2 53 dff1
U66 DFF 88 89 $D_HI $D_HI clk2 55 dff1
U67 DFF 90 91 $D_HI $D_HI clk2 57 dff1
U68 DFF 92 93 $D_HI $D_HI clk2 59 dff1
U69 DFF 94 95 $D_HI $D_HI clk2 61 dff1
U70 DFF a 96 $D_HI $D_HI clk1 76 dff1
U71 DFF b 97 $D_HI $D_HI clk1 78 dff1
U72 DFF c 98 $D_HI $D_HI clk1 80 dff1
U73 DFF d 99 $D_HI $D_HI clk1 82 dff1
U74 DFF e 100 $D_HI $D_HI clk1 84 dff1
U75 DFF f 101 $D_HI $D_HI clk1 86 dff1
U76 DFF g 102 $D_HI $D_HI clk1 88 dff1
U77 DFF h 103 $D_HI $D_HI clk1 90 dff1
U78 DFF i 104 $D_HI $D_HI clk1 92 dff1
U79 DFF j 105 $D_HI $D_HI clk1 94 dff1
U80 DFF 106 107 $D_HI $D_HI clk2 b11 dff1
U81 DFF 108 109 $D_HI $D_HI clk2 b10 dff1
U82 DFF k 110 $D_HI $D_HI clk1 106 dff1
U83 DFF l 111 $D_HI $D_HI clk1 108 dff1
U84 DFF m 112 $D_HI $D_HI clk1 b13 dff1
U85 DFF n 113 $D_HI $D_HI clk1 b12 dff1
U86 ADD(1) BT7 75 m l 114 add1
U87 ADD(1) BT8 114 lsb n $D_LO add1
.END
```

SUBMDAC

```
.SUBCKT sub_mdac  inp inn cm refp refn VNEG VPOS bi bi+1 ph1a ph1 ph2 out outb
.model inv1 ugate (tphl=1p tplh=1p)
.model and1 ugate (tphl=1p tplh=1p)
.model dff1 ueff (tpclkhl=1p tpclklh=1p)
U18 AND(3) bi a bb ph2 and1
U19 AND x ab ph2 and1
U20 AND bi+1 b ph2 and1
S2 inp 1 ph1 0 SW
S3 inn 2 ph1 0 SW
S4 VNEG 1 x 0 SW
S5 VPOS 1 bi+1 0 SW
S6 VPOS 2 x 0 SW
S7 VNEG 2 bi+1 0 SW
S8 outb 3 ph2 0 SW
S9 out 4 ph2 0 SW
S10 5 cm ph1a 0 SW
S11 6 cm ph1a 0 SW
C1 1 6 1p
C2 2 5 1p
E2 7 cm 8 cm -0.5
C3 6 3 1p
C4 5 4 1p
S12 3 inp ph1 0 SW
S13 4 inn ph1 0 SW
E3 9 cm cm 8 -0.5
R1 10 8 10k
C5 8 cm 1p
E7 10 cm 6 5 2e3
S14 5 6 ph1a 0 SW
S15 2 1 bi 0 SW
E9 11 12 inp refn 50
V4 Vth 0 1.6
E10 13 14 inp refp 50
E12 14 Vth refn inn 50
E13 12 Vth refp inn 50
R2 7 outb 500
R3 9 out 500
U27 INV 15 ph1a inv1
U28 DFF a ab $D_HI $D_HI 15 11 dff1
U29 DFF b bb $D_HI $D_HI 15 13 dff1
.ENDS sub_mdac
```


APPENDIX B

SPICE OPTIONS

In his book Inside SPICE – overcoming the obstacles of circuit simulations, the author Ron Kielkowski states:

> ...One of the most important commands in the SPICE input file is the .OPTIONS statement....

> ...Understanding the .OPTIONS statement parameters is crucial to producing fast, accurate, convergent SPICE simulations.

The book also suggests a set of options values that the author found to be reliable for most circuits, including the converters of this book. The suggested options are: