Development Strategies for Durable Hardware Language Descriptions of Analog & Mixed Signal Circuits.

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Abstract

VHDL-AMS, or VHSIC Hardware Description Language - Analog & Mixed Signal Extensions is being supported in a variety of Design Automation tools for circuit design. Although there are a number of published examples on the use of VHDL-AMS for modeling of mixed signal circuits, it is still not clear what are examples of "best practice" methods. This paper discusses research efforts to identify analog macros, or descriptions that can be re-used by other designers that are possibly targeting different fabrication processes.

1: Introduction

VHDL-AMS, or VHSIC Hardware Description Language - Analog & Mixed Signal Extensions, has recently been accepted as IEEE Standard 1076.1[1]. As an IEEE Standard, it is being supported in a variety of Design Automation tools for circuit design. Although there are a number of published examples on the use of VHDL-AMS for modeling of mixed signal circuits, it is still not clear what are examples of "best practice" methods. This paper discusses research efforts to identify analog macros, or descriptions that can be re-used by other designers. Compared to digital macros, analog macros need to meet a more difficult set of criteria in order for the description to be of use in a design library. We outline some of the analog criteria below.

2: Analog Requirements

First, analog macros typically are high performance macros. By high performance, we are referring to a high achievement in several categories and reasonable achievement in others. Considering the following category list:

Table 1 Analog Performance Categories

Power Supply Rejection Ratio (dB)	Common Mode Rejection Ratio (dB)	Output Range vs. Supply Voltage (V)
Unity Gain Frequency (GHz)	Phase Margin (degrees)	Input Common Mode Range (V)
Slew Rate (V/μs)	Power Dissipation (mW)	Layout Area (μm^2)
Voltage Gain (dB)	Offset Voltage (mV)	Settling Time (μs)
C_{load} (pF)	Flicker Noise	Broadband Noise

If High, Medium, and Low achievements are used for each category, the number of design descriptions can lead to **14 Million different amplifier types** (3^{15}). Such a large variation in the number of different kinds of amplifiers points to the fact that accurate and substantive modeling is needed. Such models are found in design kits and libraries that characterize a fabrication process. These libraries must be established before VHDL-AMS descriptions are sufficiently rich in detail. Since the interaction among the categories is dependent on the fabrication processes, i.e. it is not the same across vendors, different design kits will encompass the differences in operation of the same device design among different vendors.

3: The Challenge

In order to develop criteria for reusable analog macros, mixed signal design test cases need to be exercised. An initial requirement is determining the typical form of a mixed signal design case. We differentiate two broad classes: (1) A chip with approximately equal portions of

analog and digital cells, (2) A largely digital chip with a small fraction of analog cells. In this paper, we focus on the first case. Designs with a combination of analog and digital components are often of interest to analog designers. One reason for this interest is that this class of circuits includes very important devices for analog design, most notably, A/D and D/A converters. While these circuits may contain many thousands of digital gates, they are most often developed by analog designers, because of their power and performance constraints. With today's demand for higher performance, integrated appliances, chip designers are pressed to fit more functionality into a smaller package. In fact, many integrated circuits now on the market have several data converters on the same die. For example, chips for wireless circuits will need a pair of data converters at bandpass frequencies as well as a pair of data converters at baseband frequencies. Since the fabrication process models are critical for data converter design, these 4 data converters are often placed on the same die. In an increasing number of design situations, these data converters are of the oversampled type. For illustrative purposes, we have chosen to look at the Sigma-Delta Modulator.

In order to evaluate a particular data converter architecture efficiently, we have determined, through a number of design cycles that we gain the most insight into a converter's characteristics by first adapting a strategy of high level behavioral modeling. To this end, we evaluated several tools, which allowed us to investigate the behavioral functionality of some basic data converter models.

4: Our approach

The three applications we focused on, most recently, were Matlab from MathWorks Inc., hAMSter from SIMEC GmbH & Co. KG, and SMASH from DOLPHIN Integration. We have chosen these commercial tools taking into account cost as well as sustainability. In addition, commercial simulation tools are often positioned to be integrated with other commercial tools in the mixed signal design process, and hence tend to build a user community that communicates best practices among its users. In this paper, we again narrow our focus to the evaluation of hAMSter and SMASH. Our work with Matlab is detailed in another paper, for this conference, as mentioned later.

SMASH and hAMSter are both VHDL-AMS simulators. In addition, SMASH has the added capability to integrate a number of hardware descriptions methods into a single modeling environment. This includes the ability to incorporate Spice netlists with VHDL-AMS and the "C" programming language. VHDL-AMS is a particularly powerful tool for modeling the behavior of devices at higher levels. VHDL code is the most common method for capturing the description of digital hardware and behavior. Not until the addition of the Analog and Mixed Signal extensions, were we able to describe the nature of continuous time signals in the same model with their digital counterparts. As we will demonstrate below, we now have the capacity to characterize the analog behavior of a data converter with just a few line of code. While these examples are somewhat trivial in their sophistication, they do provide a hint of what is now possible with this new generation of tools.

5: Some Examples

For our first example of behavioral modeling of an oversampled D/A, we consider a VHDL-AMS description of a Sigma-Delta modulator, which is supplied with the High Performance AMS Tool for Engineering and Research (hAMSter).

```
--sigma delta converter
ENTITY sigdel2 IS
        GENERIC (vref : REAL := 10.0;
                 tau1 : REAL := 64.0E-6;
                 tau2 : REAL := 8.0E-6);
        PORT (clk : IN BIT;
              TERMINAL input : ELECTRICAL;
              TERMINAL output : ELECTRICAL);
BEGIN END ENTITY sigdel2;

ARCHITECTURE sd OF sigdel2 IS
  QUANTITY input_v ACROSS input;
  QUANTITY output_v ACROSS output_i THROUGH
output;
  QUANTITY sum1, sum2 : REAL;
  QUANTITY isum1 : REAL := 0.0;
  QUANTITY isum2 : REAL := 0.0;
  SIGNAL vref_help : REAL := vref;
BEGIN
  SDW : ENTITY sigdelDIG(behav)
          GENERIC MAP (vref=>vref)
          PORT MAP (clk, isum2, vref_help);
      sum1  == input_v - output_v;
      isum1 == 1.0/ tau1* sum1'INTEG;
      sum2  == isum1 - output_v;
      isum2 == 1.0/ tau2* sum2'INTEG;
      output_v == vref_help;
END ARCHITECTURE sd;
```

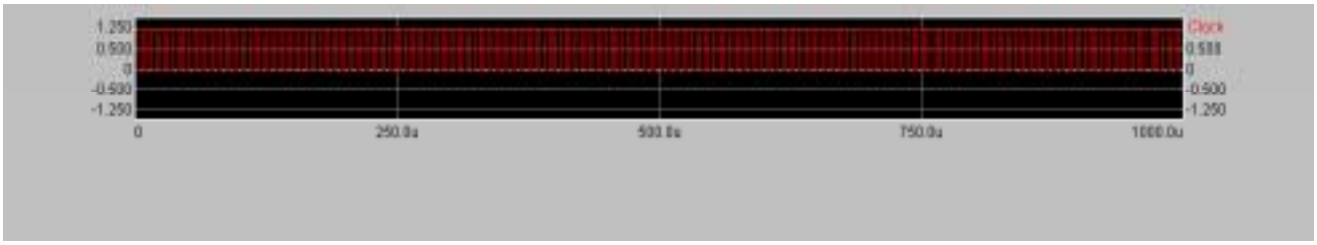

Figure 1 Digital Converter Clock

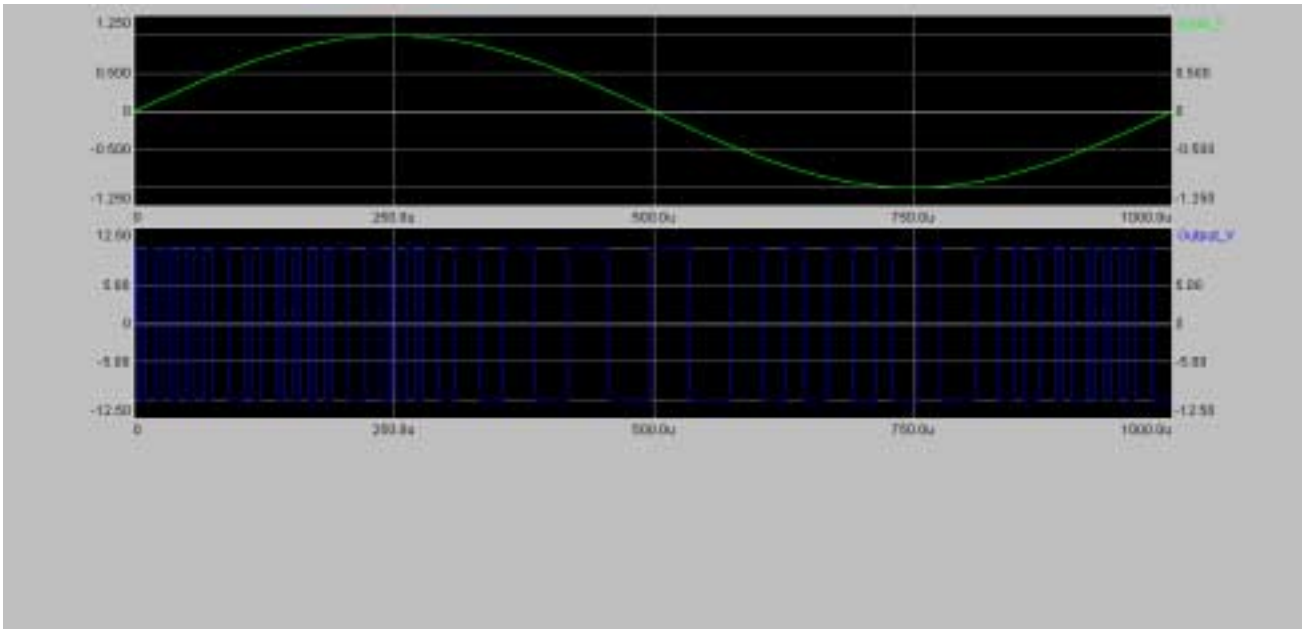

Figure 2 Input Signal and Output Response

The results from this behavioral model simulation show the digital converter clock Fig.1, the Input sinusoidal signal and the Output response Fig. 2.

The main advantage to utilizing such an abstract model is that we can use this model as a test platform for investigating various configurations of modulators and decimation filters. Additionally, we are afforded the opportunity to add more detail to the model as understanding of the various parameters is gained.

With the flexibility, provided by the AMS extensions to VHDL, models can be viewed as simple algebraic and differential equations [2] for initial investigation and then later augmented with SPICE parameters to provide a model that better represents the actual implementations in silicon.

Hamster offers the ability quickly evaluate designs with both behavioral abstractions as well as structural VHDL descriptions. As mentioned previously, SMASH can model designs with various languages and at various levels of abstraction. It offers the use of C for modeling DSP algorithms, VHDL for digital designs. Spice for parameterized analog modeling and VHDL-AMS for incorporation of all the above. SMASH also provides an interface for the Cadence Development Suite to allow for netlists to be generated from schematics and then modeled along with VHDL/AMS components. This along with SMASH's ability to do quick FFT and Bandwidth measurements makes it the primary tool we intend to investigate further. For completeness, we also include the output of SMASH Fig.3, when given the same VHDL-AMS code as listed above.

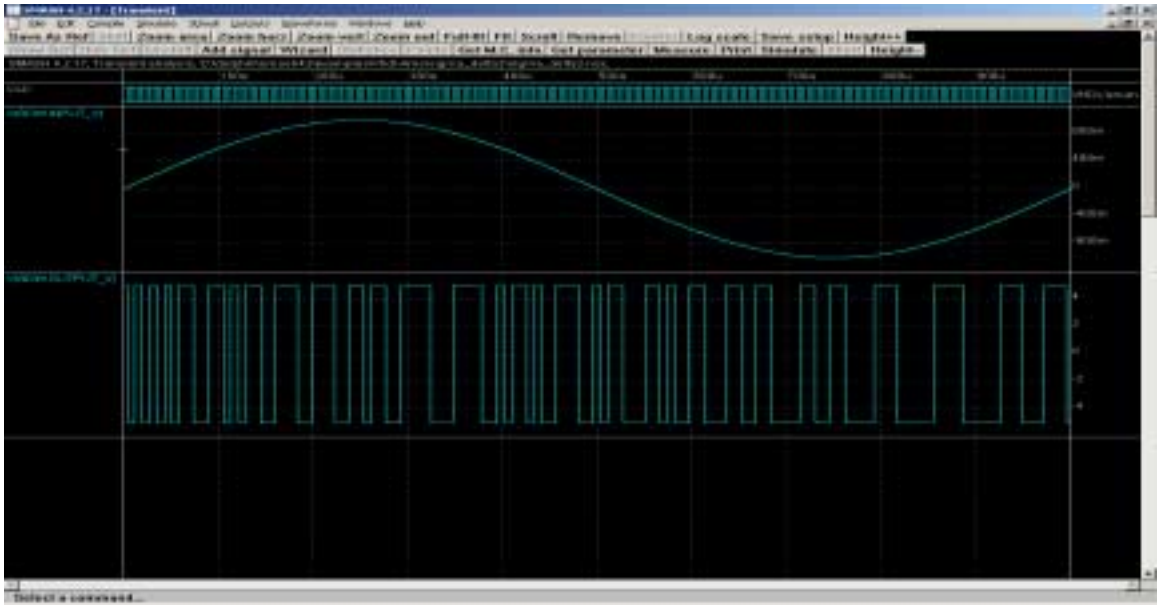

Figure 3 SMASH Output

SMASH, Hamster, and similar tools enable an environment for evaluating the difference between various architectures for oversampled data converter architectures. For example, a second order sigma delta modulators employs 2 integrator op amp cell blocks,[3] where the op amps are distinctly different from each other. The op amps are different primarily because the saturation behavior is different for the first stage compared to the second stage. As shown in the earlier part of the paper on op amp parameters, the space of possible behaviors needs to consider millions of different types of amplifiers. Thus, there are millions of possible behaviors for sigma delta modulators. We will present the change in behavior of the modulator structure as a function of the selected parameters in a VHDL-AMS environment. The parameter space has been initially explored using MATLAB simulations, as described in the paper at this conference by J. Wu & S. Bibyk on "An Efficient Behavioral Model for Delta-Sigma Modulators." Once the parameters space is fleshed out in MATLAB, it can be reproduced in a VHDL environment and thus more accurately capture the significant effects of different digital decimator architectures on the pulse density stream emerging from the modulator.

6: Conclusion

High level analog behavioral modeling of mixed signal architectures such as data converters enables the exploration of a rich design space in which the output behavior can take millions of different forms depending on the value of circuit and layout parameters. We have demonstrated modeling and simulation methods using two recently released mixed signal modelers and simulators - Hamster and SMASH. The results indicate that behavioral modeling of mixed signal systems are effective and that the main task is to produce useful models that are accurate and differentiate system behavior when the same system is fabricated from different vendors.

7: Acknowledgements

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8: References

[1] “IEEE Standard VHDL Analog and Mixed-Signal Extensions”, *IEEE Std 1076.1-1999.*
[2] E. Christen, K. Bakalar, A. Dewey, and E. Moser. “Analog and Mixed-Signal Modeling Using the VHDL-AMS Language”, 36th Design Automation Conference, Jun. 1999.
[3] S. Norsworthy, R. Schreier, and G. Temes. *Delta-Sigma Data Converters.* IEEE Press, Piscataway, NJ 08855, 1997.