

(c) If terminal Z is connected to ground, X to a signal source  $v_i$  with a source resistance  $R_s = 2 \text{ k}\Omega$ , and Y to an  $8\text{-k}\Omega$  load resistance, use the hybrid- $\pi$  model of Fig. 4.33(a), to draw the small-signal equivalent circuit of the amplifier. (Note that the current source  $I$  should be replaced with an open circuit.) Calculate the voltage gain  $v_o/v_i$ . If  $I_o$  is neglected what is the error in estimating the gain magnitude? Note: An infinite capacitance is used to indicate that the capacitance is sufficiently large that it acts as a short circuit at all signal frequencies of interest. However, the capacitor still blocks dc.

**Ans.** (a)  $-0.1 \text{ V}$ ,  $-0.8 \text{ V}$ ,  $+2 \text{ V}$ ; (b)  $40 \text{ mA/V}$ ,  $2.5 \text{ k}\Omega$ ,  $100 \text{ k}\Omega$ ; (c)  $-77 \text{ V/V}$ ,  $+3.9\%$

### 4.9 GRAPHICAL ANALYSIS

Although formal graphical methods are of little practical value in the analysis and design of most transistor circuits, it is illustrative to portray graphically the operation of a simple transistor amplifier circuit. Consider the circuit of Fig. 4.34, which we have already analyzed in Example 4.9. A graphical analysis of the operation of this circuit can be performed as follows: First, we have to determine the dc bias point. Toward that end we set  $v_i = 0$  and use the technique illustrated in Fig. 4.35 to determine the dc base current  $I_B$  (we have already employed this technique in the analysis of diode circuits in Chapter 3). We next move to the  $i_C$ - $v_{CE}$  characteristics, shown in Fig. 4.36. Observe that each of these characteristic curves is obtained by setting the base current  $i_B$  to a constant value, varying  $v_{CE}$ , and measuring the corresponding  $i_C$ . This family of  $i_C$ - $v_{CE}$  characteristic curves should be contrasted to that shown in Fig. 4.15; the latter was obtained by setting  $v_{BE}$  constant.

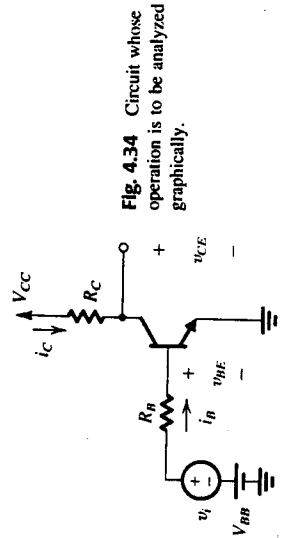
Having determined the base bias current  $I_B$ , we know that the operating point will lie on the  $i_C$ - $v_{CE}$  curve corresponding to this value of base current (the curve for  $i_B = I_B$ ). Where it lies on the curve will be determined by the collector circuit. Specifically, the collector circuit imposes the constraint

$$v_{CE} = V_{CC} - i_C R_C$$

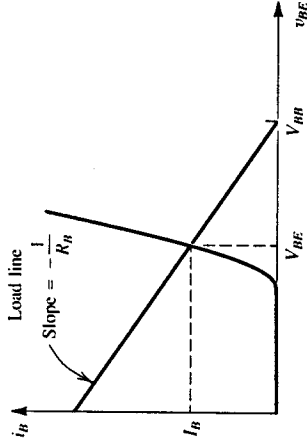
which can be rewritten as

$$i_C = \frac{V_{CC}}{R_C} - \frac{1}{R_C} v_{CE}$$

which represents a linear relationship between  $v_{CE}$  and  $i_C$ . This relationship can be represented by a straight line, as shown in Fig. 4.36. Since  $R_C$  can be considered the am-



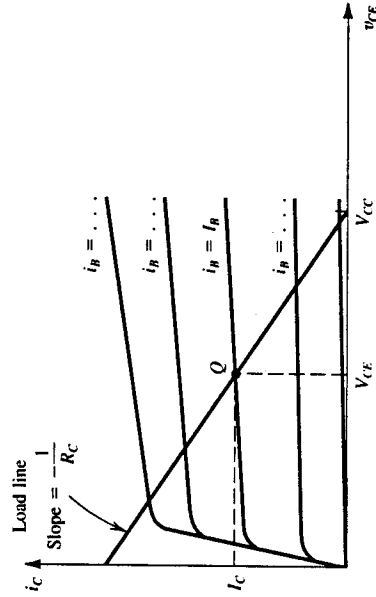
**Fig. 4.34** Circuit whose operation is to be analyzed graphically.



**Fig. 4.35** Graphical construction for the determination of the dc base current in the circuit of Fig. 4.34.

plifier load, the straight line of slope  $-1/R_C$  is known as the load line.<sup>5</sup> The dc bias point, or quiescent point,  $Q$  will be at the intersection of the load line and the  $i_C$ - $v_{CE}$  curve corresponding to the base current  $I_B$ . The coordinates of point  $Q$  give the dc collector current  $I_C$  and the dc collector-emitter voltage  $V_{CE}$ . Observe that for amplifier operation,  $Q$  should be in the active region and furthermore should be located so as to allow for a reasonable signal swing as the input signal  $v_i$  is applied. This will become clearer shortly.

The situation when  $v_i$  is applied is illustrated in Fig. 4.37. Consider first Fig. 4.37(a), which shows a signal  $v_i$  having a triangular waveform being superimposed on the dc voltage  $V_{BE}$ . Corresponding to each instantaneous value of  $V_{BE} + v_i(t)$ , one can draw a straight line with slope  $-1/R_B$ . Such an "instantaneous load line" intersects the  $i_B$ - $v_{BE}$  curve at a point whose coordinates give the total instantaneous values of  $i_B$  and  $v_{BE}$  corresponding to the



**Fig. 4.36** Graphical construction for determining the dc collector current  $I_C$  and the collector-emitter voltage  $V_{CE}$  in the circuit of Fig. 4.34.

<sup>5</sup> The term *load line* is also employed for the straight line in Fig. 4.35.

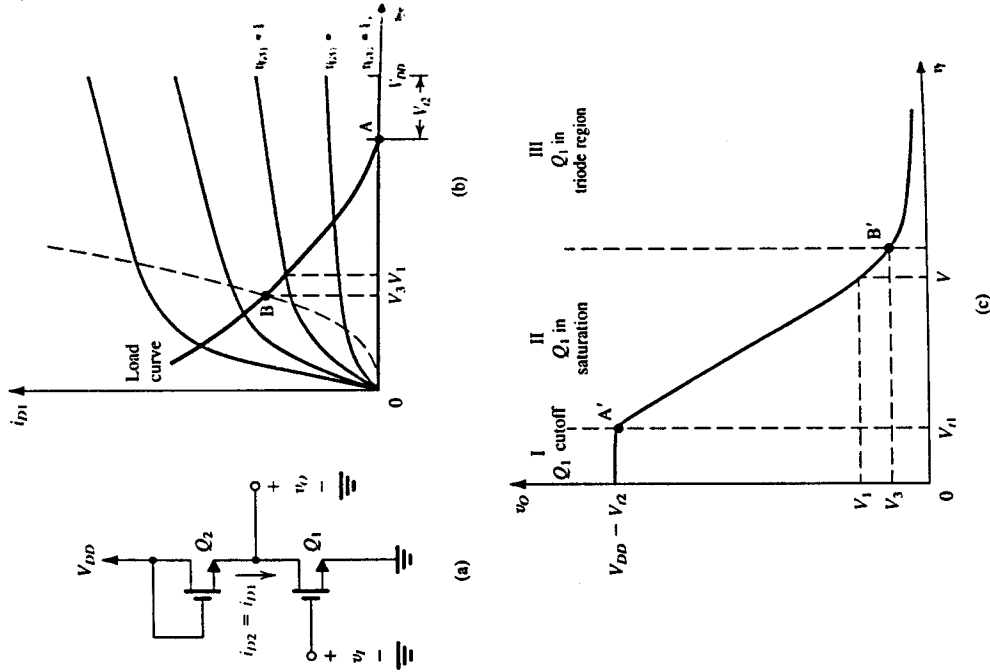


Fig. 5.52 (a) NMOS amplifier with enhancement load; (b) graphical determination of the transfer characteristic; (c) transfer characteristic.

neglected, the gain expression is modified to

$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \frac{1}{1 + X_2}$$

Thus the body effect reduces the gain magnitude by 20%.

Finally, we note that in addition to its low and fixed (i.e., independent of bias current) gain, the enhancement-load amplifier has another drawback: Its signal swing is rather limited, since  $v_o$  cannot rise above  $(V_{DD} - V_1)$ .

**Example**  
 For the enhancement-load amplifier, let  $W_1 = 100 \mu\text{m}$ ,  $L_1 = 6 \mu\text{m}$ ,  $W_2 = 6 \mu\text{m}$ , and  $L_2 = 30 \mu\text{m}$ . If the effective parameter  $X = 0.2$ , find the voltage gain without and with the body effect taken into account.  
 Ans. 41.2 V/V; -7.61 V/V

**NMOS Amplifier with Depletion Load.** Using a depletion load results in an amplifier with performance superior to that of the enhancement-load circuit. The depletion-load amplifier is shown in Fig. 5.53(a). Neglecting, for the moment, the body effect in the load transistor  $Q_2$ , we can use the graphical construction illustrated in Fig. 5.53(b) to obtain the amplifier transfer characteristic sketched in Fig. 5.53(c). As shown, the characteristic is steep, indicating a high voltage gain in region III, which is obtained when both  $Q_1$  and  $Q_2$  are operating in saturation.

For operation in region III of the transfer characteristic, the small-signal equivalent circuit in Fig. 5.54 applies. Here we have included the controlled source  $g_{mb2}v_{b2}$  that models the body effect in  $Q_2$ . Apart from this, the only other parameter representing  $Q_2$  is its output resistance  $r_{o2}$ . Analysis of the circuit in Fig. 5.54 is straightforward and can be shown to yield the following gain expression:

$$A_v \equiv \frac{v_o}{v_i} = -g_{m1} \left[ \frac{1}{g_{mb1}} \parallel r_{o1} \parallel r_{o2} \right] \quad (5.83)$$

Unfortunately, it is usually the case that  $\frac{1}{g_{mb2}}$  is much smaller than  $r_{o1}$  and  $r_{o2}$ , resulting in the gain being approximately given by

$$A_v \approx -\frac{g_{m1}}{g_{mb2}} = -\frac{g_{m1}}{X g_{m2}}$$

Thus,

$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \frac{1}{X} \quad (5.84)$$

Comparison of Eq. (5.84) with the gain expression for the enhancement-load amplifier (Eq. 5.82) reveals that the gain of the depletion-load amplifier is a factor of  $\left(\frac{1+X}{X}\right)$  greater.

Since  $X$  is typically 0.1 to 0.3, the gain increases by a factor of 3 to 10. This is, nevertheless, still quite a bit lower than the expected gain of the CMOS amplifier.

The Feedback-Type Converter

Figure 10.35 shows a simple A/D converter that employs a comparator, an up-down counter, and a D/A converter. The comparator circuit provides an output that assumes one of two distinct values: positive when the difference input signal is positive, and negative when the difference input signal is negative. We shall study comparator circuits in Chapter 12. An up-down counter is simply a counter that can count either up or down depending on the binary level applied at its up-down control terminal. Because the A/D converter of Fig. 10.35 employs a DAC in its feedback loop it is usually called a feedback-type A/D converter. It operates as follows: With a 0 count in the counter, the D/A converter output,  $v_o$ , will be zero and the output of the comparator will be high, instructing the counter to count the clock pulses in the up direction. As the count increases, the output of the DAC rises. The process continues until the DAC output reaches the value of the analog input signal, at which point the comparator switches and stops the counter. The counter output will then be the digital equivalent of the input analog voltage.

Operation of the converter of Fig. 10.35 is slow if it starts from zero. This converter however, tracks incremental changes in the input signal quite rapidly.

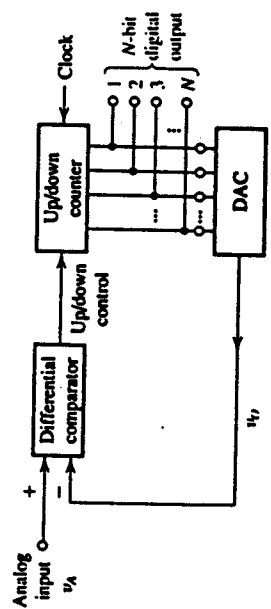


Fig. 10.35 A simple feedback-type A/D converter.

The Dual-Slope A/D Converter

A very popular high-resolution (12- to 14-bit) (but slow) A/D conversion scheme is illustrated in Fig. 10.36. To see how it operates, refer to Fig. 10.36 and assume that the analog input signal  $v_A$  is negative. Prior to the start of the conversion cycle, switch  $S_2$  is closed, thus discharging capacitor  $C$  and setting  $v_i = 0$ . The conversion cycle begins with opening  $S_2$  and connecting the integrator input through switch  $S_1$  to the analog input signal. Since  $v_A$  is negative, a current  $I = v_A/R$  will flow through  $R$  in the direction away from the integrator. Thus  $v_i$  rises linearly with a slope of  $I/C = v_A/RC$ , as indicated in Fig. 10.36(b). Simultaneously, the counter is enabled and it counts the pulses from a fixed-frequency clock. This phase of the conversion process continues for a fixed duration  $T_1$ . It ends when the counter accumulates a fixed count denoted  $n_{ref}$ . Usually, for  $N$ -bit converter,  $n_{ref} = 2^N$ . Denoting the peak voltage at the output of the integrator  $V_{ref}$ , we

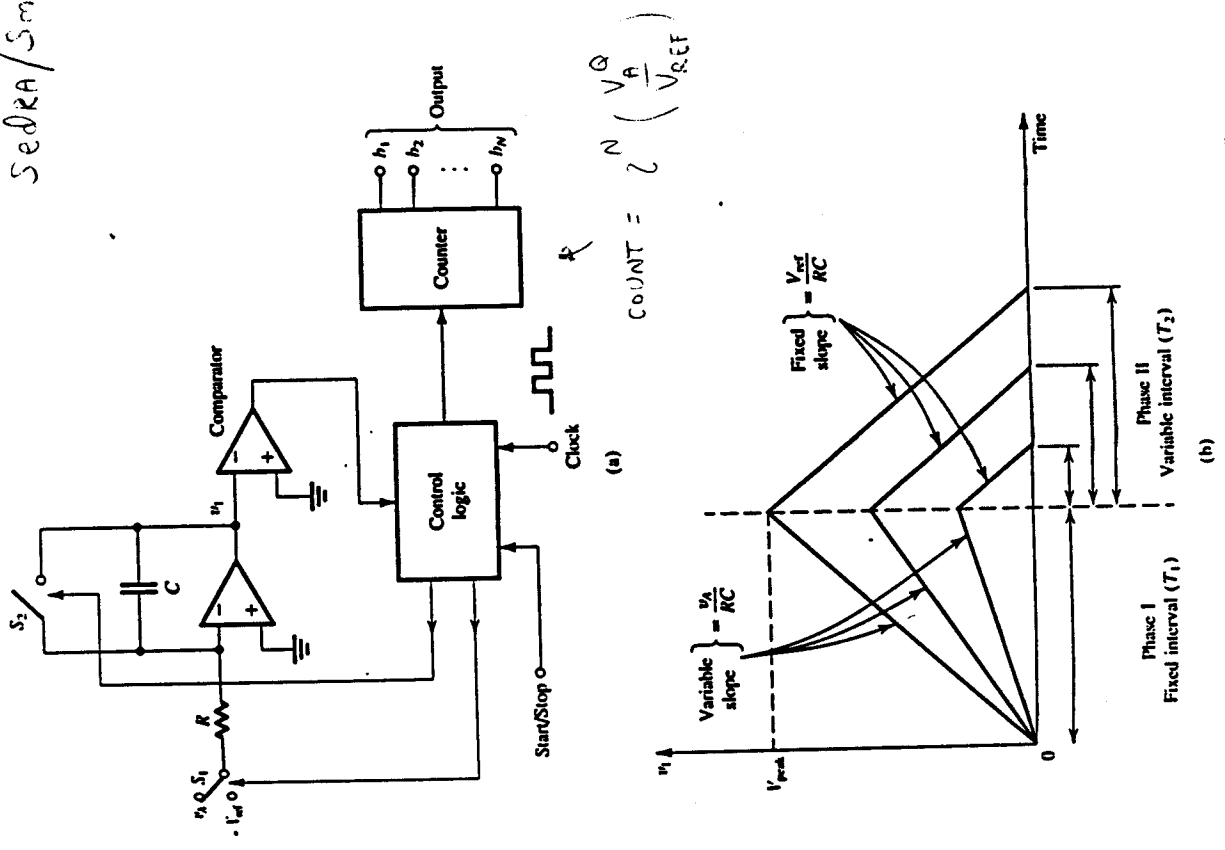


Fig. 10.36 The dual-slope A/D conversion method. Note that  $v_A$  is assumed to be negative.