Characterization of Two Standard CMOS EEPROM Designs

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Abstract

The objective of this project is to characterize the programming speed and the programming voltage requirements of floating gate EEPROM cells made in a generic CMOS process (e.g. a MOSIS tiny chip – AMI C5N 0.5 micron technology). The charge trapping and injection is based on carrier injection using cold tunneling (Fowler-Nordheim effect). The variable constraints are the sizes of the injector capacitors and control gate capacitors. All necessary positive voltages will be generated using a charge pump requiring a single power supply.

1. Introduction

This paper describes the design and implementation of CMOS EEPROM with several variable design constraints. Currently, EEPROM cells can be implemented in CMOS, but this information is not well documented. One objective was to demonstrate the feasibility of making CMOS EEPROM cells in the university environment. Another objective of this project was to characterize how different variable constraints could affect the operating parameters of the EEPROM cells. The two designs implemented are based on a floating gate transistor and use carrier injection based on cold tunneling (Fowler-Nordheim effect) [1].

The design constraints include varying the size of the injector capacitor and control gate capacitors thus minimizing the supply voltage requirements as well as reducing the power consumption of the system. This project utilizes various well-known designs that have been tested by other groups [2] – [5]. The primary design uses a single injector and floating gate, while the second design implements a newer dual injector floating gate device technology. This device attempts to reduce the programming voltage from a high voltage to a more manageable voltage comparable to that of standard supply voltages. These designs were tested by varying the injector capacitors and the control gate capacitors in an attempt to minimize the supply voltage and minimize the programming time required to set and clear the individual bits of the EEPROM cells.

2. Theory

The basis for the operation of an EEPROM cell is the use of a floating gate transistor. A floating gate is a conductor entirely surrounded by an insulator. This floating gate then serves as the gate of the PMOS transistor. In order to write data into the floating gate transistor we must inject carriers onto this gate. This carrier injection can be accomplished in the following two ways: hot electron injection and cold tunneling. This device makes use of the cold tunneling injection method. Cold tunneling makes use of the Fowler-Nordheim effect. This is a quantum mechanical effect that permits electrons to cross a thin insulating layer without a breakdown of the dielectric [1].

3. Design description

3.1 Floating gate cells

This project implements two different floating gate designs. The first design uses a single injector capacitor and a single floating gate capacitor. The injector capacitor is significantly smaller than the floating gate capacitor. This characteristic allows electrons to tunnel through the injector capacitor oxide. This allows the electrons to be stored on the floating gate capacitor. The capacitors are connected using a polysilicon line that is also connected to the gate of a standard PMOS transistor of a PMOS/NMOS pair. To set the bit, the injector capacitor must have a high voltage applied to induce tunneling through the gate oxide while the floating gate capacitor is grounded. To clear the bit, the

 0-7803-7150-X/01/$10.00@2001 IEEE

voltage supply polarity is reversed, thus drawing the electrons off of the floating gate capacitor [2].

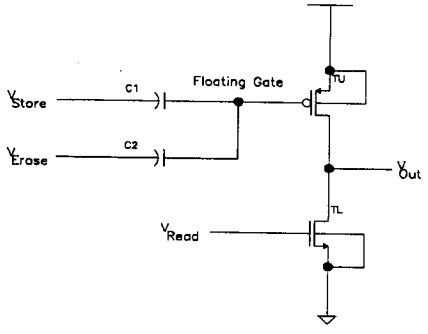
The first design consists of a single injection capacitor, a single control capacitor, and two transistors. A PMOS transistor is used as the composite transistor and an NMOS transistor is used for the reading transistor. The ratio of the injector and control gate capacitors was varied to determine the most effective design. The ratios used are 1:25, 1:36, 1:49, 1:81, and 1:100.

The schematic and the layout of the single injector gate design are shown in Figure 1. To write to the EEPROM cell, a positive voltage is applied to the control capacitor (V_{Store}), while the injector (V_{Erase}) is connected to the ground. The tunnel effect then takes place where the electrons are accumulated on the floating gate. The potential of the floating gate is then decreased as a result. On the contrary, when the positive voltage is applied to V_{Erase}, and V_{Store} is connected to the ground, the erasure is achieved. The tunnel effect occurs in the opposite direction, removing electrons from the floating gate, which increases its potential [2].

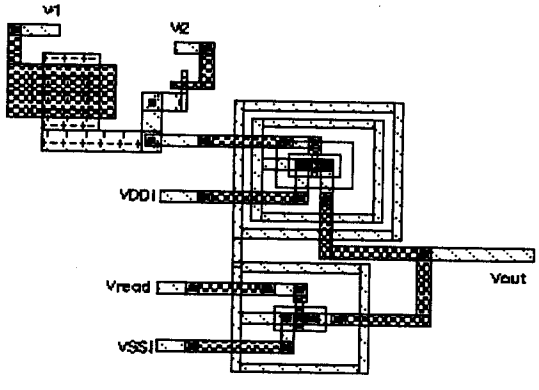
The reading of the EEPROM cell (V_{out}) is done by connecting V_{Store} and V_{Erase} to the ground, so that the accumulated electrons in the floating gate are not disturbed, and applying a positive voltage (V_{read}) to the NMOS transistor to turn it on [2].

The second design, shown in Figure 2, implements two injector capacitors and a single floating gate capacitor in an attempt to lower the programming voltage. To achieve this, the second injector capacitor is connected to the floating gate and is biased with a polarity opposite that of the first injector capacitor. This design allows the injector capacitor's polarity to remain constant. The other advantage of this design is that it allows the supply voltage to be centered on zero volts, rather than the single higher voltage required of the single injector capacitor design. This allows for the use of supply voltages that are typically available for standard CMOS devices [3], [6].

To read the state of the bit, a PMOS/NMOS pair is implemented as mentioned for the single floating gate capacitor. The stored value can then be read on the V_{mem} output line.

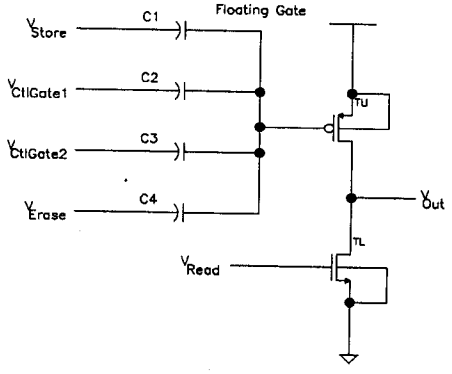


A. Schematic

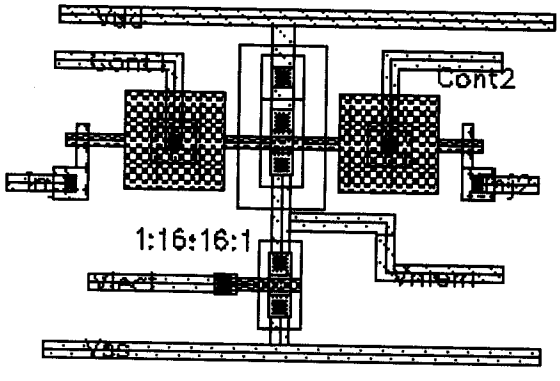


B. Layout

Figure 1. Single injector gate memory cell



A. Schematic



B. Layout

Figure 2. Double injector gate memory cell

3.2 Charge pumps

The charge pump requires a high voltage to be applied to the floating gates during the write cycle. The Dickson charge pump design was investigated to allow the EEPROM chip to run from a single power supply.

A Dickson charge pump, shown in Figure 3, is composed of a chain of diodes and capacitors arranged in such a way that charge is transferred to the output capacitor [6]. The two capacitors and diodes are switched by two clocks that run 180° out of phase. The first capacitor is charged to the level of the input voltage. This charge is then stored on the second capacitor and eventually on the output capacitor. These single cells are cascaded to increase the final output voltage. The final capacitor can be either switched or directly coupled to a load.

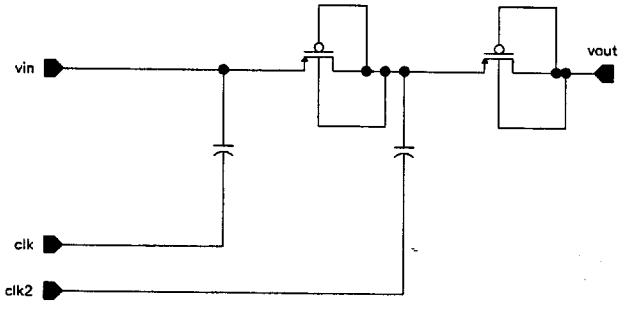


Figure 3. Dickson charge pump schematic

4. Project objectives

By varying the capacitor ratios, the amount of charge required to set or clear the floating gate will be affected. This project will implement several different ratios of the injector capacitors and the floating gate capacitors in an attempt to optimize the performance of the device. These ratios will also be implemented in the two injector capacitor design. Comparison between these two designs will be made to determine the advantages and disadvantages of each. Characterization of the performance of these different designs will lead to a better understanding of how these factors can be modified to enhance performance.

References

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