design iterations before an optimized gate-level representation that met all design constraints was obtained. Thus, the *designer's mind* was used as the logic synthesis too illustrated in Figure 14-1.

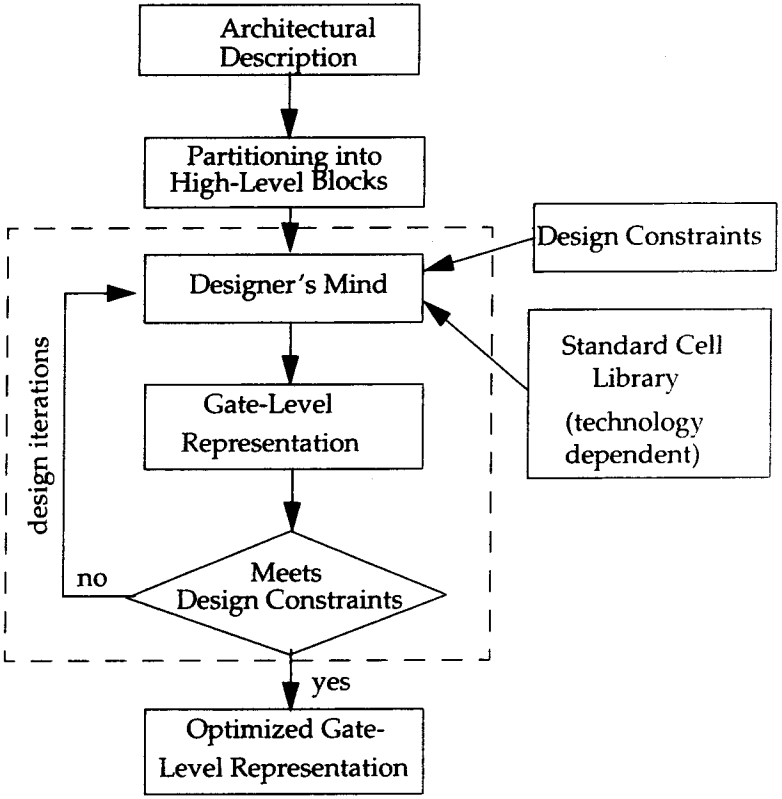

Figure 14-1 Designer's Mind as the Logic Synthesis Tool

The advent of *computer-aided logic synthesis tools* has automated the process of converti the high-level description to logic gates. Instead of trying to perform logic synthesis their minds, designers can now concentrate on the architectural trade-offs, high-level description of the design, accurate design constraints, and optimization of cells in the standard cell library. These are fed to the computer-aided logic synthesis tool, which performs several iterations internally and generates the optimized gate-level descripti Also, instead of drawing the high-level description on a screen or a piece of paper,

designers describe the high-level design in terms of HDLs. Verilog HDL has become one of the popular HDLs for the writing of high-level descriptions. Figure 14-2 illustrates the process.

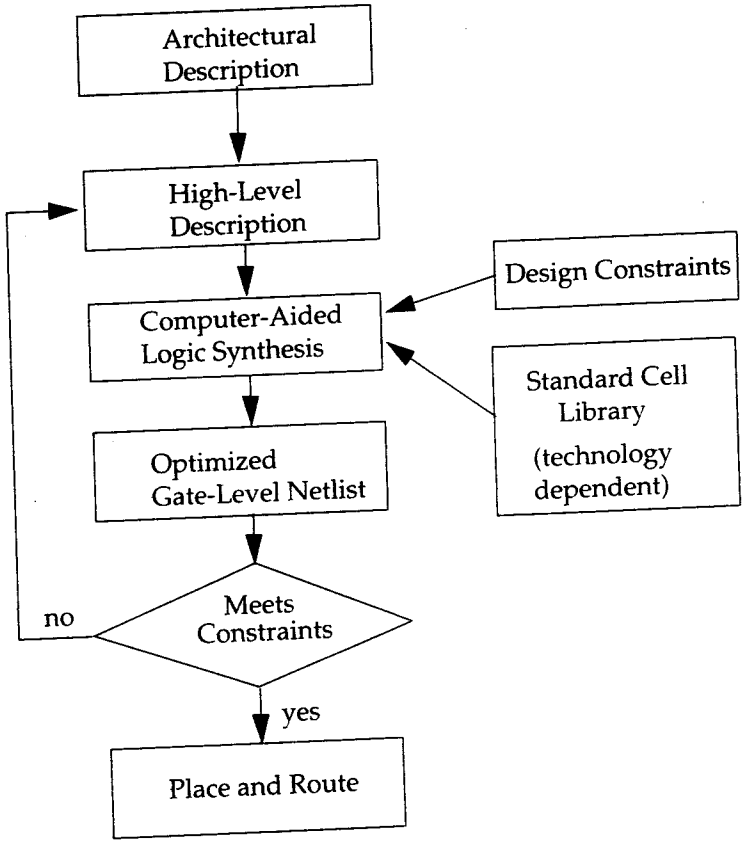

Figure 14-2 Basic Computer-Aided Logic Synthesis Process

Automated logic synthesis has significantly reduced time for conversion from high-level design representation to gates. This has allowed designers to spend more time on designing at a higher level of representation, because less time is required for converting the design to gates.