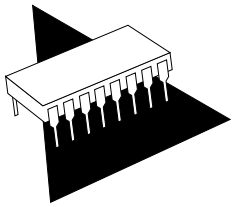

STD90/MDL90

0.35μm 3.3V CMOS Standard Cell Library for Pure Logic/MDL Products

STD90/MDL90
0.35μm 3.3V CMOS Standard Cell Library
for Pure Logic/MDL Products
Data Book

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Introduction

This databook contains information about STD90/MDL90 0.35μm 3.3V TLM/QLM standard cell library for pure logic products developed by SEC (Samsung Electronics Corporation).

The “library” basically contains various kinds of internal and I/O cells and soft-macros which are used for developing ASIC (Application Specific Integrated Circuit). It also includes a design kit helping designers to work in a workstation platform, and all sorts of design environments needed for an automatic chip design.

There are seven chapters in this databook:

In this databook each cell is followed by its AC electrical characteristics, and these characteristic values are almost equal when the corresponding cell is operated in a real chip.

The purpose of this databook is to prevent any misuse or misapplication of STD90/MDL90 cell library by providing precise information about the cell list, electrical data, directions for use, and matters demanding special attention.

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1 Introduction

2 Electrical Characteristics

3 Internal Macrocells

Flip-Flops

4 Input/Output Cells

Introduction

1

Table of Contents

1.1 Library Description

Samsung ASIC offers STD90/MDL90 as 0.35μm CMOS standard cell libraries based on a completely new blended process. Samsung's world-leading DRAM process is merged with a sophisticated 0.35μm cell-based logic process providing up to 4 layers of interconnect metal with various I/O pad–pitch options.

STD90/MDL90 can support up to three million gate count of logic providing 90% of usable gates with four layer metal. STD90/MDL90 is 40% faster than 0.5μm second generation library STD85. Logic density is 2.5 times greater than that of STD85.

A fully configurable memory compiler is available and datapath elements with up to 64 bit bus width are supported.

To support mixed voltage environments, 3.3V and 5V-tolerant IO cells are available. LVTTL, LVCMOS, Schmitt trigger, PCI and USB buffers are supported.

To better support a system-on-a-chip design style, various core cells are available including processor cores like ARM7TDMI, 80C51 and Oak. The list of analog core cells includes ADC, DAC, CODEC and PLL.

The STD90/MDL90 design kit supports Synopsys Design Compiler, VSS, Verilog-XL, Powerview, Mentor, Motive, Sunrise and IKOS. Samsung design methodology offers a comprehensive timing solution including static timing analysis, floorplanning, RC extraction and delay calculation with very deep-submicron solutions from leading EDA vendors. For the latest status and details, please refer to the design kit release notes.

1.2 Features

- 3.3V standard cell library including process cores, analog cores and DRAMs.
- 0.35μm quad layer metal HCMOS technology
  – Unified process for DRAM, logic and analog
- High basic cell usages
  – Up to 3 million gates
  – Maximum usage: 90% for quad layer metal
- High speed
  – Typical 2-input NAND gate delay(ND2D4): 91ps (F/O=2 + WL(0.03pF))
- Fully configurable Static RAMs and ROMs
  – Up to 512K-bit Diffusion/Metal-2 ROM available
  – Up to 128K-bit Single-Port Static RAM available
  – Up to 64K-bit Dual-Port Static RAM
- Configurable datapath elements available
  – 4-64 bit bus width
  – adder, ALU, barrel shifter, carry-select adder, multiplier, multi-port register file
- Operating Temperature (T_A)
  – Commercial range: 0˚C to +70˚C
  – Industrial range: –40˚C to +85˚C
- Selectable output current drive capability
  – 1/2/4/8/12/16/20/24mA available for 3.3V
  – 1/2/4/6mA available for 5V-tolerant output buffers
- 3.3V and 5V-tolerant I/O interface including LVTTL, LVCMOS, PCI, USB buffer.
- Processor core integration capability including ARM7TDMI, 80C51, Oak and others
- Analog core integration capability including ADC, DAC, CODEC, PLL and others
- Various package options
- Fully integrated CAD software support
  - Logic synthesis: Synopsys Design Compiler
  - Logic simulation: Cadence Verilog-XL, Cadence NC-Verilog, Viewlogic ViewSim, Mentor ModelSim-VHDL, Mentor ModelSim-Verilog, Synopsys VSS, Synopsys VCS
  - Scan insertion and ATPG: Synopsys TestGen, Synopsys Test Compiler, Mentor Fastscan
  - Static timing analysis: Synopsys PrimeTime, Synopsys MOTIVE
  - RC analysis: Avant! Star-RC
  - Power analysis: Synopsys DesignPower, CubicPower (In-House Tool)
  - Formal verification: Synopsys Formality, Chrysalis Design VERIFYer, Verplex Tuxedo-LEC
  - Fault simulation: Cadence Verifault, SuperTest (In-House Tool)
  - Delay calculator: CubicDelay (In-House Tool)
- Cell set optimized for synthesis

1.3 CAE Support

STD90/MDL90 supports a rich collection of industry-standard EDA tools from Cadence, Synopsys, Mentor graphics, and Avant! on multiple design platforms such as Solaris and HP. Customers are allowed to choose among the industry-leading EDA tools from design capture, synthesis, simulation, and DFT to layout. Several powerful proprietary software tools are seamlessly integrated in our design kits to improve your product quality.

For high simulation accuracy, STD90/MDL90 uses a proprietary delay calculator. Cell delay is calculated based on a matrix of delay parameters for each macrocell, and signal interconnect delay is calculated based on the RC tree analysis.

1.4 Product Family

STD90/MDL90 library include the following design elements:

- Internal Macrocells
- Compiled Macrocells
- Input/Output Cells
- JTAG Boundary Scans.

1.4.1 INTERNAL MACROCELLS

Macrocells are the lowest level of logic functions such as NAND, NOR and flip-flop used for logic designs. There are about 430 different types of internal macrocells. They usually come in three levels of drive strength (1X, 2X and 4X).

These macrocells have many levels of representations—logic symbol, logic model, timing model, transistor schematic, HSPICE netlist, physical layout, and placement and routing model.

1.4.2 COMPILED MACROCELLS

Compiled macrocells of STD90/MDL90 consist of compiled memory and compiled datapath macrocells.

Compiled memory macrocells include two types of single-port RAMs (synchronous and asynchronous), one dual-port RAM (synchronous) and two types of ROMs (synchronous diffusion and metal-2 programmable). Synchronous memories have a fully synchronous operation for clock. Asynchronous memories have a synchronous operation for Write Enable in write mode and have an asynchronous operation for address in read mode. Those compiled memories have an automatic power-down mode that significantly reduces power consumption for read and write operations. This power-down mode ensures that memory consumes power for the minimum amount of time needed for a read or write operation. For all memories, flexible memory aspect ratio is provided. In case of single-port synchronous SRAM, the bit-write capability is available. Now, a softmacro based memory BIST (Built-In Self Test) capability is available. Several memory macrocells of the same type or the different type in a circuit can be tested by single BIST circuit.

Compiled datapath macrocells include adder, ALU, barrel shifter, carry select adder, multiplier and multi-port register file. Adder supports both addition and subtraction and adopts a group-bypass carry propagation scheme to improve performance. ALU supports 9 arithmetic operations and 15 logical operations. Carry select adder is much faster than adder and adopts a double-carry propagation scheme to improve performance. Multiplier supports pipe-lined

scheme to improve performance and also accumulation scheme. Multi-port register file allows 1-to-2 write and 1-to-4 read ports and each port is fully independent. In write mode, this register file operates synchronously for clock. In read mode, it operates asynchronously for address.

We provide two kinds of engineering design services. One is to support additional compiled datapath macrocells such as Comparators, Detectors, Incrementers and Decrementers, Multiplexers, and so on. The other is to support hardwired datapath module design.

1.4.3 INPUT/OUTPUT CELLS

There are about four hundred different I/O buffers. Each I/O cell is implemented solely on the basic I/O cell architecture which forms the periphery of a chip.

A test logic is provided to enable the efficient parametric (threshold voltage) testing on input buffers including LVCMOS, CMOS and TTL level converters, Schmitt trigger input buffers, clock drivers and oscillator buffers. Pull-up and pull-down resistors are optional features.

Three basic types of output buffers (non-inverting, tri-state and open drain) are available in a range of driving capabilities from 1mA to 24mA for 3.3V drive and 1mA to 6mA for 5V-tolerant drive. One or two levels of slew rate controls are provided for each buffer type (except 1mA and 2mA buffers) to reduce output power/ground noise and signal ringing, especially in simultaneous switching outputs.

Bi-directional buffers are combinations of input buffers and output buffers (tri-state or open drain) in a single unit. The I/O structure has been fully characterized for ESD protection and latch-up resistance.

For user's convenience, STD90/MDL90 library provides 100KΩ pull-down and pull-up resistances respectively.

1.4.3.1 I/O Cell Drives Options

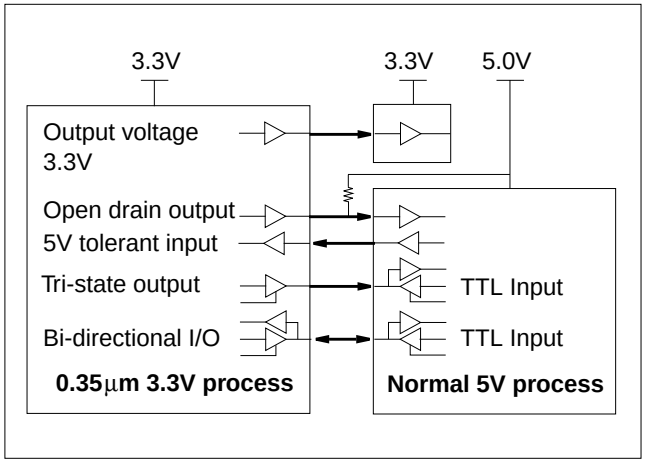
To provide designers with the greater flexibility, each I/O buffer can be selected among various current levels (e.g., 1mA, 2mA,..., 24mA). The choice of current-level for I/O buffers affects their propagation delay and current noise.

The slew rate control helps decrease the system noise and output signal overshoot/undershoot caused by the switching of output buffers. The output edge rate can be slowed down by selecting the high slew rate control cells. STD90/MDL90 provides three different sets of output slew rate controls. Only one I/O slot is required for any slew rate control options.

1.4.3.2 5V Tolerant I/O Buffers

STD90/MDL90 library is a process which has the most optimum performance in 3.3V. In this process, voltages more than 3.6V are not allowed at the gate oxide because of a reliability problem. And a special circuit is adopted in order to make pin voltage tolerable up to 5.25V and to offer TTL interface driving up to 6mA. Obviously, this circuit is constructed not to permit more than 3.6V at the gate oxide. The external circuit diagram is as follows.

The maximum external tolerance voltage of this buffer is 5.5V. And the leakage current of tri-state input pin and output pin is less than 100nA in 0 ~ 5V. It can be used as a 3.3V normal buffer.



1.4.3.3 PCI Buffers

In addition to input, output, bi-directional, slew rate controlled and Schmitt trigger I/O buffers, Samsung ASIC offers PCI (Peripheral Component Interconnect) 2.1 compliant I/O buffers. 3.3V for 33MHz and 5V-tolerant for 33MHz PCI buffers are included in the library.

1.4.3.4 USB (Universal Serial Bus) Buffers

Various kinds of peripheral equipments such as mouse, joy stick, keyboard, modem, scanner and printer improve the power of a computer. However, it is not easy to connect and use them properly in the computer.

USB specification established late in 1995 is a good solution for this problem, providing facile method of an expansion. Samsung ASIC offers full speed and low speed USB buffers.

1.5 Propagation Delays

Interconnection wire length, temperature and supply voltage are the chief factors affecting propagation delays.

1.5.1 WIRE LENGTH LOAD

Table 1-1. shows the equivalent standard load matrix for 3-layer and 4-layer metal interconnect. The equivalent standard load values are function of gatecount and fanout. These values are based on capacitive loading and are used in wire length estimates which affect propagation delay.

Table 1-1. Equivalent Standard loads for 3-layer and 4-layer Metal Interconnect

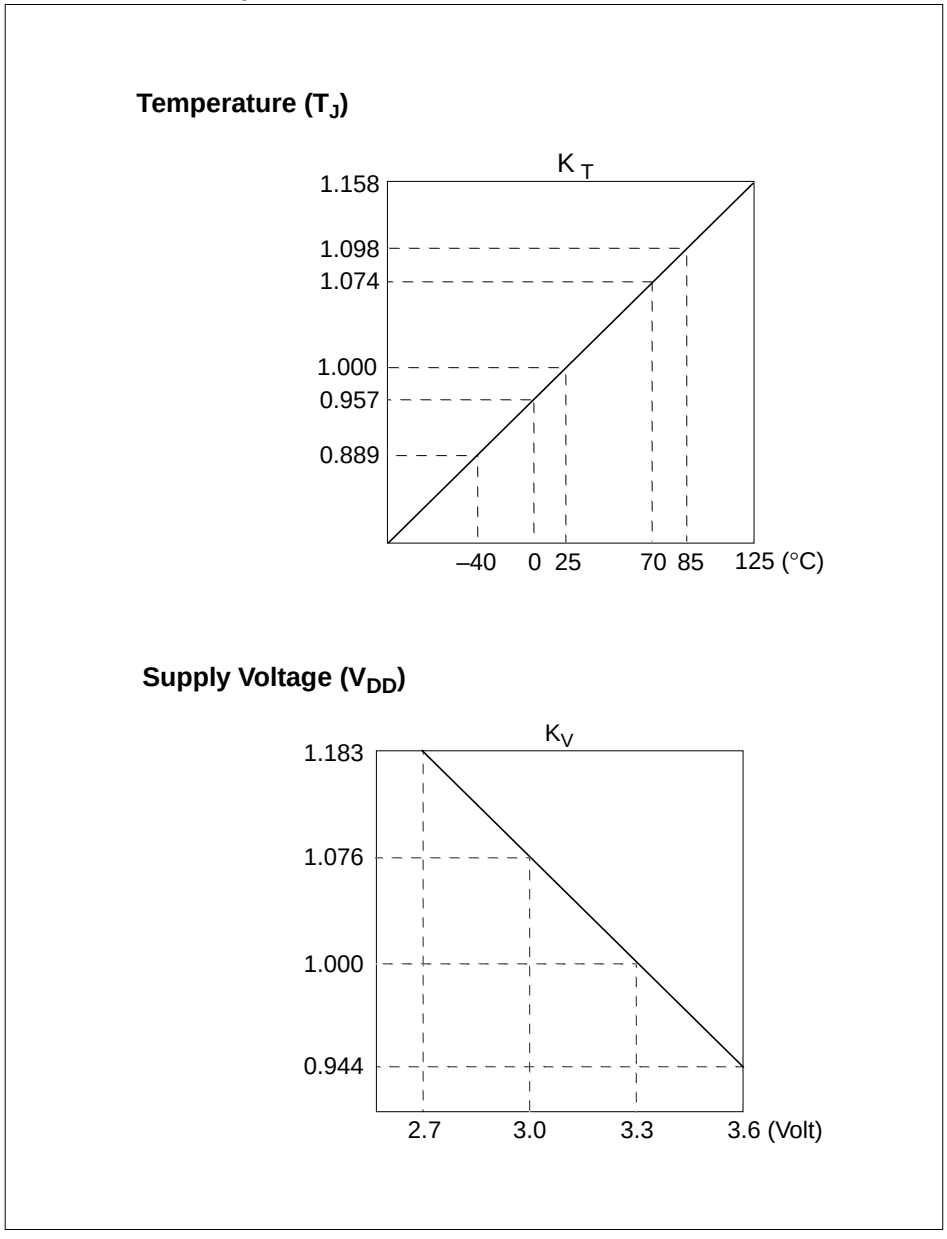
Gates Count	Fanouts										
	1	2	3	4	5	6	7	8	16	32	64
TLM											
5000	0.633	1.227	2.091	2.797	3.434	4.043	5.526	7.415	29.289	58.284	116.494
10000	0.837	1.605	3.042	4.213	5.162	6.047	6.974	10.304	30.547	60.946	121.893
50000	2.292	4.511	6.804	9.023	11.316	13.535	15.828	18.121	36.316	72.633	145.266
100000	2.514	5.103	7.618	10.133	12.721	15.236	17.751	20.340	40.754	81.508	163.017
150000	12.647	16.863	21.079	22.337	24.463	25.184	26.951	30.815	56.028	89.571	179.142
200000	13.313	17.751	22.189	23.520	25.758	26.516	28.374	32.442	58.894	94.156	188.239
300000	14.644	19.526	24.408	26.183	28.605	29.400	31.426	35.900	65.088	103.920	207.618
400000	15.976	21.301	26.442	28.254	30.935	31.841	34.070	38.849	70.358	112.130	223.964
500000	17.823	23.764	29.706	31.686	34.656	35.647	38.122	43.568	74.889	119.378	238.387
600000	19.080	25.440	31.980	34.065	37.227	38.269	40.910	46.838	77.036	122.828	245.226
800000	21.984	29.312	37.162	39.500	43.113	44.281	47.309	54.314	83.250	132.784	265.011
1000000	24.696	32.928	42.005	44.580	48.612	49.900	53.288	61.298	89.022	142.031	283.387
1500000	32.133	42.843	55.191	58.434	63.625	65.247	69.629	80.347	106.405	169.855	338.729
2000000	39.100	52.133	67.548	71.417	77.695	79.629	84.941	98.198	122.664	195.883	390.495
QLM											
5000	0.570	1.104	1.882	2.517	3.091	3.639	4.073	6.673	26.360	52.455	104.844
10000	0.753	1.444	2.738	3.792	4.646	5.442	6.277	9.274	27.492	54.852	109.704
50000	2.063	4.060	6.124	8.121	10.184	12.181	14.245	16.309	32.684	65.369	130.739
100000	2.263	4.593	6.856	9.119	11.449	13.713	15.976	18.306	36.678	73.357	146.715
150000	11.383	15.177	18.971	20.103	22.017	22.666	24.255	27.734	50.425	80.613	161.227
200000	11.982	15.976	19.970	21.168	23.182	23.864	25.536	29.198	53.005	84.741	169.415
300000	13.180	17.573	21.967	23.565	25.744	26.460	28.283	32.310	58.579	93.528	186.856
400000	14.378	19.171	23.798	25.428	27.842	28.657	30.663	34.965	63.323	100.917	201.568
500000	16.041	21.388	26.735	28.517	31.191	32.082	34.310	39.211	67.400	107.440	214.548
600000	17.172	22.896	28.782	30.658	33.504	34.442	36.819	42.154	69.333	110.545	220.703
800000	19.786	26.381	33.446	35.551	38.801	39.853	42.579	48.883	74.926	119.505	238.509
1000000	22.227	29.636	37.804	40.122	43.751	44.909	47.959	55.167	80.120	127.827	255.048
1500000	28.920	38.559	49.672	52.591	57.263	58.723	62.666	72.312	95.764	152.870	304.856
2000000	35.190	46.920	60.793	64.275	69.926	71.666	76.447	88.378	110.398	176.295	351.446
2500000	41.058	54.744	71.204	75.211	81.776	83.781	89.345	103.415	124.067	198.176	394.965
3000000	46.543	62.058	80.934	85.433	92.853	95.104	101.400	117.470	136.818	218.585	435.558

1.5.2 TEMPERATURE AND SUPPLY VOLTAGE

The next figure describes propagation delay derating factors (K_T, K_V) as a function of on-chip junction temperature (T_J) and supply voltage (V_{DD}). As a result of power dissipation, the junction temperature is generally higher than the ambient temperature.

The temperature of the die inside the package (junction temperature, T_J) is calculated using chip power dissipation and the thermal resistance to the ambient temperature (θ_{JA}) of the package. Information on package thermal performance can be obtained from Samsung application engineers.

Figure 1-1. Effect of Temperature and Supply Voltage on Propagation Delay



1.5.3 BEST AND WORST CASE CONDITIONS

A circuit should be designed to operate properly within a given specification level, either commercial or industrial. It is recommended that circuits be simulated for best case, normal case, and worst case conditions at each specification level.

The following expressions also allow for the effect of process variation on circuit performance.

Best case (Worst case):

T_{BC} (T_{WC}) = K_P x K_T x K_V x T_{NOM}

Worst case:

T_{WC} = K_{PWC} x K_T x K_V x T_{NOM}

where

T_{BC} = Best case propagation delay
T_{WC} = Worst case propagation delay
T_{NOM} = Normal propagation delay
(T_J = 25°C, V_{DD} = 3.3V and typical process)
K_P, K_T, K_V = Refer toTable 1-2., Table 1-3., and Table 1-4.

1.5.4 DERATING FACTORS OF STD90/MDL90

The multipliers can be applied to nominal delay data in order to estimate the effects of supply voltage, temperature and process. Nominal data are provided for conditions of V_{DD} = 3.3V, T_J = 25°C and typical process.

The derating factors of STD90/MDL90 is as follows.

Table 1-2. STD90/MDL90 Process Derating Factor (K_P)

Process Factor (K_P)	Slow	Typ	Fast
	1.3	1.0	0.7

Table 1-3. STD90/MDL90 Temperature Derating Factor (K_T)

Temp. (°C)	125	85	70	25	0	–40
K_T	1.158	1.098	1.074	1.000	0.957	0.889

Table 1-4. STD90/MDL90 Voltage Derating Factor (K_V)

Voltage (V)	3.6	3.3	3.0	2.7
K_V	0.944	1.000	1.076	1.183

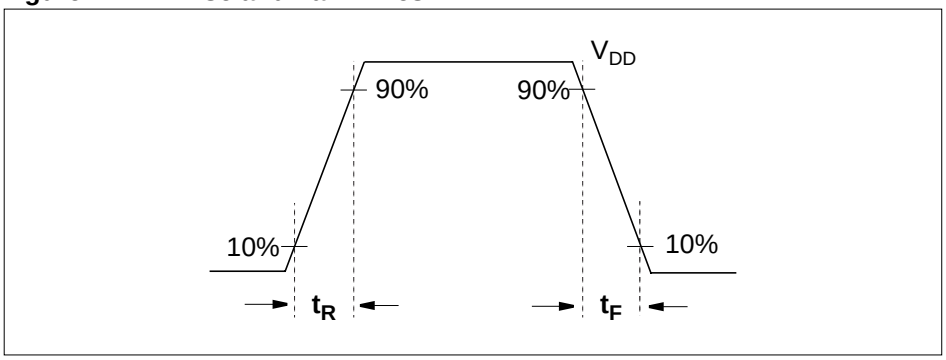
1.5.5 TIMING PARAMETERS

This section discusses issues involving timing parameters for primitive cells.

1.5.5.1 Rise / Fall Times

The definition of rise time (t_R) and fall time (t_F) is shown in the following figure.

Figure 1-2. Rise and Fall Times

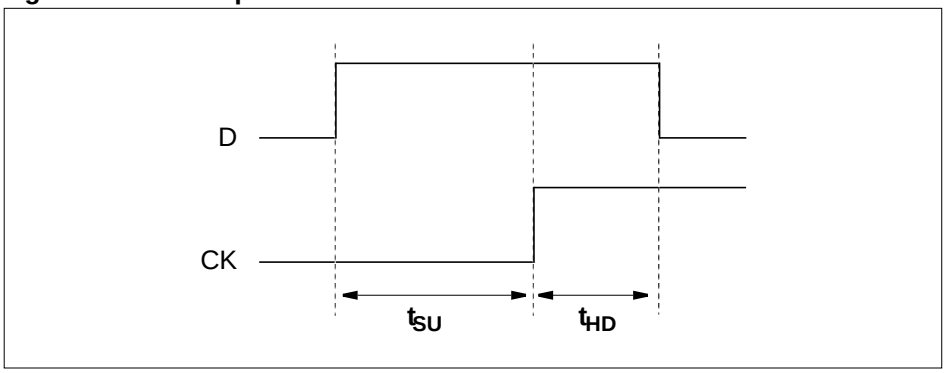


1.5.5.2 Setup / Hold Times

Setup time (t_{SU}) is a minimum period in which the input data to a flip-flop or a latch must be stable before the active edge of the clock occurs. Hold time (t_{HD}) is a minimum period in which the input data to a flip-flop or a latch must remain stable after the active edge of the clock has occurred.

The next figure shows the relationship between setup and hold times for a standard flip-flop triggered on the rising edge of the clock.

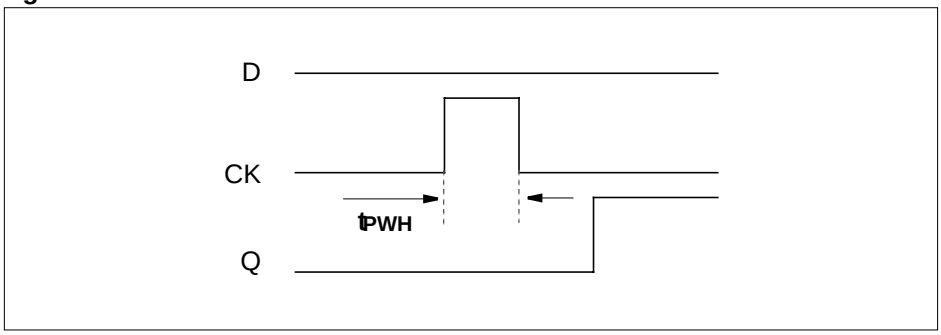
Figure 1-3. Setup and Hold Times



1.5.5.3 Minimum Pulse Widths

Minimum clock pulse widths (t_{PWH}, t_{PWL}) are the time intervals during a clock signal is high or low, so that it ensures proper operation of a flip-flop or a latch.

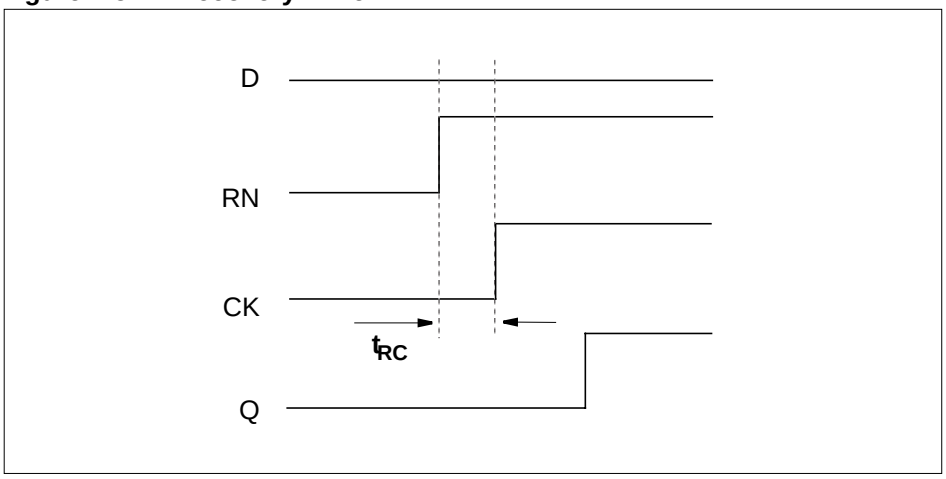
Figure 1-4. Minimum Pulse Width



1.5.5.4 Recovery Times

Recovery time (t_{RC}) is the minimum time after an asynchronous pin is disabled that an active clock edge will propagate data from input to output. If the active edge or clock occurs before the specified recovery time, the input data will not propagate.

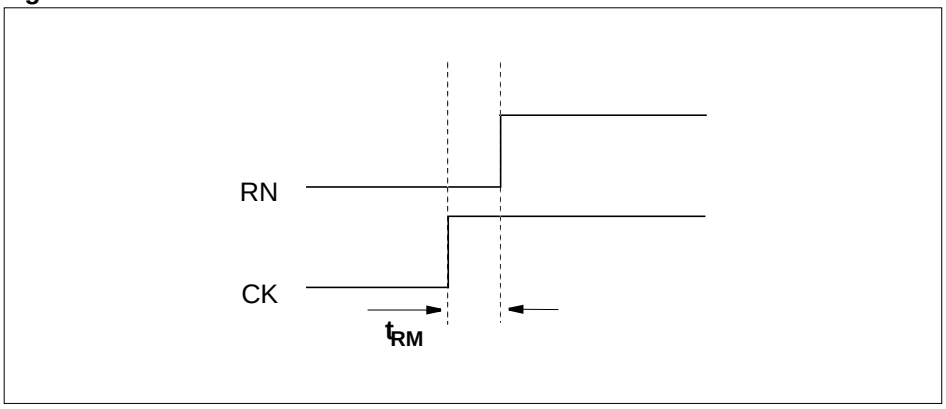
Figure 1-5. Recovery Time



1.5.5.5 Removal Times

Removal time (t_{RM}) is the minimum time in which the asynchronous set or reset pin to a F/F or a latch must remain enabled after the active edge of the clock has occurred. If the set or reset pin is disabled before the specified removal time, the input data may propagate incorrectly.

Figure 1-6. Removal Time

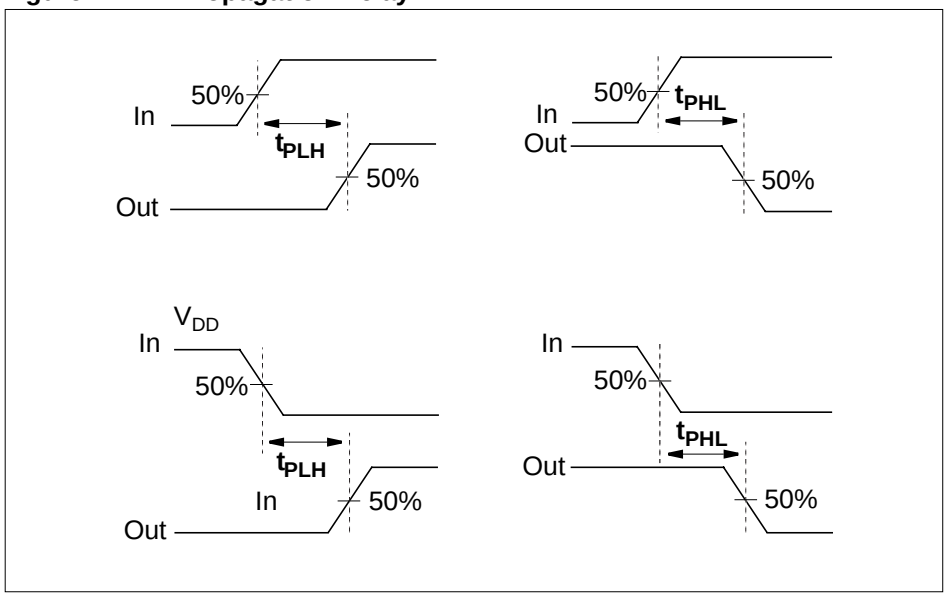


1.5.5.6 Propagation Delays

A delay for a macrocell is considered to be a rising delay (t_{PLH}) if the signal on the output pin is rising. For a rising input and a rising output, the rising delay is the interval between the times the input becomes 50% of supply voltage (V_{DD}) and the output becomes 50% of V_{DD}.

If the input is falling and the output is rising, the rising delay is the interval between the times the input falls to 50% of V_{DD} and the output rises to 50% of V_{DD}. The converse is true for a falling delay (t_{PHL}).

Figure 1-7. Propagation Delay

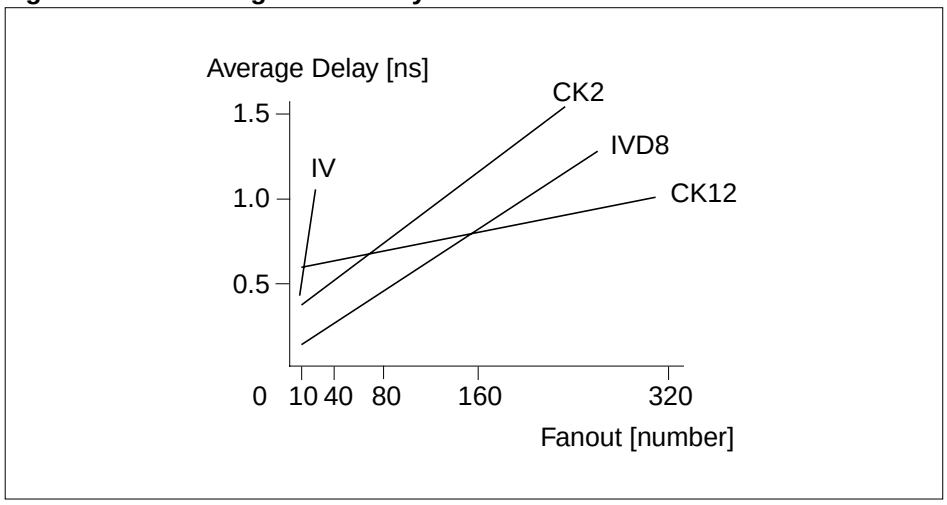


1.5.6 PROPER USE OF BUFFERS

Figure 1-8. shows the average propagation delays of an internal inverter (IV), an 8X inverter (IVD8), a normal clock driver (CK2), and a high clock driver (CK12) in STD90/MDL90.

Note that transistors used in I/O buffers over CK6 are larger and have lower ON channel resistance than those of the N and P channel transistors in primitive cells. CK2 and CK4 can be used as clock driver for core limited design and clock driver over CK6 can be used for high fanout signals.

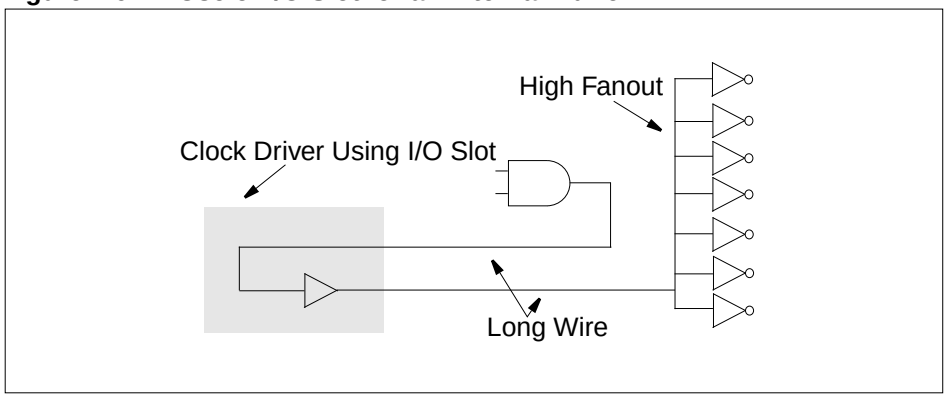
Figure 1-8. Average Gate Delay in STD90/MDL90



One caution, emphasized in Figure 1-9. shows that if you route to a buffer that uses an I/O slot from an internal element and back into internal logic, the additional wiring needed could increase propagation delays materially. Higher drive strength internal cells may be more appropriate than I/O slot buffers.

Realize also that using I/O slot cells for internal buffering removes those locations for use as external I/Os and uses two wiring channels, thereby increasing routability congestion on master slice products.

Figure 1-9. Use of I/O Slot for an Internal Buffer



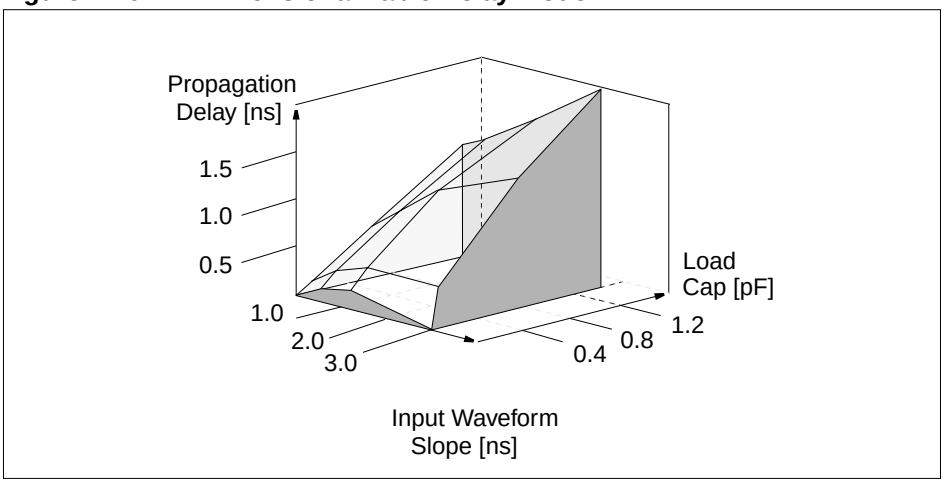
1.6 Delay Model

The ASIC timing characteristics consist of the following components:

- Cell propagation delay from input to output transitions based on input waveform slope, fanout loads and distributed interconnection wire resistance and capacitance.
- Interconnection wire delay across the metal lines.
- Timing requirement parameters such as setup time, hold time, recovery time, skew time, minimum pulse width, etc.
- Derating factors for junction temperature, power supply voltage, and process variations.

Timing model for STD90/MDL90 focuses on how to characterize cell propagation delay time accurately. To accomplish this goal, 2-dimensional table look-up delay model has been adopted. The index variables of this table are input waveform slope and output load capacitance. See the figure below. Samsung ASIC design automation system supports an n-dimensional table model even though we adopted 2-dimensional model for our 0.35μm cell-based products.

Figure 1-10. 2-Dimensional Table Delay Model



The Table 1-5. shows an example of this model for 2-input NAND cell. The data in this table are high-to-low transition delay times from one of the two input pins to output pin. The number of points and values of the index variables can differ for each cell.

Table 1-5. Table Delay Model Example

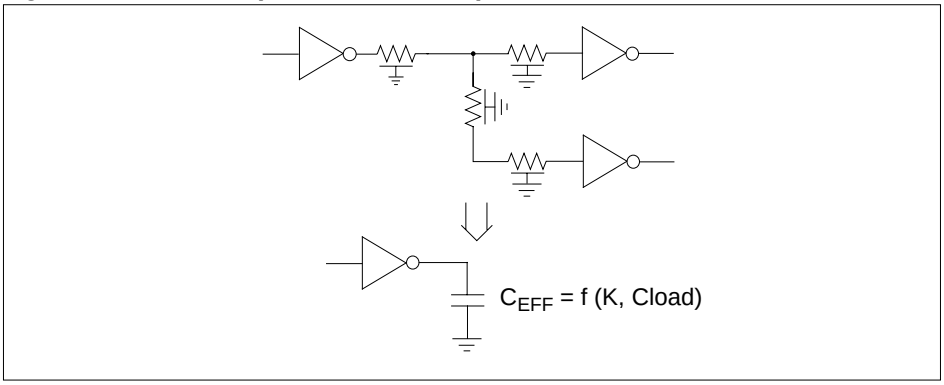
SLOPE \ CAP	0.011	0.043	0.504	0.964
0.024	0.06060	0.12196	0.78281	1.44330
0.255	0.08601	0.15686	0.81447	1.47460
1.627	0.11397	0.24258	1.03300	1.67820
3.000	0.09984	0.26318	1.21660	1.90920

Notice that 4-by-4 table is used. Delay values between grid points and beyond this table are determined by linear interpolation and extrapolation methods. This general table delay model provides great flexibility as well as high accuracy since extensive software revisions are not required when a cell library is updated. The other timing components such as interconnection wire delay, timing requirement parameters and derating factors are characterized in a commonly-accepted way in industry.

The delay time due to the interconnection wire can be separated into two components. One is the signal propagation delay time across the metal lines. This delay time component is computed through conventional RC analysis based on $\prod$-model. The other is an additional delay on the driving cell due to the wire load. The traditional way to compute this is based on the lumped capacitance model, ignoring wire resistance.

For sub-micron technology, this approximation cannot be accepted any more. The wire resistance has a shielding effect on the driving cell from load capacitances. An effective capacitance C_{EFF}, a single capacitance approximating distributed interconnection wire resistance and capacitance, is derived, as illustrated in the following figure. The compensation factor K, extracted for each cell, is a function of the length of interconnection wires and the layout topology. All these effects are merged to determine the effective capacitance and this value is used as an index of the table delay model.

Figure 1-11. Concept of Effective Capacitance



The figure below summarizes the features of Samsung ASIC's delay model.

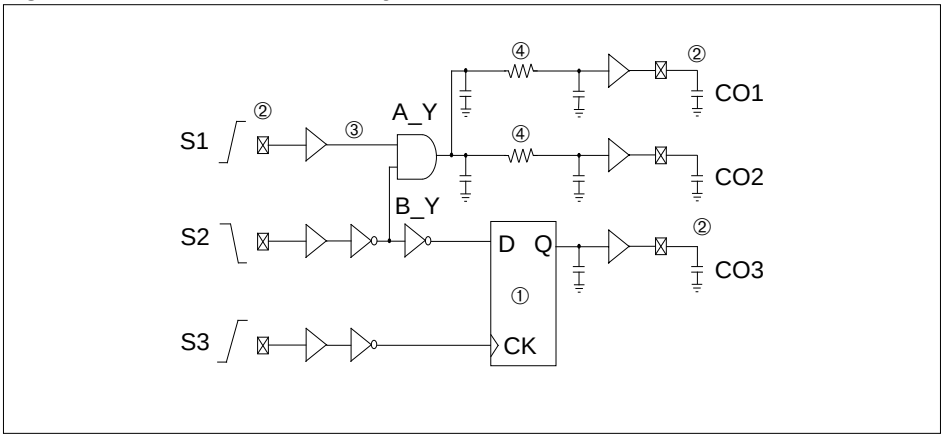
① 2-dimensional table delay model for output loading and input waveform slope effects is used.The slopes (t_R, t_F) and delay times (t_{PLH}, t_{PHL}) of all cell instances are calculated recursively.

② The input waveform slope of each primary input pad and the loading capacitance of each primary output pad can be assigned individually or by default.

③ Pin to pin delays of cells and interconnection wires are supported.

④ The effect of distributed interconnection wire resistance and capacitance on cell delay is analysed using the effective capacitance concept.

Figure 1-12. Features of Delay Model



1.7 Testability Design Methodology

1.7.1 SCAN DESIGN

- Multiplexed scan flip-flop that minimizes the area or delay overhead needed to implement scan design.
- Automated design rules checking, scan insertion, and test pattern generation
- High fault coverage on synchronous designs

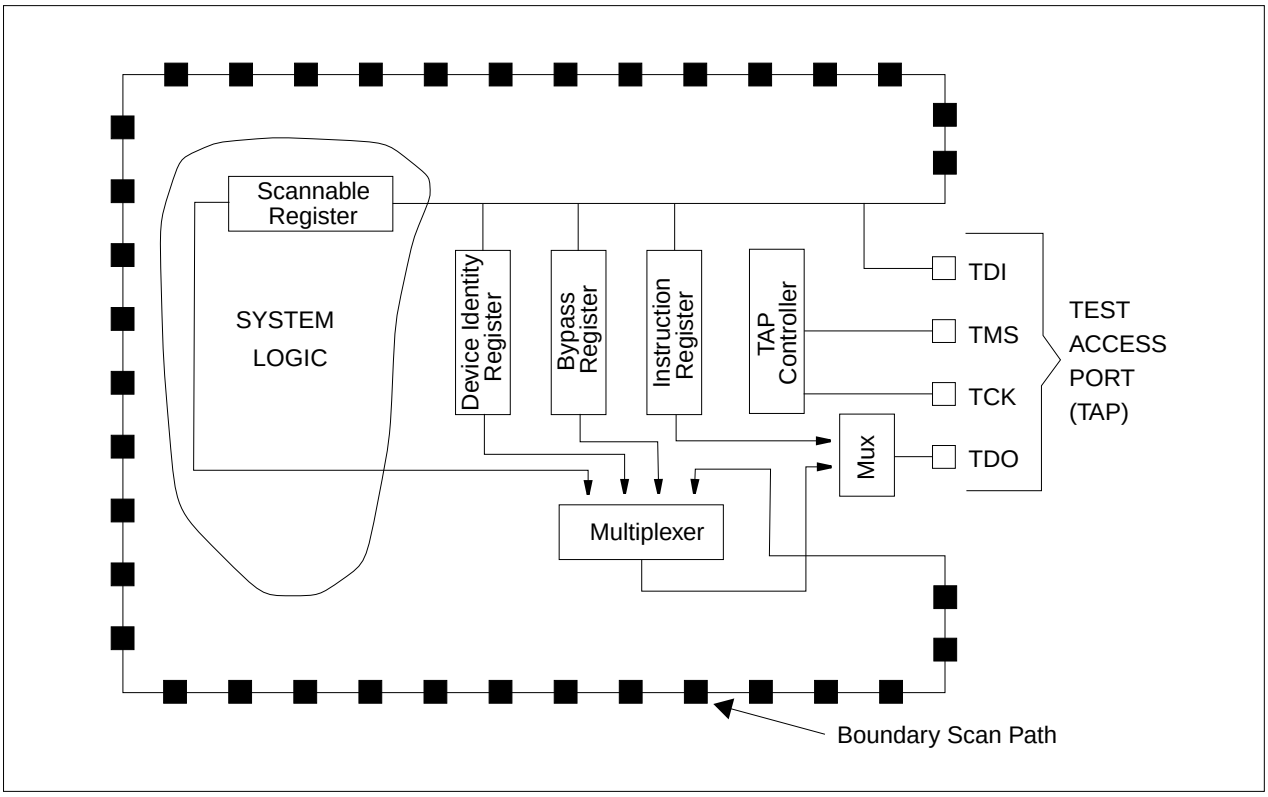
1.7.2 BOUNDARY-SCAN

- IEEE Std 1149.1
- JTAG boundary-scan registers with primitive cells
- Boundary-Scan Description Language (BSDL) description for board testing
- Combination with internal scan design and core testing

Boundary Scan Architecture

A boundary scan architecture contains TAP (Test Access Port), TAP controller, instruction register and a group of test data registers. The instruction and test data registers are separate shift-register-based paths connected in parallel with a common serial data input and a common serial data output which are connected to TAP, TDI and TDO signals. TAP controller selects the alternative instruction and test data register paths between TDI and TDO. The schematic view of the top level design of the test logic architecture is shown in the Figure 1-13.

Figure 1-13. JTAG Test Access Port (TAP) Block Diagram



Boundary Scan Functional Block Descriptions

TAP (Test Access Port)

TAP is a general-purpose port that can provide with an access to many test support functions built into a component, including the test logic. It includes three inputs (TCK; Test Clock Signal, TMS; Test Mode Signal and TDI; Test Data Input) and one output (TDO; Test Data Output) required by the test logic. An optional fourth input (TRSTN; Test Reset) is provided for the asynchronous initialization of the test logic. The values applied at TMS and TDI pins are sampled on the rising edge of TCK, and the value placed on TDO pin changes on the falling edge of TCK.

TAP Controller

TAP controller receives TCK, interprets the signals on TMS, and generates clock and control signals for both instruction and test data registers and for other parts of the test circuitries as required.

Instruction Register/Instruction Decoder

Test instructions are shifted into and held by the instruction register. Test instructions include a selection of tests to be performed or the test data register to be accessed. A basic 3-bit instruction register and its instruction decoder are provided as macrofunctions in the library.

Test Data Registers

Data registers include a bypass register, a boundary scan register, a device identification register and other design specific registers. Only the bypass- and boundary scan registers are mandatory; the rest are optional.

Bypass register: The bypass register provides a single-bit serial connection through the circuit when none of the other test data registers is selected. It can be used to allow test data to flow through a given device to the other components in a product without affecting a normal operation.

Boundary scan register: The boundary scan register detects typical production defects in board interconnects, such as opens, shorts, etc. It also allows an access to component inputs and outputs when you test their logic or sample flow-through signals. Special boundary scan register macrocells are provided for this purpose. These special registers is discussed in the next section of next pages.

Design-specific test data register: These optional registers may be provided to allow an access to design-specific test support features in the integrated circuit, such as self-test, scan test.

Device identification register: This is an optional test data register that allows the manufacturer part number and variant of a components to be identified. The 32-bit identification register is partitioned into four fields:

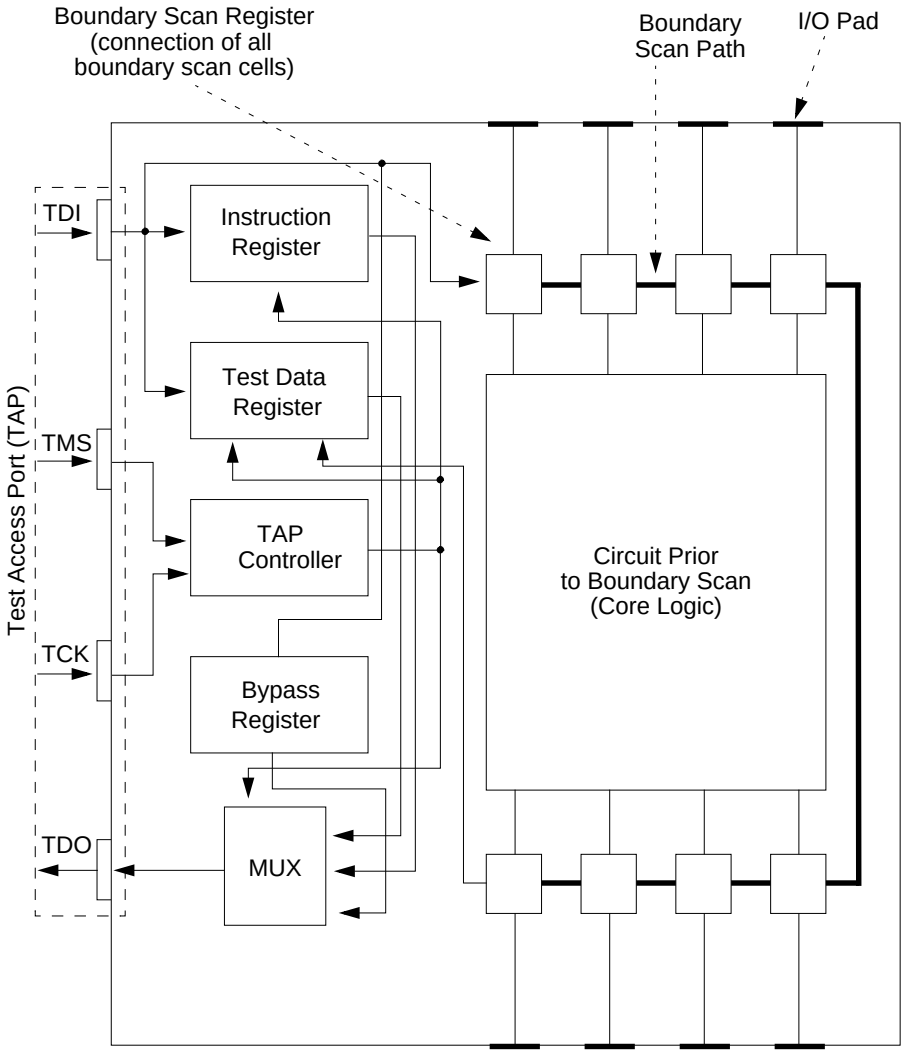
Device version identifier1st field	The first four bits beginning from MSB	
Device part number	2nd field	16 bits
Manufacturer's JEDEC number	3rd field	11 bits
LSB	4th field	1 bit —tied in High

The ASIC designer is free to fill the version and part number in any manner as long as the total twenty bits are used.

Samsung's JEDEC code: 78 decimal = 1001110
Continuation field (4 bits) = 0000

Contents of device identification register:

XXXX XXXXXXXXXXXXXXX 0000 1001110 1
Users can define these two fields.



1.7.3 BIST (BUILT-IN SELF-TEST)

- Efficient test solution for compiled memory macrocells
- At speed and parallel testing of multiple memories
- Less routing overhead and test pin requirements

1.8 Maximum Fanouts

1.8.1 INTERNAL MACROCELLS

The maximum fanouts for STD90/ MDL90 primitive cells are as follows. Note that these fanout limitation values are calculated when the rise and fall times of the input signal is 0.255ns. Depending on the rise and fall times, the maximum fanout limitations can be varied case by case.

In the following table the maximum fanout values for all pins of STD90/ MDL90 internal macrocells are listed.

Table 1-6. Maximum Fanouts of Internal Macrocells
(t_R/t_F = 0.255ns, one fanout (SL) = 0.01352pF)

Cell Name	Out put Pin	Maximum Fanout
Logic Cells		
AD2	Y	76
AD2D2	Y	151
AD2D4	Y	305
AD3DH	Y	41
AD3	Y	76
AD3D2	Y	151
AD3D4	Y	305
AD4DH	Y	41
AD4	Y	76
AD4D2	Y	151
AD4D4	Y	305
AD5	Y	39
AD5D2	Y	78
AD5D4	Y	304
ND2DH	Y	39
ND2	Y	67
ND2D2	Y	134
ND2D4	Y	268
ND3DH	Y	33
ND3	Y	54
ND3D2	Y	109
ND3D4	Y	219
ND4DH	Y	28
ND4	Y	42
ND4D2	Y	84
ND4D2B	Y	152
ND4D4	Y	304
ND5	Y	77
ND5D2	Y	152
ND5D4	Y	304
ND6	Y	77
ND6D2	Y	152
ND6D4	Y	304
ND8	Y	77
ND8D2	Y	153
ND8D4	Y	304
NR2DH	Y	21
NR2	Y	39
NR2D2	Y	79
NR2D2B	Y	152
NR2D4	Y	304
NR3DH	Y	13
NR3	Y	25
NR3D2	Y	51
NR3D2B	Y	153
NR3D4	Y	308
NR4DH	Y	10
NR4	Y	18
NR4D2	Y	37
NR4D2B	Y	153
NR4D4	Y	305
NR5	Y	76
NR5D2	Y	151
NR5D4	Y	305
NR6	Y	76
NR6D2	Y	151
NR6D4	Y	305
NR8	Y	76
NR8D2	Y	151
NR8D4	Y	305
OR2DH	Y	41
OR2	Y	76
OR2D2	Y	152
OR2D4	Y	304
OR3DH	Y	41
OR3	Y	76
OR3D2	Y	151
OR3D4	Y	304
OR4DH	Y	41
OR4	Y	76
OR4D2	Y	151
OR4D4	Y	304
OR5	Y	65
OR5D2	Y	130
OR5D4	Y	260
XN2	Y	76
XN2D2	Y	151
XN2D4	Y	305
XN3	Y	76
XN3D2	Y	151
XN3D4	Y	303
XO2	Y	76
XO2D2	Y	151
XO2D4	Y	305
XO3	Y	76
XO3D2	Y	151
XO3D4	Y	302
AO21	Y	38
AO21D2	Y	75
AO21D2B	Y	152
AO21D4	Y	304
AO211	Y	24
AO211D2	Y	49
AO211D2B	Y	151
AO211D4	Y	305
AO2111	Y	17
AO2111D2	Y	35
AO22	Y	37
AO22D2	Y	74
AO22D2B	Y	152
AO22D4	Y	304
AO22A	Y	37
AO22D2A	Y	152
AO22D4A	Y	304
AO221	Y	23
AO221D2	Y	48
AO221D4	Y	305
AO222	Y	23
AO222D2	Y	47
AO222D2B	Y	152
AO222D4	Y	305
AO222A	Y	36
AO222D2A	Y	152
AO222D4A	Y	305
AO2222	Y	16
AO2222D2	Y	152
AO2222D4	Y	305
AO31	Y	37
AO31D2	Y	74

Cell Name	Out put Pin	Maximum Fanout
AO31D4	Y	304
AO311	Y	23
AO311D2	Y	47
AO311D4	Y	305
AO3111	Y	16
AO3111D2	Y	33
AO32	Y	36
AO32D2	Y	152
AO32D4	Y	304
AO321	Y	22
AO321D2	Y	152
AO321D4	Y	305
AO322	Y	22
AO322D2	Y	152
AO322D4	Y	305
AO33	Y	35
AO33D2	Y	152
AO33D4	Y	304
AO331	Y	22
AO331D2	Y	152
AO331D4	Y	305
AO332	Y	21
AO332D2	Y	152
AO332D4	Y	305
AO4111	Y	16
AO4111D2	Y	152
OA21	Y	38
OA21D2	Y	77
OA21D2B	Y	152
OA21D4	Y	304
OA211	Y	36
OA211D2	Y	72
OA211D2B	Y	152
OA211D4	Y	304
OA2111	Y	33
OA2111D2	Y	67
OA22	Y	37
OA22D2	Y	74
OA22D2B	Y	152
OA22D4	Y	305
OA22A	Y	39
OA22D2A	Y	77
OA22D4A	Y	304
OA221	Y	32
OA221D2	Y	66
OA221D4	Y	304
OA222	Y	27
OA222D2	Y	55
OA222D2B	Y	151
OA222D4	Y	305
OA2222	Y	21
OA2222D2	Y	151
OA2222D4	Y	305
OA31	Y	25
OA31D2	Y	50
OA31D4	Y	304
OA311	Y	24
OA311D2	Y	49
OA311D4	Y	304
OA3111	Y	21
OA3111D2	Y	48
OA32	Y	24
OA32D2	Y	48
OA32D4	Y	305
OA321	Y	23
OA321D2	Y	152
OA321D4	Y	304
OA322	Y	22
OA322D2	Y	152
OA322D4	Y	305
OA33	Y	22
OA33D2	Y	46
OA33D4	Y	305

Cell Name	Out put Pin	Maximum Fanout
OA331	Y	22
OA331D2	Y	152
OA331D4	Y	305
OA332	Y	20
OA332D2	Y	152
OA332D4	Y	305
OA4111	Y	17
OA4111D2	Y	152
SCG1	Y	55
SCG2	Y	76
SCG3	Y	55
SCG4	Y	65
SCG5	Y	76
SCG6	Y	76
SCG7	Y	67
SCG8	Y	76
SCG9	Y	76
SCG10	Y	76
SCG11	Y	25
SCG12	Y	39
SCG13	Y	67
SCG14	Y	66
SCG15	Y	55
SCG16	Y	39
SCG17	Y	67
SCG18	Y	55
SCG19	Y	38
SCG20	Y	39
SCG21	Y	25
SCG22	Y	39
SCG23	S	76
	CO	76
DL1D2	Y	126
DL1D4	Y	268
DL2D2	Y	126
DL2D4	Y	268
DL3D2	Y	126
DL3D4	Y	268
DL4D2	Y	126
DL4D4	Y	268
DL5D2	Y	126
DL5D4	Y	268
DL10D2	Y	126
DL10D4	Y	268
IVDH	Y	41
IV	Y	76
IVD2	Y	152
IVD3	Y	228
IVD4	Y	305
IVD6	Y	456
IVD8	Y	608
IVD16	Y	1221
IVCD11	Y	75
	YN	76
IVCD13	Y	73
	YN	228
IVCD22	Y	150
	YN	152
IVCD26	Y	144
	YN	456
IVCD44	Y	301
	YN	305
IVT	Y	69
IVTD2	Y	135
IVTD4	Y	274
IVTD8	Y	545
IVTD16	Y	1093
IVTN	Y	68
IVTND2	Y	135
IVTND4	Y	274
IVTND8	Y	545
IVTND16	Y	1094
NIDH	Y	41

Cell Name	Out put Pin	Maximum Fanout
NID	Y	76
NID2	Y	152
NID3	Y	228
NID4	Y	304
NID6	Y	455
NID8	Y	607
NID16	Y	1218
NIT	Y	68
NITD2	Y	135
NITD4	Y	274
NITD8	Y	545
NITD16	Y	1092
NITN	Y	68
NITND2	Y	135
NITND4	Y	274
NITND8	Y	545
NITND16	Y	1092
Flip-Flops		
FD1	Q	76
	QN	76
FD1D2	Q	151
	QN	151
FD1CS	Q	76
	QN	76
FD1CSD2	Q	152
	QN	152
FD1S	Q	76
	QN	76
FD1SD2	Q	152
	QN	152
FD1SQ	Q	76
FD1SQD2	Q	152
FD1Q	Q	76
FD1QD2	Q	151
FD2	Q	76
	QN	76
FD2D2	Q	151
	QN	152
FD2CS	Q	77
	QN	77
FD2CSD2	Q	153
	QN	153
FD2S	Q	76
	QN	76
FD2SD2	Q	151
	QN	152
FD2SQ	Q	76
FD2SQD2	Q	151
FD2Q	Q	76
FD2QD2	Q	151
FD3	Q	76
	QN	76
FD3D2	Q	152
	QN	152
FD3CS	Q	76
	QN	76
FD3CSD2	Q	152
	QN	151
FD3S	Q	76
	QN	76
FD3SD2	Q	152
	QN	151
FD3SQ	Q	76
FD3SQD2	Q	152
FD3Q	Q	76
FD3QD2	Q	152
FD4	Q	76
	QN	76
FD4D2	Q	151
	QN	151
FD4CS	Q	76
	QN	76

Cell Name	Out put Pin	Maximum Fanout
FD4CSD2	Q	151
	QN	151
FD4S	Q	76
	QN	76
FD4SD2	Q	151
	QN	151
FD4SQ	Q	76
FD4SQD2	Q	151
FD4Q	Q	76
FD4QD2	Q	151
FD5	Q	76
	QN	76
FD5D2	Q	152
	QN	152
FD5S	Q	76
	QN	76
FD5SD2	Q	152
	QN	152
FD6	Q	76
	QN	76
FD6D2	Q	151
	QN	151
FD6S	Q	76
	QN	76
FD6SD2	Q	151
	QN	152
FD7	Q	76
	QN	76
FD7D2	Q	152
	QN	151
FD7S	Q	76
	QN	76
FD7SD2	Q	152
	QN	152
FD8	Q	76
	QN	76
FD8D2	Q	151
	QN	151
FD8S	Q	76
	QN	76
FD8SD2	Q	151
	QN	151
FDS2	Q	76
	QN	76
FDS2D2	Q	152
	QN	152
FDS2CS	Q	76
	QN	76
FDS2CSD2	Q	152
	QN	152
FDS2S	Q	76
	QN	76
FDS2SD2	Q	152
	QN	152
FDS3	Q	76
	QN	76
FDS3D2	Q	152
	QN	152
FDS3CS	Q	76
	QN	76
FDS3CSD2	Q	152
	QN	152
FDS3S	Q	76
	QN	76
FDS3SD2	Q	152
	QN	152
FJ1	Q	76
	QN	77
FJ1D2	Q	152
	QN	152
FJ1S	Q	76
	QN	77

Cell Name	Out put Pin	Maximum Fanout
FJ1SD2	Q	152
	QN	151
FJ2	Q	76
	QN	76
FJ2D2	Q	151
	QN	152
FJ2S	Q	76
	QN	76
FJ2SD2	Q	151
	QN	152
FJ4	Q	76
	QN	76
FJ4D2	Q	151
	QN	151
FJ4S	Q	76
	QN	76
FJ4SD2	Q	151
	QN	151
FT2	Q	76
	QN	76
FT2D2	Q	151
	QN	151
Latches		
LD1	Q	76
	QN	76
LD1D2	Q	152
	QN	151
LD1A	Q	47
LD1D2A	Q	94
LD1Q	Q	76
LD1QD2	Q	152
LD2	Q	76
	QN	76
LD2D2	Q	151
	QN	152
LD2Q	Q	77
LD2QD2	Q	153
LD3	Q	76
	QN	76
LD3D2	Q	152
	QN	151
LD4	Q	76
	QN	76
LD4D2	Q	151
	QN	151
LD5	Q	76
	QN	76
LD5D2	Q	152
	QN	151
LD5S	Q	76
	QN	76
LD5SD2	Q	152
	QN	152
LD5Q	Q	76
LD5QD2	Q	152
LD6	Q	76
	QN	76
LD6D2	Q	151
	QN	152
LD6Q	Q	77
LD6QD2	Q	153
LD7	Q	76
	QN	76
LD7D2	Q	152
	QN	151
LD8	Q	76
	QN	76
LD8D2	Q	152
	QN	151
LS0	Q	66
	QN	65
LS0D2	Q	128
	QN	128

Cell Name	Out put Pin	Maximum Fanout
LS1	Q	44
	QN	44
LS1D2	Q	152
	QN	152
Busholder Holder		
busholder	Y	10000
Decoders		
DC4	Y0	76
	Y1	76
	Y2	76
	Y3	76
DC4I	YN0	67
	YN1	67
	YN2	66
	YN3	66
DC8I	YN0	54
	YN1	54
	YN2	54
	YN3	54
	YN4	54
	YN5	54
	YN6	54
	YN7	54
Adders		
FADH	S	41
	CO	41
FA	S	76
	CO	76
FAD2	S	151
	CO	151
HADH	S	41
	CO	41
HA	S	76
	CO	76
HAD2	S	151
	CO	151
Multiplexers		
MX2DH	Y	41
MX2	Y	76
MX2D2	Y	151
MX2D4	Y	305
MX2X4	Y0	76
	Y1	76
	Y2	76
	Y3	76
MX2IDH	YN	41
MX2I	YN	76
MX2ID2	YN	152
MX2ID4	YN	305
MX2IDHA	YN	20
MX2IA	YN	37
MX2ID2A	YN	153
MX2ID4A	YN	305
MX2IX4	YN0	76
	YN1	76
	YN2	76
	YN3	76
MX3I	YN	76
MX3ID2	YN	151
MX3ID4	YN	305
MX4	Y	76
MX4D2	Y	151
MX4D4	Y	303
MX8	Y	75
MX8D2	Y	150
MX8D4	Y	299

1.8.2 I/O Cells

The maximum fanouts for I/O cells are as follows.

Table 1-7. Maximum Fanouts of I/O Cells
(t_R/t_F = 0.255ns, one fanout (SL) = 0.01352pF)

Cell Name	Output Pin	Maximum Fanouts
pic	Y	281
pic_abb	Y	281
picc_abb	Y	280
picd	Y	281
picu	Y	281
pipci	Y	1575
pis	Y	279
pisd	Y	279
pisu	Y	279
psosck1	YN	110
psosck17	YN	110
psosck2	YN	110
psosck27	YN	110
psoscm1	YN	27
psoscm16	YN	27
psoscm2	YN	343
psoscm26	YN	344
psoscm3	YN	797
psoscm36	YN	797
ptic	Y	276
pticd	Y	276
pticu	Y	276
ptipci3	Y	162
ptipci5	Y	162
ptis	Y	276
ptisd	Y	275
ptisu	Y	275

1.8.2 CK CELL MAX FANOUT

STD90/MDL90 max fanout for ck cells

<Condition>
- VDD = 3.3V
- Fanout = 0.00945pF (= input cap for CK pin of FD1)
- Standard Load (SL) = 0.01352pF
- Input slope = 0.255ns
- Max output transition time (mott) = 3.0ns
- Maximum frequency $\leq$ 150MHz
- Net length (μm/fanout): branch net length for each fanout except trunk

Table 1-8. Maximum Fanout of Clock Cells

Trunk width (μm)	8				In case that interconnection is not considered
Net length (μm/fanout)	20		200		
Trunk length (μm)	5000	10000	5000	10000	
ck2	354	267	122	92	556
ck4	758	633	262	219	1112
ck6	1125	936	389	324	1651
ck8	1478	1201	510	415	2204
ck12	2106	1596	721	550	3287
ck16	2643	1865	897	641	4359
ck20	3082	2039	1041	700	5146

1.8.3 I/O CELLS

The maximum fanouts for I/O cells are as follows.

Table 1-9. Maximum Fanout for NID Cells

Trunk width (μm)	0.6		8		In case that interconnection is not considered
Net length (μm/fanout)	20		200		
Trunk length (μm)	5000	10000	5000	10000	
nid	19	.	.	.	76
nid2	67	16	15	.	152
nid3	109	43	36	9	228
nid4	143	62	56	28	304
nid6	197	87	95	65	455
nid8	235	102	134	101	607
nid16	315	129	279	228	1218

For high fanout nets including clock net, Samsung strongly recommends using clock tree synthesis.

1.9 Product Line-Up

Table 1-9. Optimum Gates vs. Pad Numbers on STD90/MDL90

Ref. No	Estimated Gates	Total Pads
01	30,000	76
02	50,000	100
03	100,000	144
04	150,000	180
05	200,000	208
06	250,000	232
07	300,000	256
08	350,000	276
09	400,000	296
10	500,000	340
11	600,000	372
12	700,000	404
13	800,000	432
14	900,000	456
15	1,000,000	516
16	1,200,000	564
17	1,400,000	608
18	1,600,000	652
19	1,800,000	692
20	2,000,000	756
21	2,500,000	844
22	3,000,000	928

NOTE: Chip size can be changed depending on the circuit design.

1.10 Package Capability By Lead Count

Package	Lead Inductance	Lead Count							
SOP/SSOP (Small Outline Package)									
		8	16	20	24	28	44	56	70
3.9 x 8.7mm	< 2nH			■					
3.9 x 9.9 mm	< 4nH					■			
4.0 x 5.1mm	< 2nH	■							
4.4 x 6.9 mm	< 3nH		■						
4.4 x 6.9 mm	< 3nH			■					
5.3 x 3.0 mm	< 3nH			■					
5.3 x 7.2 mm	< 3nH			■					
5.3 x 10.2 mm	< 4nH					■			
5.3 x 15.6 mm	< 5nH				■				
5.4 x 14.1 mm	< 5nH			■					
7.5 x 18.4 mm	< 8nH							■	
12.6 x 29.0mm	< 20nH						■		
12.7 x 29.0 mm	< 16nH								■
TSOP/TSSOP (Thin SOP)									
		8	28	32	44	48	54	56	66
4.4 x 3.0mm	< 3nH	■							
4.4 x 9.7 mm	< 3nH		■						
6.1 x9.7mm	< 3nH		■						
6.1 x 14.0 mm	< 6nH							■	
10.2 x 18.9 mm	< 8nH				■				
10.2 x 21.4 mm	< 7nH			■					
10.2 x 22.6 mm	< 7nH					■	■		■
12.0 x 20.0mm	< 6nH					■			
12.4 x 16.4 mm	< 7nH					■			
PSOP/PSSOP (Power SOP)									
		8	16	20					
3.9 x 9.9 mm	< 3nH		■						
6.1 x 7.64 mm	< 3nH	■							
7.6 x 12.8 mm	< 3nH			■					
11.0 x 15.9 mm	< 6nH		■						

Package	Lead Inductance	Lead Count									
QFP (Quad Flat Package)		44	48	64	80	100	128	160	208	240	256
7 x 7 mm	< 3nH		■								
10 x 10 mm	< 5nH	■	■								
12 x 12 mm	< 5nH				■						
14 x 14 mm	< 6nH			■		■					
14 x 20 mm	< 12nH			■	■	■	■				
24 x 24 mm	< 11nH							■			
28 x 28 mm	< 17nH							■	■		■
32 x 32 mm	< 15nH									■	
TQFP (Thin Quad Flat Package)		32	48	80	100	144	160	176	208		
7 x 7 mm	< 4nH	■	■								
12 x 12 mm	< 5nH			■							
14 x 14 mm	< 5nH				■						
14 x 20 mm	< 10nH				■						
20 x 20 mm	< 9nH					■					
24 x 24 mm	< 11nH						■	■			
28 x 28 mm	< 13nH								■		
PLCC (Plastic Leaded Chip Carrier)		44	84								
16.6 x 16.5mm	<5nH	■									
29.3 x 29.3 mm	< 13nH		■								

Package	Lead Inductance		Lead Count										
SBGA (Super BGA)													
	Lp/g	**Lsig**	256	304	352	432	560	600					
27 x 27 mm	< 3nH	< 7nH	■										
31 x 31 mm	< 3nH	< 8nH		■									
35 x 35 mm	< 3nH	< 8nH			■								
40 x 40 mm	< 3nH	< 9nH				■							
42.5 x 42.5 mm	< 3nH	< 9nH					■						
45 x 45 mm	< 3nH	< 9nH						■					
PBGA (Plastic BGA)													
	Lp/g	**Lsig**	119	121	169	204	208	217	225	249	256	272	300
14 x 22 mm	< 4nH	<9nH	■										
15 x 15 mm	< 4nH	< 13nH		■									
23 x 23 mm	< 4nH	< 18nH			■	■	■	■		■			
27 x 27 mm	< 4nH	< 21nH							■		■	■	■
31 x 31 mm	< 4nH	< 13nH											
35 x 35 mm	< 4nH	< 14nH											
PBGA (Plastic BGA)													
	Lp/g	**Lsig**	304	316	324	329	352	360	385	388	420	456	
14 x 22 mm	< 4nH	<10nH											
15 x 15 mm	< 4nH	< 13nH											
23 x 23 mm	< 4nH	< 18nH											
27 x 27 mm	< 4nH	< 21nH		■	■								
31 x 31 mm	< 4nH	< 13nH	■			■		■	■				
35 x 35 mm	< 4nH	< 14nH					■			■	■	■	

1.11 Power Dissipation

1.11.1 ESTIMATION OF POWER DISSIPATION IN CMOS CIRCUIT

CMOS circuits have been traditionally considered to consume low power since they draw very small amount of current in a steady state. However, the recent revolution in a CMOS technology that allows very high gate density has changed the way the power dissipation should be understood. The power dissipation in a CMOS circuit is affected by various factors such as the number of gates, the switching frequency, the loading on the output of a gate, and so on.

Power dissipation is important when designers decide the amount of necessary power supply current for the device to operate in safety. Propagation delays and reliability of the device also depend on power dissipation that determines the temperature at which the die operates. To obtain high speed and reliability, designers must estimate power dissipation of the device accurately and determine the appropriate environments including the package and system cooling methods.

This section describes the concepts of two types of power dissipation (static and dynamic) in a CMOS circuit, the method of calculating those in the Samsung STD90/MDL90 library, and finally their relationship with temperature.

1.11.2 STATIC (DC) POWER DISSIPATION

There are two types of static or DC current contributing to the total static power dissipation in CMOS circuits.

One is the leakage current of the gates resulted by a reverse bias between a well and a substrate region. There is no DC current path from power to ground in a CMOS because one of the transistor pair is always off, therefore, no static current except the leakage current flows through the internal gates of the device. The amount of this leakage current is, however, in the range of tens of nano amperes, which is negligible.

The other is DC current that flows through the input and output buffers when the circuit is interfaced with other devices, especially TTL. The current of pull-up/ pull-down transistor in the input buffers is about 35μA typically, which is also negligible. Therefore, only DC current that the output buffers source or sink has to be counted to estimate the total static power dissipation.

DC power dissipation of output and bi-directional buffers is determined by the following formula:

$$P_{DC\_OUTPUT}\,[mW] = \left(\sum_{k=1}^{n} (V_{OL(k)} \times I_{OL(k)} \times t_{L(k)}) + \sum_{k=1}^{n} ((V_{DD} - V_{OH(k)}) \times I_{OH(k)} \times t_{H(k)}) \right) / T$$

$$P_{DC\_BI}\,[mW] = \left(\sum_{k=1}^{n} (V_{OL(k)} \times I_{OL(k)} \times t_{L(k)}) + \sum_{k=1}^{n} ((V_{DD} - V_{OH(k)}) \times I_{OH(k)} \times t_{H(k)}) \right) \times S_{out} / T$$

where,

n = Number of output and bidirectional buffers

T = Total operation time in output mode

t_H = The sum of logic high state time

t_L = The sum of logic low state time

$t_L + t_H = T$ (Supposed that all output and bidirectional buffers have just logic high or low state)

Sout is the output mode ratio of bidirectional buffers (typically 0.5)

1.11.3 DYNAMIC (AC) POWER DISSIPATION

When a CMOS gate changes its state, it draws switching current as a result of charging or discharging a load capacitance, C_L. The energy associated with the switching current for a node capacitance, C_L, is

$C_L \times V_{DD}^2$

where V_{DD} is the power supply voltage.

In addition to the power dissipated by the load capacitance, CMOS circuits consume power due to the short-circuit current flowing through a temporary VDD-to-ground path during switching.

The dynamic power dissipation for an entire chip is much more complicated to estimate since it depends on the degree of switching activity of the circuit. Samsung has found that the degree of switching activity is 10% on the average and recommends this number to be used in estimating the total dynamic power dissipation.

1.11.4 POWER DISSIPATION IN STD90/MDL90

This section describes the equations on how to estimate the power dissipation in STD90/MDL90. As explained in the previous section, the total power dissipation (P_{TOTAL}) consists of static power dissipation (P_{DC}) and dynamic power dissipation (P_{AC}).

$$P_{TOTAL} = P_{DC} + P_{AC}$$

Since only output buffers contribute to the static power dissipation,

$$P_{DC} = P_{DC\_OUTPUT}$$

where P_{DC_OUTPUT} is the static power dissipated when output buffers source or sink.

The dynamic power dissipation is caused by three components: input buffers (P_{AC_INPUT}), output buffers (P_{AC_OUTPUT}), bidirectional buffers (P_{AC_BI}), and internal cells ($P_{AC\_INTERNAL}$).

$$P_{AC} = P_{AC\_INPUT} + P_{AC\_OUTPUT} + P_{AC\_BI} + P_{AC\_INTERNAL}$$

Each term mentioned above is characterized by the following equations:

$$P_{AC\_INPUT}\,[mW] = 10.89 \times \sum_{i}^{N\_input} (0.001 \times Si \times Fi \times C_{i\_inload})$$

$$P_{AC\_OUTPUT}\,[mW] = 10.89 \times \sum_{i}^{N\_output} (0.001 \times Si \times Fi \times C_{i\_outload})$$

$$P_{AC\_BI}\,[mW] = 10.89 \times \sum_{i}^{N\_bi} (0.001 \times Si \times Fi \times C_{i\_inload}) \times (1 - S_{out}) + 10.89 \times \sum_{i}^{N\_bi} (0.001 \times Si \times Fi \times C_{i\_outload}) \times S_{out}$$

$$P_{AC\_INTERNAL}\,[mW] = 0.001 \times (0.8433 \times S + 0.0485) \times G \times F + \sum_{i}^{N\_macro} (0.001 \times Pi \times Fi)$$

where

N_input is the number of input buffers used,
N_output is the number of output buffers used,
N_bi is the number of bidirectional buffers used,
N_macro is the number of macro cells used,
G is the size of the design in gate count,
F is the operating frequency in MHz,
S is the estimated degree of switching activity (typically 0.1),
Sout is the output mode ratio of bidirectional buffers (typically 0.5),
C is the load capacitance in pF.
P is the characterized power for the i-th hard macro block (μW/MHz)

1.11.5 TEMPERATURE AND POWER DISSIPATION

The total power dissipation, P_{TOTAL} can be used to find out the device temperature by the following equation:

$$\theta_{JA} = (T_J - T_A) / P_{TOTAL}$$

where

θ_{JA} is the thermal impedance,
T_J is the junction temperature of the device,
T_A is the ambient temperature.

Thermal impedances of the Samsung packages are given in the following table. The junction temperature, obtained by multiplying P_{TOTAL} by the appropriate θ_{JA} and adding T_A, determines the derating factor for the propagation delays and also indicates the reliability measures. Hence, designers can achieve the desired derating factor and reliability targets by choosing appropriate packages and system cooling methods.

Table 1-10. Thermal Impedances of Samsung Plastic Packages

	SOP/TSOP								
Pin Number	**20**	**24**	**28**	**32**	**44**	**50**	**54**	**62**	**66**
θ_{JA}[°C/W]	63	58	41-44	46-56	44-71	39-59	34-56	27-33	34-46

	QFP									
Pin Number	**44**	**48**	**80**	**100**	**120**	**128**	**160**	**208**	**240**	**256**
θ_{JA}[°C/W]	51-62	43-56	43-74	27-61	33-47	43-51	29-51	22-43	28-47	29-42

	TQFP/LQFP							
Pin Number	**32**	**64**	**100**	**144**	**160**	**176**	**208**	**256**
θ_{JA}[°C/W]	68-70	47	37-70	38	35-62	31-34	37-56	30-42

	PBGA			
Pin Number	**272**	**388**	**356 (TEPBGA)**	**452 (TEPBGA)**
θ_{JA}[°C/W]	19-22	16-19	16	14

	SBGA				
Pin Number	**256**	**304**	**352**	**432**	**600**
θ_{JA}[°C/W]	14.1	13.1	11.7	10.2	8.3

1.12 V_{DD}/V_{SS} Rules And Guidelines

There are three of VDD and VSS in STD90, providing power with internal and I/O area.

- Core logic
  – VDD3I, VSSI
- Pre-drive (I/O area)
  – VDD3P, VSSP
- Output-drive (I/O area)
  – VDD3O, VSSO

The number of VDD and VSS pads required for a specific design depends on the following factors:

- Number of input and output buffers
- Number of simultaneous switching outputs
- Number of used gates and simultaneous switching gates
- Operating frequency.

1.12.1 BASIC PLACEMENT GUIDELINES

The purpose of these guidelines is to minimize IR drop and noise for reliable device operations.

- Core logic and pre-driver V_{DD}/V_{SS} pads should be evenly distributed on all sides of the chip.
- If you have core block demanding high power (compiled memory, analog), extra power pads should be placed on that side.
- Power pads for SSO group should be evenly distributed in the SSO group.
- Do not place the quiet signal (analog, reference) or analog power (VDDA/VSSA) or bi-directional buffer next to a SSO group.
- The opposite types of power pads (V_{DD}/V_{SS}) should be placed as close as possible.
- If it is possible, do not place power pads (V_{DD}/V_{SS}) at the corner of the chip.

1.12.2 VDD3I/VSSI PAD ALLOCATION GUIDELINES

The purpose of these guidelines is to ensure that minimum number of core logic power pad pairs meeting the ElectroMigration current limit are used. The number of VDD3I/VSSI pads required for a specific design is determined by the function of the operating frequency of a chip.

- VDD3I bus width and the number of pads are equal to those of VSSI
- VDD3I/VSSI buses and pads should be distributed evenly in the core and on each side of the chip.
- The total number of core logic VDD3I pads is equal to that of VSSI pads.

The number of VDD3I/VSSI pad pairs required for a design can be calculated from the following expression:

The number of VDD3I/VSSI pad pairs =

$$\left\| \left[0.001 \times (0.2555 \times S + 0.0147) \times G \times F + \sum_{i}^{N\_macro} (Pi \times Fi) \right] / I_{em} \right\| round-up$$

where,

G = The core (excluding hard macro blocks) size in the gate counts
S = The switching ratio (typically = 0.1)
F = Operating frequency (MHz)
Pi = Characterized current for the i-th hard macro block (mA/MHz)
Fi = Operating frequency for the i-th hard macro block (MHz)
Iem = Current limit per VDD/VSS pad pairs based on ElectroMigration rule (100mA)

For reliable device operation and minimize IR voltage drop, minimum number of VDD3I/VSSI power pad pairs is 4.

Extra power may be needed for the demanding high power macro blocks (SRAM, analog block...).

1.13.3 VDD3P/VSSP ALLOCATION GUIDELINES.

These guidelines ensure that an adequate input threshold voltage margin is maintained during a switching.

- The number of VDD3P/VSSP pads required for a design can be calculated from the following expressions:

$$Number\_of\_VDD3P/VSSP\_pad\text{-}pairs = \left\| \frac{I_{eq\_p}}{I_{em}} \right\| round-up$$

In above expression, Ieq_p = ∑(Average current of input/output buffers and bi-direction pre-drivers at maximum operational I/O frequency.) [mA] (Refer Table 1-11)

$$I_{eq\_p} = \sum_{i}^{N\_input} \left(I_{eq\_p\_in} \times \frac{F_i}{100} \right) + \sum_{j}^{N\_output} \left(I_{j\_eq\_p\_out} \times \frac{F_j}{100} \right) + \sum_{k}^{N\_bi} \left[\left(I_{k\_eq\_p\_in} \times \frac{F_k}{100} \right) (1 - S_{out}) + \left(I_{k\_eq\_p\_out} \times \frac{F_k}{100} \right) \times S_{out} \right]$$

where

N_input is the number of input buffers used,
N_output is the number of output buffers used,
N_bi is the number of bidirectional buffers used,
F is the operating frequency in MHz,
S_{out} is the output mode ratio of bidirectional buffers (typically 0.5),
I_{em} = Current limit per VDD/VSS pad pairs based on ElectroMigration rule. (100mA)

Table 1-11(a). Ieq_p (at F = 100MHz) for Each Type of Input Buffer

Input Buffer Type	CMOS	CMOS Schmitt
Ieq_p_in (mA)	0.6	0.7

Table 1-11(b). Ieq_p (at F = 100MHz) for Each Type of Output Buffer

Output Buffer Type	B1-8 (T1 – 8)	B12-24 (T12–24)	B4-24 (T4–24) Slew-Rate
Ieq_p_out (mA)	0.5	0.8	0.8

NOTE: T1 means 1mA output driver cells, and T24 means 24mA output driver cells.

For reliable device operation and minimizing IR voltage drop, minimum number of VDD3P/VSSP power pad pairs is 4.

1.12.4 VDD3O/VSSO ALLOCATION GUIDE

SSO (Simultaneous Switching Output) current induced in power and ground inductance can cause system failure because of voltage fluctuations. For the calculation of output driver power and pad numbers, we consider the SSO noise as well as current limit based on ElectroMigration. We may define SSO as output are considered to be simultaneous in 1ns window such as bus type buffers.

The number of VDD3O/VSSO pads required for a device can be calculated from the following expression.

* In case of heavy load, high frequency and low package inductance, the number of power pads for SSO block could be determined by electromigration rule rather than limit of SSO noise. So the number of power pads for SSO block should be determined as the worse one of the power pad number under the limit of SSO noise and that under the limit of electromigration rule.

1) Number of power pads for SSO block under the limit of SSO noise

- Calculating the number of power pad for each SSO group from the following expressions:

$$NVDDO_{each\_SSO} = \frac{number\_of\_SSO}{NBvdd} \times L_{pg} \times \frac{1}{D_{SSO\_mode}}$$

$$NVSSO_{each\_SSO} = \frac{number\_of\_SSO}{NBvss} \times L_{pg} \times \frac{1}{D_{SSO\_mode}}$$

In above formula,

NVDDOeach_sso = Number of VDD3O pad required for each SSO group

NVSSOeach_sso = Number of VSSO pad required for each SSO group

NBvdd=Number of buffers per VDD3O power pad with 1nH lead inductance (Refer Table 1-13.)

NBvss = Number of buffers per VSSO ground pas with 1nH lead inductance

L_{pg} = Package lead frame inductance (Refer 1.10 Package Capability by Lead Count)

$Dsso\_mode = D_{L\_mode} \times D_{P\_mode} \times D_{V\_mode} \times D_{T\_mode} \times D_{C\_mode}$ (Refer Table 1-12.)

D_{L_mode} = Lead inductance derating factor

D_{P_mode} = Process derating factor

D_{V_mode} = Voltage derating factor

D_{T_mode} = Temperature derating factor

D_{C_mode} = Cload derating factor (mode is either vdd or vss.)

Table 1-12. Derating Equation

Item	Mode	Equation	Range
Package Lead	D_{L_vdd}	0.0052 x Lpg + 0.9794 – 0.0052 x Lpg + 1.0825	3nH ≤ Lpg ≤ 15nH 10nH ≤ Lpg ≤ 15nH
	D_{L_vss}	– 0.0094 x Lpg + 1.0377 0.0377 x Lpg + 0.5660	3nH ≤ Lpg ≤ 10nH 10nH < Lpg ≤ 15nH
Process	D_{P_vdd}	1.0000 1.1134 1.2887	best typical worst
	D_{P_vss}	1.0000 1.3208 1.5094	best typical worst
Voltage	D_{V_vdd}	– 0.4467 x voltage + 2.5670 – 0.3093 x voltage + 2.1134	3.0 ≤ voltage ≤ 3.3 3.3 < voltage ≤ 3.6
	D_{V_vss}	– 0.4403 x voltage + 2.5283 – 0.2516 x voltage + 1.9057	3.0 ≤ voltage ≤ 3.3 3.3 < voltage < 3.6
Temperature	D_{T_vdd}	0.0008 x temperature + 1.0000 0.0006 x temperature + 1.0066	-40 ≤ temperature ≤ 25 25 < temperature ≤ 125
	D_{T_vss}	0.0045 x temperature + 1.0000 0.0034 x temperature + 1.0274	-40 ≤ temperature ≤ 25 25 < temperature ≤ 125
Cload	D_{C_vdd}	0.0155 x Cload + 0.5361 0.0180 x Cload + 0.4588	10pF ≤ Cload ≤ 30pF 30pF < Cload ≤ 50pF
	D_{C_vss}	0.0255 x Cload + 0.2358 0.0142 x Cload + 0.5755	10pF ≤ Cload ≤ 30pF 30pF < Cload ≤ 50pF

Table 1-13. NBvdd/NBvss Parameter (Process = best, Volt = 3.6V Temp. = 0˚C, Llead = 1nH)

Buffer Type	Voltage Type	Normal		Slew-Rate Medium (sm)		Slew-Rate High (sh)	
		NBvdd	NBvss	NBvdd	NBvss	NBvdd	NBvss
pob1 (pot1)	3.3V Interface	470	300	–	–	–	–
pob2 (pot2)		375	210	–	–	–	–
pob4 (pot4)		194	106	355	275	–	–
pob8 (pot8)		128	56	154	102	–	–
pob12 (pot12)		96	46	136	64	300	65
pob16 (pot16)		82	42	120	54	285	55
pob20 (pot20)		74	38	112	50	270	50
pob24 (pot24)		74	36	106	48	255	50
ptot1	5V Tolerant	600	330	–	–	–	
ptot2		390	165	–	–		
ptot4		200	92	425	295		
ptot6		160	66	345	250		

NOTE: pob1 means 1mA output driver cells, and pob24 means 24mA output driver cells.

- Calculating the number of required power pad for total SSO from the following expression:

  NVDDO1sso = ∑NVDDOeach_sso

  NVSSO1sso = ∑NVSSOeach_sso

  When there are SSO blocks which are not switching simultaneously with the others, only maximum value of NVDDO_each_sso/NVSSO_each_sso among those SSO block should be accounted.

  In above formula,

  NVDDOsso = Number of VDD3O pad per total SSO buffers

  NVSSOsso = Number of VSSO pad per total SSO buffers

2) Number of power pads for SSO block under the limit of electromigration rule

- Calculating the following expression:

$$NVDDO2_{SSO}/NVSSO2_{SSO} = \frac{I_{eq\_o}}{I_{em}}$$

$$I_{eq\_o} = \sum_{i}^{N\_SSO\_output} (0.001 \times C_{i\_outload} \times V_i \times F_i \times S_i) + \sum_{j}^{N\_SSO\_bi} (0.001 \times C_{j\_outload} \times V_j \times F_j \times S_j \times S_{j\_out})$$

where

N_SSO_output is the number of simultaneous switching output buffers used,
N_SSO_bi is the number of simultaneous switching bidirectional buffers used,
Coutload = Output load capacitance [pF]
V = Operating voltage [V]
F = Maximum I/O operating frequency [MHz]
S = Switching ratio (typically 0.5)
S_{out} = Output mode ratio of bidirectional buffers, (typically 0.5).
I_{em} = Current limit per VDD/VSS pad paris based on electromigration rule.(100mA)

3) Number of power pads for non-SSO block

- Calculating the following expression:

$$NVDDO_{non\_SSO}/NVSSO_{non\_SSO} = \frac{I_{eq\_o}}{I_{em}}$$

$$I_{eq\_o} = \sum_{i}^{N\_non\_SSO\_output} (0.001 \times C_{i\_outload} \times V_i \times F_i \times S_i) + \sum_{j}^{N\_non\_SSO\_bi} (0.001 \times C_{j\_outload} \times V_j \times F_j \times S_j \times S_{j\_out})$$

where

N_non_SSO_output is the number of simultaneous switching output buffers used,
N_non_SSO_bi is the number of simultaneous switching bidirectional buffers used,
Coutload = Output load capacitance [pF]
V = Operating voltage [V]
F = Maximum I/O operating frequency [MHz]
S = Switching ratio (typically 0.5)
S_{out} = Output mode ratio of bidirectional buffers, (typically 0.5).
I_{em} = Current limit per VDD/VSS pad paris based on electromigration rule.(100mA)

4) Total number of power pads for VDD3O/VSSO

- Calculating the following expressions:

$$\text{Number of VDD3O} = \lVert \max(NVDDO1_{SSO}, NVDDO2_{SSO}) + NVDDO_{non\_SSO} \rVert \text{ round-up}$$

$$\text{Number of VSSO} = \lVert \max(NVSSO1_{SSO}, NVSSO2_{SSO}) + NVSSO_{non\_SSO} \rVert \text{ round-up}$$

When open drain type buffers are used, you can consider using VSSO pads since they have current sink only.

1.13 Crystal Oscillator Consideration

1.13.1 OVERVIEW

STD90/MDL90 contains a circuit commonly referred to as an “on-chip oscillator.” The on-chip circuit itself is not an oscillator but an amplifier which is suitable for being used as the amplifier part of a feedback oscillator. With proper selection of off-chip components, this oscillator circuit performs better than any other types of clock oscillators.

It is very important to select suitable off-chip components to work with the on-chip oscillator circuitry. It should be noted, however, that Samsung cannot assume the responsibility of writing specifications for the off-chip components of the complete oscillator circuit, nor of guaranteeing the performance of the finished design in production, any more than a transistor manufacturer, whose data sheets show a number of suggested amplifier circuits, can assume responsibility for the operation, in production, of any of them.

We are often asked why we don’t publish a list of required crystal or ceramic resonator specifications, and recommend values for the other off-chip components. This has been done in the past, but sometimes with consequences that were not intended.

Suppose we suggest a maximum crystal resistance of 30 ohms for some given frequency. Then your crystal supplier tells you the 30 ohm crystals are going to cost twice as much as 50 ohm crystals. Fearing that Samsung will not “guarantee operation” with 50 ohm crystals, you order the expensive ones.

In fact, Samsung guarantees only what is embodied within an Samsung product. Besides, there is no reason why 50 ohm crystals couldn’t be used, if the other off-chip components are suitably adjusted.

Should we recommend values for the other off-chip components? Should we do for 50 ohm crystals or 30 ohm crystals? With respect to what should we optimize their selection? Should we minimize start-up time or maximize frequency stability?

In many applications, neither start-up time nor frequency stability is particularly critical, and our “recommendations” are only restricting your system to unnecessary tolerances. It all depends on the application.

1.13.2 OSCILLATOR DESIGN CONSIDERATIONS

ASIC designers have a number of options for clocking the system. The main decision is whether to use the “on-chip” oscillator or an external oscillator. If the choice is to use the on-chip oscillator, what kinds of external components are to use an external oscillator, what type of oscillator would it be?

The decisions have to be based on both economic and technical requirements. In this section we will discuss some of the factors that should be considered.

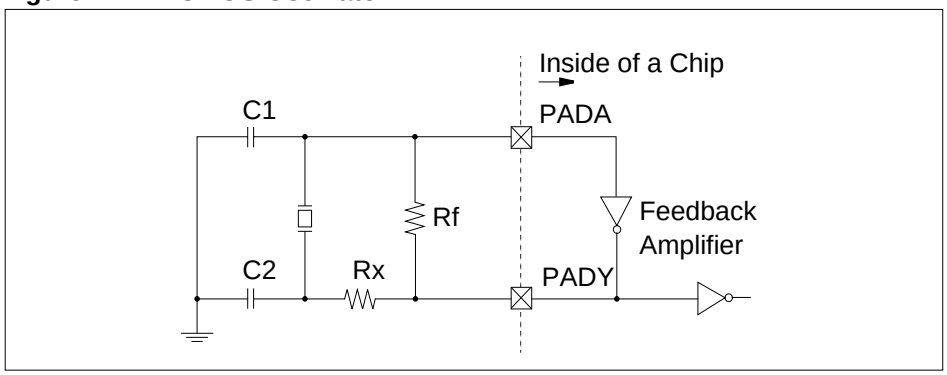
1.13.2.1 On-Chip Oscillator

In most cases, the on-chip amplifier with the appropriate external components provides the most economical solution to the clocking problem. Exceptions may arise in server environments when frequency tolerances are tighter than about 0.01%.

The external components that commonly used for CMOS gate oscillator are a

positive reactance (normal crystal oscillator), two capacitors, C1 and C2, and two resistor Rf and Rx as shown in the figure below.

Figure 1-14. CMOS Oscillator



1.13.2.2 Crystal Specifications

Specifications for an appropriate crystal are not very critical, unless the frequency is. Any fundamental-mode crystal of medium or better quality can be used.

We are often asked what maximum crystal resistance should be specified. The best answer to that question is the lower the better, but use what is available.

The crystal resistance will have some effect on start-up time and steady-state amplitude, but not so much that it can't be compensated for by appropriate selection of the capacitances, C1 and C2.

Similar questions are asked about specifications of load capacitance and shunt capacitance. The best advice we can give is to understand what these parameters mean and how they affect the operation of the circuit (that being the purpose of this application note), and then to decide for yourself if such specifications are meaningful in your frequency tolerances are tighter than about 0.1%.

Part of the problem is that crystal manufacturers are accustomed to talking "ppm" tolerances with radio engineers and simply won't take your order until you've filled out their list of frequency tolerance requirements, both for yourself and to the crystal manufacturer. Don't pay for 0.003% crystals if your actual frequency tolerance is 1%.

1.13.2.3 Oscillation Frequency

The oscillation frequency is determined 99.5% by the crystal and up to about 0.5% by the circuit external to the crystal.

The on-chip amplifier has little effect on the frequency, which is as it should be, since the amplifier parameterizes temperature and process dependent.

The influence of the on-chip amplifier on the frequency is by means of its input and output (pin-to-ground) capacitances, which parallel C1 and C2, and the PADA-to-PADY (pin-to-pin) capacitance, which parallels the crystal. The input and pin-to-pin capacitances are about 7pF each.

Internal phase deviations capacitance of 25 to 30pF. These deviations from the ideal have less effect in the positive reactance oscillator (with the inverting amplifier) than in a comparable series resonant oscillator (with the non-inverting amplifier) for two reasons: first, the effect of the output capacitor; second, the positive reactance oscillator is less sensitive, frequency-wise, to such phase errors.

1.13.2.4 C1 / C2 Selection

Optimal values for the capacitors C1 and C2 depend on whether a quartz crystal or ceramic resonator is being used, and also on application-specific requirements on start-up time and frequency tolerance.

Start-up time is sometimes more critical in microcontroller systems than frequency stability, because of various reset and initialization requirements.

Less commonly, accuracy of the oscillator frequency is also critical, for example, when the oscillator is being used as a time base. As a general rule, fast start-up and stable frequency tend to pull the oscillator design in opposite directions.

Considerations of both start-up time and frequency stability over temperature suggest that C1 and C2 should be about equal and at least 20pF. (But they don't have to be either.)

Increasing the value of these capacitances above some 40 or 50pF improves frequency stability. It also tends to increase the start-up time. These is a maximum value (several hundred pH, depending on the value of R1 of the quartz or ceramic resonator) above which the oscillator won't start up at all.

If the on-chip amplifier is a simple inverter, the user can select values for C1 and C2 between some 20 and 100pF, depending on whether start-up time or frequency stability is the more critical parameter in a specific application.

1.13.2.5 Rf / Rx Selection

A CMOS inverter might work better in this application since a large Rf (1mega-ohm) can be used to hold the inverter in its linear region.

Logic gates tend to have a fairly low output resistance, which testabilizes the oscillator. For that reason a resistor Rx (several k-ohm) is often added to the feedback network, as shown in Figure 1-14.

At higher frequencies a 20 or 30pF capacitor is sometimes used in the Rx position, to compensate for some of the internal propagation delay.

1.13.2.6 Pin Capacitance

Internal pin-to-ground and pin-to-pin capacitances, and PADA and PADY have some effect on the oscillator. These capacitances are normally taken to be in the range of 5 to 10pF, but they are extremely difficult to evaluate. Any measurement of one such capacitance necessarily include effects from the others.

One advantage of the positive reactance oscillator is that the pin-to ground cap. is paralleled by an external bulk capacitance, so a precise determination of their value is unnecessary.

We would suggest that there is little justification for more precision than to assign them a value of 7pF (PADA-to-ground and PADA-to-PADY). This value is probably not in error by more than 3 or 4pF. The PADY-to-ground cap. is not entirely a “pin capacitance”, but more like an “equivalent output capacitance” of some 25 to 30pF, having to include the effect of internal phase delays. This value varies to some extent with temperature, process, and frequency.

1.13.2.7 Placement of Components

Noise glitches arising at PADA or PADY pins at the wrong time can cause a miscount in the internal clock-generating circuitry. These kinds of glitches can be produced through capacitive coupling between the oscillator components and PCB traces carrying digital signals with fast rise and fall times.

For this reason, the oscillator components should be mounted close to the chip and have short, direct traces to the PADA, PADY, and V_{SS} pins.

If possible, use dedicated V_{SS} and V_{DD} pin for only crystal feedback amplifier.

1.13.3 TROUBLESHOOTING OSCILLATOR PROBLEMS

The first thing to consider in case of difficulty is that there may be significant differences in stray caps between the test jig and the actual application, particularly if the actual application is on a multi-layer board.

Noise glitches, that are not present in the test jig but are in the application board, are another possibility. Capacitive coupling between the oscillator circuitry and other signal has already been mentioned as a source of miscounts in the internal clocking circuitry. Inductive coupling is also doubtful, if there is strong current nearby. These problems are a function of the PCB layout.

Surrounding oscillator components with “quit” traces (for example, VCC and ground) will alleviate capacitive coupling to signals having fast transition time. To minimize inductive coupling, the PCB layout should minimize the areas of the loops formed by oscillator components.

The loops demanding to be checked are as follows:

PADA through the resonator to PADY;
PADA through C1 to the V_{SS} pin;
PADY through C2 to the V_{SS} pin.

It is not unusual to find that the ground ends of C1 and C2 eventually connect up to the V_{SS} pin only after looping around the farthest ends of the board. Not good.

Finally, it should not be overlooked that software problems sometimes imitate the symptoms of a slow-starting oscillator or incorrect frequency. Never underestimate the perversity of a software problem.

Electrical Characteristics

2

Contents

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3 ± 0.3V, T_A = 0 to 70°C (In case of normal I/O)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IH}	High level input voltage					V
	LVCMOS interface		2.0			
V_{IL}	Low level input voltage					V
	LVCMOS interface				0.8	
VT	Switching threshold	LVCMOS		1.4		V
VT+	Schmitt trigger, positive-going threshold	LVCMOS			2.0	
VT-	Schmitt trigger, negative-going threshold	LVCMOS	0.8			
I_{IH}	High level input current					µA
	Input buffer	$V_{IN} = V_{DD}$	–10		10	
	Input buffer with pull-down		10	30	60	
I_{IL}	Low level input current					µA
	Input buffer	$V_{IN} = V_{SS}$	–10		10	
	Input buffer with pull-up		–60	–30	–10	
V_{OH}	High level output voltage					V
	Type B1 to B24[Note2]	I_{OH} = –1µA	V_{DD} – 0.05			
	Type B1	I_{OH} = –1mA	2.4			
	Type B2	I_{OH} = –2mA				
	Type B4	I_{OH} = –4mA				
	Type B8	I_{OH} = –8mA				
	Type B12	I_{OH} = –12mA				
	Type B16	I_{OH} = –16mA				
	Type B20	I_{OH} = –20mA				
	Type B24	I_{OH} = –24mA				
V_{OL}	Low level output voltage					V
	Type B1 to B24[Note2]	I_{OL} = 1µA			0.05	
	Type B1	I_{OL} = 1mA			0.4	
	Type B2	I_{OL} = 2mA				
	Type B4	I_{OL} = 4mA				
	Type B8	I_{OL} = 8mA				
	Type B12	I_{OL} = 12mA				
	Type B16	I_{OL} = 16mA				
	Type B20	I_{OL} = 20mA				
	Type B24	I_{OL} = 24mA				
I_{OZ}	Tri-state output leakage current	V_{OUT} =V_{SS} or V_{DD}	–10		10	µA
I_{OS}	Output short circuit current	V_{DD} = 3.6V, V_O = V_{DD}			210	mA
		V_{DD} = 3.6V, V_O = V_{SS}	–170			
I_{DD}	Quiescent supply current	V_{IN} = V_{SS} or V_{DD}			100[Note3]	µA
C_{IN}	Input capacitance[Note4]	Any Input and Bidirectional Buffers			4	pF
C_{OUT}	Output capacitance[Note4]	Any Output Buffer			4	pF

V_{DD} = 3.3 ± 0.3V, V_{EXT} = 5 ± 0.25V, T_A = 0 to 70°C (In case of 5V-tolerant I/O)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IH}[Note1]	High level input voltage					V
	LVCMOS interface		2.0			
V_{IL}[Note1]	Low level input voltage					V
	LVCMOS interface				0.8	
VT	Switching threshold	LVCMOS		1.4		V
VT+	Schmitt trigger, positive-going threshold	LVCMOS			2.0	
VT-	Schmitt trigger, negative-going threshold	LVCMOS	0.8			
I_{IH}	High level input current					µA
	Input buffer	$V_{IN} = V_{DD}$	–10		10	
	Input buffer with pull-down		10	30	60	
I_{IL}	Low level input current					µA
	Input buffer	$V_{IN} = V_{SS}$	–10		10	
	Input buffer with pull-up		–60	–30	–10	
V_{OH}	High level output voltage					V
	Type B1 to B16[Note2]	I_{OH} = –1µA	V_{DD} – 0.05			
	Type B1	I_{OH} = –1mA	2.4			
	Type B2	I_{OH} = –2mA				
	Type B4	I_{OH} = –4mA				
	Type B6	I_{OH} = –6mA				
V_{OL}	Low level output voltage					V
	Type B1 to B16[Note2]	I_{OL} = 1µA			0.05	
	Type B1	I_{OL} = 1mA			0.4	
	Type B2	I_{OL} = 2mA				
	Type B4	I_{OL} = 4mA				
	Type B6	I_{OL} = 6mA				
I_{OZ}	Tri-state output leakage current	V_{OUT} =V_{SS} or V_{EXT}	–10		10	µA
I_{OS}	Output short circuit current	V_{DD} = 3.6V, V_O = V_{DD}			55	mA
		V_{DD} = 3.6V, V_O = V_{SS}	–55			
I_{DD}	Quiescent supply current	V_{IN} = V_{SS} or V_{DD}			100[Note3]	µA
C_{IN}	Input capacitance[Note4]	Any input and bidirectional buffers			4	pF
C_{OUT}	Output capacitance[Note4]	Any output buffer			4	pF

NOTES:

1. All 5V-tolerant input have less than 0.2V hysteresis.
2. Type B1 means 1mA output driver cells, and type B6/B24 means 6mA/24mA output driver cells.
3. This value depends on the customer design.
4. This value excludes package parasitics.

V_{DD} = 3V ± 10%, T_A = 0 to 70°C

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IH}	High level input voltage					V
	CMOS interface		1.8			
V_{IL}	Low level input voltage					V
	CMOS interface				0.8	
VT	Switching threshold	CMOS		1.4		V
VT+	Schmitt trigger, positive-going threshold	CMOS		1.7	1.9	
VT-	Schmitt trigger, negative-going threshold	CMOS	0.8	1.0		
I_{IH}	High level input current					µA
	Input buffer	$V_{IN} = V_{DD}$	–10		10	
	Input buffer with pull-down		10	30	60	
I_{IL}	Low level input current					µA
	Input buffer	$V_{IN} = V_{SS}$	–10		10	
	Input buffer with pull-up		–60	–30	–10	
V_{OH}	High level output voltage					V
	Type B1 to B24[Note1]	I_{OH} = –1µA	V_{DD} – 0.05			
	Type B1	I_{OH} = –1mA	2.4			
	Type B2	I_{OH} = –2mA				
	Type B4	I_{OH} = –4mA				
	Type B8	I_{OH} = –8mA				
	Type B12	I_{OH} = –12mA				
	Type B16	I_{OH} = –16mA				
	Type B20	I_{OH} = –20mA				
	Type B24	I_{OH} = –24mA				
V_{OL}	Low level output voltage					V
	Type B1 to B24[Note1]	I_{OL} = 1µA			0.05	
	Type B1	I_{OL} = 1mA			0.4	
	Type B2	I_{OL} = 2mA				
	Type B4	I_{OL} = 4mA				
	Type B8	I_{OL} = 8mA				
	Type B12	I_{OL} = 12mA				
	Type B16	I_{OL} = 16mA				
	Type B20	I_{OL} = 20mA				
	Type B24	I_{OL} = 24mA				
I_{OZ}	Tri-state output leakage current	V_{OUT} =V_{SS} or V_{VDD}	– 5		5	µA
I_{OS}	Output short circuit current	V_{DD} = 3.3V, V_O = V_{DD}			170	mA
		V_{DD} = 3.3V, V_O = V_{SS}	–150			
I_{DD}	Quiescent supply current	V_{IN} = V_{SS} or V_{DD}			100[Note2]	µA
C_{IN}	Input capacitance[Note3]	Any input and bidirectional buffers			4	pF
C_{OUT}	Output capacitance[Note3]	Any output buffer			4	pF

NOTES:

1. Type B1 means 1mA output driver cells, and type B6/B24 means 6/24mA output driver cells.
2. This value depends on the customer design.
3. This value excludes package parasitics.

Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
V_{DD}	DC supply voltage	– 0.3 to 3.8		V
V_{IN}	DC input voltage	3.3V I/O	–0.3 to V_{DD} +0.3	V
		5V- tolerant	–0.3 to 5.5	
I_{IN}	DC input current	±10		mA
T_{STG}	Storage temperature	– 40 to 125		°C

Recommended Operating Conditions

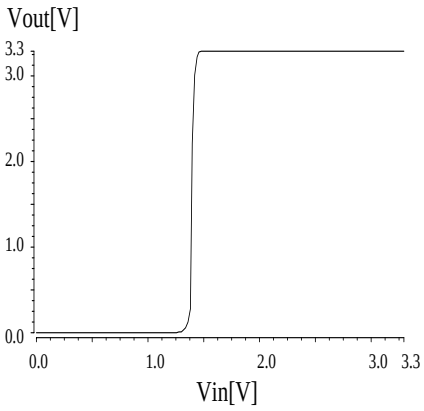
Symbol	Parameter		Rating	Unit
V_{DD}	DC supply voltage	3.3V	3.0 to 3.6	V
		3V	2.7 to 3.3	V
T_A	Commercial temperature range		0 to 70	°C
	Industrial temperature range		– 40 to 85	

NOTE: All electrical characteristics are applied in digital cell library without analog core.

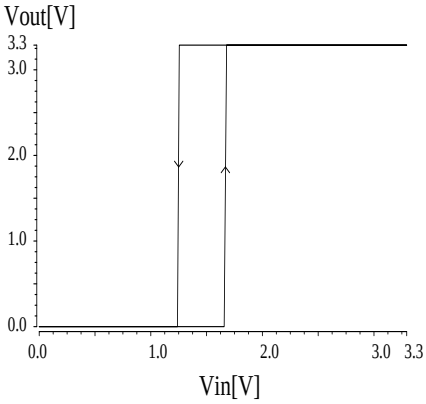
INPUT BUFFER DC CURVES

Input Buffer Transfer Curves

[V_{DD} = 3.3V, T_A = 25°C, Typical Process]



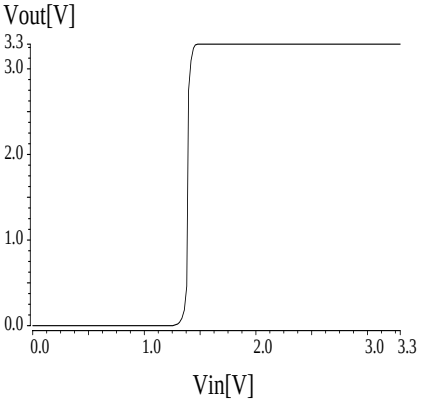
CMOS



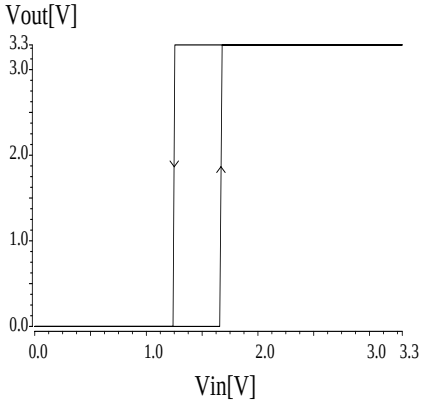
CMOS Schmitt Trigger

Input Clock Drivers Transfer Curves

[V_{DD} = 3.3V, T_A = 25°C, Typical Process]



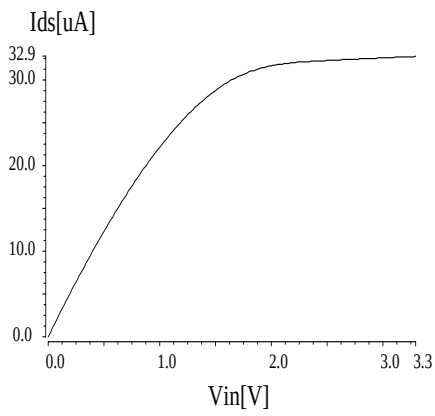
CMOS



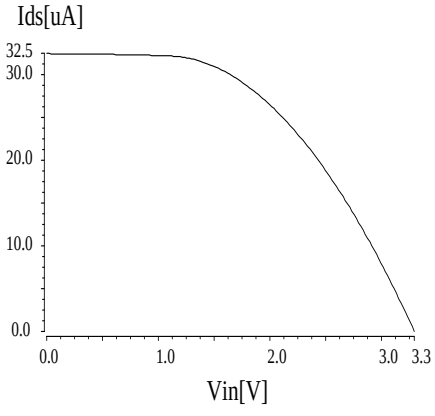
CMOS Schmitt Trigger

Input Buffer Pull-Down/Pull-Up Characteristics

[V_{DD} = 3.3V, T_A = 25°C, Typical Process]



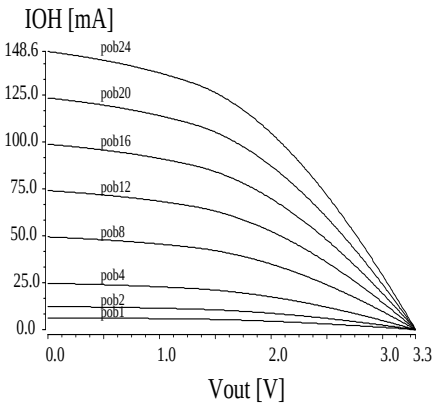
Pull-Down



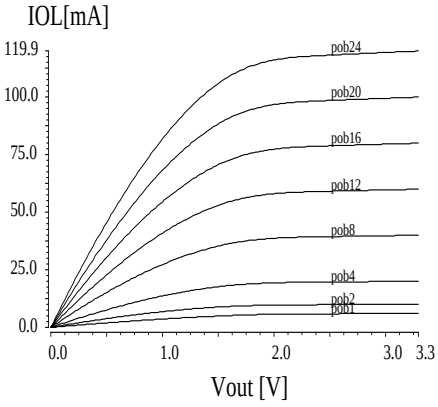
Pull-Up

OUTPUT DRIVE CAPABILITIES

IV Characteristics [V_{DD} = 3.3V, T_A = 25°C, Typical Process]



P-TR Characteristics



N-TR Characteristics

Internal Macrocells

3

Contents

OVERVIEW

The third chapter contains data sheets of logic cells, flip-flops, latches, bus holder, internal clock drivers, decoders, adders and multiplexers.

The electrical characteristics of each cell follow its basic cell data.

Summary tables in the following pages list the whole STD90/MDL90 internal macrocells by the type and show their reference page numbers for your convenience. Moreover, you can find the more detailed description tables on the leading pages of each category.

SUMMARY TABLES

Logic Cells

Flip-Flops

Cell Type	Cell Name	Page
D Flip-Flop with Negative Edge Trigger	FD5/FD5D2	3-318
	FD5S/FD5SD2	3-320
	FD6/FD6D2	3-322
	FD6S/FD6SD2	3-324
	FD7/FD7D2	3-327
	FD7S/FD7SD2	3-329
	FD8/FD8D2	3-332
	FD8S/FD8SD2	3-336
D Flip-Flop with Synchronous Clear	FDS2/FDS2D2	3-340
	FDS2CS/FDS2CSD2	3-342
	FDS2S/FDS2SD2	3-345
	FDS3/FDS3D2	3-347
	FDS3CS/FDS3CSD2	3-349
	FDS3S/FDS3SD2	3-352
JK Flip-Flop	FJ1/FJ1D2	3-355
	FJ1S/FJ1SD2	3-357
	FJ2/FJ2D2	3-359
	FJ2S/FJ2SD2	3-361
	FJ4/FJ4D2	3-364
	FJ4S/FJ4SD2	3-367
Toggle Flip-Flop	FT2/FT2D2	3-370

Latches

Cell Type	Cell Name	Page
D Latch with Active High	LD1/LD1D2	3-373
	LD1A/LD1D2A	3-375
	LD1Q/LD1QD2	3-377
	LD2/LD2D2	3-379
	LD2Q/LD2QD2	3-382
	LD3/LD3D2	3-384
	LD4/LD4D2	3-387
D Latch with Active Low	LD5/LD5D2	3-390
	LD5Q/LD5QD2	3-392
	LD5S/LD5SD2	3-394
	LD6/LD6D2	3-397
	LD6Q/LD6QD2	3-400
	LD7/LD7D2	3-402
	LD8/LD8D2	3-405
SR Latch	LS0/LS0D2	3-408
	LS1/LS1D2	3-410

Bus Holder

Cell Type	Cell Name	Page
Bus Holder	BUSHOLDER	3-414

Internal Clock Drivers

Cell Type	Cell Name	Page
Internal Clock Driver	CK2/CK4/CK6/CK8/CK12/CK16/CK20	3-416

Decoders

Cell Type	Cell Name	Page
Non-Inverting Decoder	DC4	3-419
Inverting Decoder	DC4I	3-421
	DC8I	3-423

Adders

Cell Type	Cell Name	Page
Full Adder	FADH/FA/FAD2	3-427
Half Adder	HADH/HA/HAD2	3-431
Complex Cells	SCG23	3-434

Multiplexers

Cell Type	Cell Name	Page
2 > 1 Non-Inverting Mux	MX2DH/MX2/MX2D2/MX2D4	3-436
	MX2X4	3-439
2 > 1 Inverting Mux	MX2IDH/MX2I/MX2ID2/MX2ID4	3-441
	MX2IDHA/MX2IA/MX2ID2A/MX2ID4A	3-444
	MX2IX4	3-447
3 > 1 Inverting Mux	MX3I/MX3ID2/MX3ID4	3-449
4 > 1 Non-Inverting Mux	MX4/MX4D2/MX4D4	3-453
8 > 1 Non-Inverting Mux	MX8/MX8D2/MX8D4	3-457

Cell Names & Function Descriptions

Cell Name	Function Description
AD2DH	2-Input AND with 0.5X Drive
AD2	2-Input AND with 1X Drive
AD2D2	2-Input AND with 2X Drive
AD2D4	2-Input AND with 4X Drive
AD3DH	3-Input AND with 0.5X Drive
AD3	3-Input AND with 1X Drive
AD3D2	3-Input AND with 2X Drive
AD3D4	3-Input AND with 4X Drive
AD4DH	4-Input AND with 0.5X Drive
AD4	4-Input AND with 1X Drive
AD4D2	4-Input AND with 2X Drive
AD4D4	4-Input AND with 4X Drive
AD5	5-Input AND with 1X Drive
AD5D2	5-Input AND with 2X Drive
AD5D4	5-Input AND with 4X Drive
ND2DH	2-Input NAND with 0.5X Drive
ND2	2-Input NAND with 1X Drive
ND2D2	2-Input NAND with 2X Drive
ND2D4	2-Input NAND with 4X Drive
ND3DH	3-Input NAND with 0.5X Drive
ND3	3-Input NAND with 1X Drive
ND3D2	3-Input NAND with 2X Drive
ND3D4	3-Input NAND with 4X Drive
ND4DH	4-Input NAND with 1X Drive
ND4	4-Input NAND with 1X Drive
ND4D2	4-Input NAND with 2X Drive
ND4D2B	4-Input NAND with 2X(Buffered) Drive
ND4D4	4-Input NAND with 4X Drive
ND5	5-Input NAND with 1X Drive
ND5D2	5-Input NAND with 2X Drive
ND5D4	5-Input NAND with 4X Drive
ND6	6-Input NAND with 1X Drive
ND6D2	6-Input NAND with 2X Drive
ND6D4	6-Input NAND with 4X Drive
ND8	8-Input NAND with 1X Drive
ND8D2	8-Input NAND with 2X Drive
ND8D4	8-Input NAND with 4X Drive
NR2DH	2-Input NOR with 0.5X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
NR2	2-Input NOR with 1X Drive
NR2D2	2-Input NOR with 2X Drive
NR2D2B	2-Input NOR with 2X(Buffered) Drive
NR2D4	2-Input NOR with 4X Drive
NR3DH	3-Input NOR with 0.5X Drive
NR3	3-Input NOR with 1X Drive
NR3D2	3-Input NOR with 2X Drive
NR3D2B	3-Input NOR with 2X(Buffered) Drive
NR3D4	3-Input NOR with 4X Drive
NR4DH	4-Input NOR with 0.5X Drive
NR4	4-Input NOR with 1X Drive
NR4D2	4-Input NOR with 2X Drive
NR4D2B	4-Input NOR with 2X(Buffered) Drive
NR4D4	4-Input NOR with 4X Drive
NR5	5-Input NOR with 1X Drive
NR5D2	5-Input NOR with 2X Drive
NR5D4	5-Input NOR with 4X Drive
NR6	6-Input NOR with 1X Drive
NR6D2	6-Input NOR with 2X Drive
NR6D4	6-Input NOR with 4X Drive
NR8	8-Input NOR with 1X Drive
NR8D2	8-Input NOR with 2X Drive
NR8D4	8-Input NOR with 4X Drive
OR2DH	2-Input OR with 0.5X Drive
OR2	2-Input OR with 1X Drive
OR2D2	2-Input OR with 2X Drive
OR2D4	2-Input OR with 4X Drive
OR3DH	3-Input OR with 0.5X Drive
OR3	3-Input OR with 1X Drive
OR3D2	3-Input OR with 2X Drive
OR3D4	3-Input OR with 4X Drive
OR4DH	4-Input OR with 0.5X Drive
OR4	4-Input OR with 1X Drive
OR4D2	4-Input OR with 2X Drive
OR4D4	4-Input OR with 4X Drive
OR5	5-Input OR with 1X Drive
OR5D2	5-Input OR with 2X Drive
OR5D4	5-Input OR with 4X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
XN2	2-Input Exclusive-NOR with 1X Drive
XN2D2	2-Input Exclusive-NOR with 2X Drive
XN2D4	2-Input Exclusive-NOR with 4X Drive
XN3	3-Input Exclusive-NOR with 1X Drive
XN3D2	3-Input Exclusive-NOR with 2X Drive
XN3D4	3-Input Exclusive-NOR with 4X Drive
XO2	2-Input Exclusive-OR with 1X Drive
XO2D2	2-Input Exclusive-OR with 2X Drive
XO2D4	2-Input Exclusive-OR with 4X Drive
XO3	3-Input Exclusive-OR with 1X Drive
XO3D2	3-Input Exclusive-OR with 2X Drive
XO3D4	3-Input Exclusive-OR with 4X Drive
AO21	2-AND into 2-NOR with 1X Drive
AO21D2	2-AND into 2-NOR with 2X Drive
AO21D2B	2-AND into 2-NOR with 2X(Buffered) Drive
AO21D4	2-AND into 2-NOR with 4X Drive
AO211	2-AND into 3-NOR with 1X Drive
AO211D2	2-AND into 3-NOR with 2X Drive
AO211D2B	2-AND into 3-NOR with 2X(Buffered) Drive
AO211D4	2-AND into 3-NOR with 4X Drive
AO2111	2-AND into 4-NOR with 1X Drive
AO2111D2	2-AND into 4-NOR with 2X Drive
AO22	Two 2-ANDs into 2-NOR with 1X Drive
AO22D2	Two 2-ANDs into 2-NOR with 2X Drive
AO22D2B	Two 2-ANDs into 2-NOR with 2X(Buffered) Drive
AO22D4	Two 2-ANDs into 2-NOR with 4X Drive
AO22A	2-AND and 2-NOR into 2-NOR with 1X Drive
AO22D2A	2-AND and 2-NOR into 2-NOR with 2X Drive
AO22D4A	2-AND and 2-NOR into 2-NOR with 4X Drive
AO221	Two 2-ANDs into 3-NOR with 1X Drive
AO221D2	Two 2-ANDs into 3-NOR with 2X Drive
AO221D4	Two 2-ANDs into 3-NOR with 4X Drive
AO222	Three 2-ANDs into 3-NOR with 1X Drive
AO222D2	Three 2-ANDs into 3-NOR with 2X Drive
AO222D2B	Three 2-ANDs into 3-NOR with 2X(Buffered) Drive
AO222D4	Three 2-ANDs into 3-NOR with 4X Drive
AO222A	Inverting 2-of-3 Majority with 1X Drive
AO222D2A	Inverting 2-of-3 Majority with 2X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
AO222D4A	Inverting 2-of-3 Majority with 4X Drive
AO2222	Four 2-ANDs into 4-NOR with 1X Drive
AO2222D2	Four 2-ANDs into 4-NOR with 2X Drive
AO2222D4	Four 2-ANDs into 4-NOR with 4X Drive
AO31	3-AND into 2-NOR with 1X Drive
AO31D2	3-AND into 2-NOR with 2X Drive
AO31D4	3-AND into 2-NOR with 4X Drive
AO311	3-AND into 3-NOR with 1X Drive
AO311D2	3-AND into 3-NOR with 2X Drive
AO311D4	3-AND into 3-NOR with 4X Drive
AO3111	3-AND into 4-NOR with 1X Drive
AO3111D2	3-AND into 4-NOR with 2X Drive
AO32	3-AND and 2-AND into 2-NOR with 1X Drive
AO32D2	3-AND and 2-AND into 2-NOR with 2X Drive
AO32D4	3-AND and 2-AND into 2-NOR with 4X Drive
AO321	3-AND and 2-AND into 3-NOR with 1X Drive
AO321D2	3-AND and 2-AND into 3-NOR with 2X Drive
AO321D4	3-AND and 2-AND into 3-NOR with 4X Drive
AO322	3-AND and Two 2-ANDs into 3-NOR with 1X Drive
AO322D2	3-AND and Two 2-ANDs into 3-NOR with 2X Drive
AO322D4	3-AND and Two 2-ANDs into 3-NOR with 4X Drive
AO33	Two 3-ANDs into 2-NOR with 1X Drive
AO33D2	Two 3-ANDs into 2-NOR with 2X Drive
AO33D4	Two 3-ANDs into 2-NOR with 4X Drive
AO331	Two 3-ANDs into 3-NOR with 1X Drive
AO331D2	Two 3-ANDs into 3-NOR with 2X Drive
AO331D4	Two 3-ANDs into 3-NOR with 4X Drive
AO332	Two 3-ANDs and 2-AND into 3-NOR
AO332D2	Two 3-ANDs and 2-AND into 3-NOR with 2X Drive
AO332D4	Two 3-ANDs and 2-AND into 3-NOR with 4X Drive
AO4111	4-AND into 4-NOR with 1X Drive
AO4111D2	4-AND into 4-NOR with 2X Drive
OA21	2-OR into 2-NAND with 1X Drive
OA21D2	2-OR into 2-NAND with 2X Drive
OA21D2B	2-OR into 2-NAND with 2X(Buffered) Drive
OA21D4	2-OR into 2-NAND with 4X Drive
OA211	2-OR into 3-NAND with 1X Drive
OA211D2	2-OR into 3-NAND with 2X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
OA211D2B	2-OR into 3-NAND with 2X(Buffered) Drive
OA211D4	2-OR into 3-NAND with 4X Drive
OA2111	2-OR into 4-NAND with 1X Drive
OA2111D2	2-OR into 4-NAND with 2X Drive
OA22	Two 2-ORs into 2-NAND with 1X Drive
OA22D2	Two 2-ORs into 2-NAND with 2X Drive
OA22D2B	Two 2-ORs into 2-NAND with 2X(Buffered) Drive
OA22D4	Two 2-ORs into 2-NAND with 4X Drive
OA22A	2-OR and 2-NAND into 2-NAND with 1X Drive
OA22D2A	2-OR and 2-NAND into 2-NAND with 2X Drive
OA22D4A	2-OR and 2-NAND into 2-NAND with 4X Drive
OA221	Two 2-ORs into 3-NAND with 1X Drive
OA221D2	Two 2-ORs into 3-NAND with 2X Drive
OA221D4	Two 2-ORs into 3-NAND with 4X Drive
OA222	Three 2-ORs into 3-NAND with 1X Drive
OA222D2	Three 2-ORs into 3-NAND with 2X Drive
OA222D2B	Three 2-ORs into 3-NAND with 2X(Buffered) Drive
OA222D4	Three 2-ORs into 3-NAND with 4X Drive
OA2222	Four 2-ORs into 4-NAND with 1X Drive
OA2222D2	Four 2-ORs into 4-NAND with 2X Drive
OA2222D4	Four 2-ORs into 4-NAND with 4X Drive
OA31	3-OR into 2-NAND with 1X Drive
OA31D2	3-OR into 2-NAND with 2X Drive
OA31D4	3-OR into 2-NAND with 4X Drive
OA311	3-OR into 3-NAND with 1X Drive
OA311D2	3-OR into 3-NAND with 2X Drive
OA311D4	3-OR into 3-NAND with 4X Drive
OA3111	3-OR into 4-NAND with 1X Drive
OA3111D2	3-OR into 4-NAND with 2X Drive
OA32	3-OR and 2-OR into 2-NAND with 1X Drive
OA32D2	3-OR and 2-OR into 2-NAND with 2X Drive
OA32D4	3-OR and 2-OR into 2-NAND with 4X Drive
OA321	3-OR and 2-OR into 3-NAND with 1X Drive
OA321D2	3-OR and 2-OR into 3-NAND with 2X Drive
OA321D4	3-OR and 2-OR into 3-NAND with 4X Drive
OA322	3-OR and Two 2-ORs into 3-NAND with 1X Drive
OA322D2	3-OR and Two 2-ORs into 3-NAND with 2X Drive
OA322D4	3-OR and Two 2-ORs into 3-NAND with 4X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
OA33	Two 3-ORs into 2-NAND with 1X Drive
OA33D2	Two 3-ORs into 2-NAND with 2X Drive
OA33D4	Two 3-ORs into 2-NAND with 4X Drive
OA331	Two 3-ORs into 3-NAND with 1X Drive
OA331D2	Two 3-ORs into 3-NAND with 2X Drive
OA331D4	Two 3-ORs into 3-NAND with 4X Drive
OA332	Two 3-ORs and 2-OR into 3-NAND with 1X Drive
OA332D2	Two 3-ORs and 2-OR into 3-NAND with 2X Drive
OA332D4	Two 3-ORs and 2-OR into 3-NAND with 4X Drive
OA4111	4-OR into 4-NAND with 1X Drive
OA4111D2	4-OR into 4-NAND with 2X Drive
SCG1	2-NAND and two (2-AND into 2-NOR)s into 3-NAND
SCG2	Two 2-ANDs into 2-OR
SCG3	Two 2-NANDs into 3-NAND
SCG4	Two (two 2-ANDs into 2-NOR)s into 2-NAND
SCG5	Three 2-ANDs into 3-OR
SCG6	2-AND into 2-OR
SCG7	2-NAND and (2-AND into 2-NOR) into 2-NAND
SCG8	2-AND into 3-OR
SCG9	2-OR into 2-AND
SCG10	Two 2-ORs into 2-AND
SCG11	Two 2-NORs into 3-NOR
SCG12	2-NAND into 2-NOR
SCG13	2-NOR into 2-NAND
SCG14	2-NAND into 2-NAND
SCG15	2-NAND into 3-NAND
SCG16	2-OR with one inverted input into 2-NAND
SCG17	2-AND into 2-NOR into 2-NAND
SCG18	2-AND into 2-NOR into 3-NAND
SCG19	2-AND into 2-AND into 2-NOR
SCG20	2-NOR into 2-NOR
SCG21	2-NOR into 3-NOR
SCG22	2-NAND into 2-OR into 2-NAND
DL1D2	1ns Delay Cell with 2X Drive
DL1D4	1ns Delay Cell with 4X Drive
DL2D2	2ns Delay Cell with 2X Drive
DL2D4	2ns Delay Cell with 4X Drive
DL3D2	3ns Delay Cell with 2X Drive

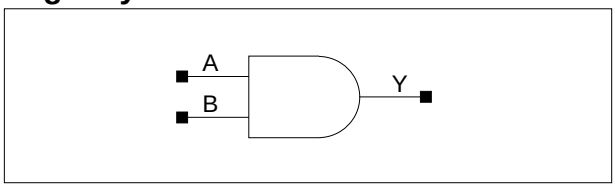
Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
DL3D4	3ns Delay Cell with 4X Drive
DL4D2	4ns Delay Cell with 2X Drive
DL4D4	4ns Delay Cell with 4X Drive
DL5D2	5ns Delay Cell with 2X Drive
DL5D4	5ns Delay Cell with 4X Drive
DL10D2	10ns Delay Cell with 2X Drive
DL10D4	10ns Delay Cell with 4X Drive
IVDH	Inverter with 0.5X Drive
IV	Inverter with 1X Drive
IVD2	Inverter with 2X Drive
IVD3	Inverter with 3X Drive
IVD4	Inverter with 4X Drive
IVD6	Inverter with 6X Drive
IVD8	Inverter with 8X Drive
IVD16	Inverter with 16X Drive
IVCD11	1X Inverter into 1X Inverter
IVCD13	1X Inverter into 3X Inverter
IVCD22	2X Inverter into 2X Inverter
IVCD26	2X Inverter into 6X Inverter
IVCD44	4X Inverter into 4X Inverter
IVT	Inverting Tri-State Buffer with Enable High, 1X Drive
IVTD2	Inverting Tri-State Buffer with Enable High, 2X Drive
IVTD4	Inverting Tri-State Buffer with Enable High, 4X Drive
IVTD8	Inverting Tri-State Buffer with Enable High, 8X Drive
IVTD16	Inverting Tri-State Buffer with Enable High, 16X Drive
IVTN	Inverting Tri-State Buffer with Enable Low, 1X Drive
IVTND2	Inverting Tri-State Buffer with Enable Low, 2X Drive
IVTND4	Inverting Tri-State Buffer with Enable Low, 4X Drive
IVTND8	Inverting Tri-State Buffer with Enable Low, 8X Drive
IVTND16	Inverting Tri-State Buffer with Enable Low, 16X Drive
NID	Non-Inverting Buffer with 1X Drive
NID2	Non-Inverting Buffer with 2X Drive
NID3	Non-Inverting Buffer with 3X Drive
NID4	Non-Inverting Buffer with 4X Drive
NID6	Non-Inverting Buffer with 6X Drive
NID8	Non-Inverting Buffer with 8X Drive
NID16	Non-Inverting Buffer with 16X Drive
NIT	Non-Inverting Tri-State Buffer with Enable High, 1X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
NITD2	Non-Inverting Tri-State Buffer with Enable High, 2X Drive
NITD4	Non-Inverting Tri-State Buffer with Enable High, 4X Drive
NITD8	Non-Inverting Tri-State Buffer with Enable High, 8X Drive
NITD16	Non-Inverting Tri-State Buffer with Enable High, 16X Drive
NITN	Non-Inverting Tri-State Buffer with Enable Low, 1X Drive
NITND2	Non-Inverting Tri-State Buffer with Enable Low, 2X Drive
NITND4	Non-Inverting Tri-State Buffer with Enable Low, 4X Drive
NITND8	Non-Inverting Tri-State Buffer with Enable Low, 8X Drive
NITND16	Non-Inverting Tri-State Buffer with Enable Low, 16X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Cell Data

Input Load (SL)								Gate Count			
AD2DH		*AD2*		*AD2D2*		*AD2D4*		*AD2DH*	*AD2*	*AD2D2*	*AD2D4*
A	B	A	B	A	B	A	B				
0.5	0.5	0.8	0.8	1.1	1.1	1.1	1.1	1.33	1.33	1.67	2.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AD2DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.206	0.070 + 0.068*SL	0.057 + 0.072*SL	0.047 + 0.072*SL
	t_F	0.156	0.054 + 0.051*SL	0.040 + 0.054*SL	0.031 + 0.055*SL
	t_{PLH}	0.210	0.143 + 0.034*SL	0.146 + 0.033*SL	0.147 + 0.033*SL
	t_{PHL}	0.204	0.144 + 0.030*SL	0.149 + 0.029*SL	0.149 + 0.029*SL
B to Y	t_R	0.206	0.068 + 0.069*SL	0.057 + 0.072*SL	0.047 + 0.072*SL
	t_F	0.156	0.054 + 0.051*SL	0.041 + 0.054*SL	0.031 + 0.055*SL
	t_{PLH}	0.198	0.131 + 0.034*SL	0.135 + 0.033*SL	0.135 + 0.033*SL
	t_{PHL}	0.215	0.155 + 0.030*SL	0.160 + 0.029*SL	0.160 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

AD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.149	0.077 + 0.036*SL	0.068 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.121	0.059 + 0.031*SL	0.051 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.185	0.147 + 0.019*SL	0.154 + 0.017*SL	0.156 + 0.017*SL
	t_{PHL}	0.185	0.146 + 0.019*SL	0.153 + 0.018*SL	0.154 + 0.018*SL
B to Y	t_R	0.148	0.076 + 0.036*SL	0.068 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.123	0.061 + 0.031*SL	0.052 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.173	0.135 + 0.019*SL	0.142 + 0.017*SL	0.144 + 0.017*SL
	t_{PHL}	0.197	0.159 + 0.019*SL	0.165 + 0.018*SL	0.166 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.104	0.068 + 0.018*SL	0.063 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.082	0.051 + 0.015*SL	0.046 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.171	0.149 + 0.011*SL	0.158 + 0.009*SL	0.165 + 0.009*SL
	t_{PHL}	0.175	0.153 + 0.011*SL	0.162 + 0.009*SL	0.168 + 0.009*SL
B to Y	t_R	0.103	0.066 + 0.018*SL	0.064 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.084	0.052 + 0.016*SL	0.049 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.158	0.136 + 0.011*SL	0.146 + 0.009*SL	0.153 + 0.009*SL
	t_{PHL}	0.187	0.164 + 0.011*SL	0.174 + 0.009*SL	0.181 + 0.009*SL

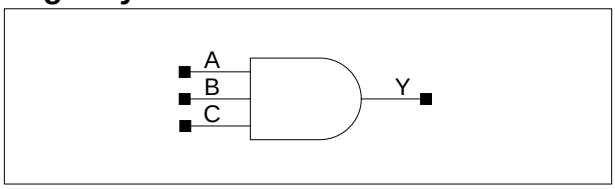
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AD2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.105	0.087 + 0.009*SL	0.086 + 0.009*SL	0.065 + 0.010*SL
	t_F	0.079	0.062 + 0.009*SL	0.064 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.212	0.198 + 0.007*SL	0.207 + 0.005*SL	0.228 + 0.004*SL
	t_{PHL}	0.208	0.195 + 0.007*SL	0.203 + 0.005*SL	0.221 + 0.004*SL
B to Y	t_R	0.106	0.087 + 0.009*SL	0.087 + 0.009*SL	0.065 + 0.010*SL
	t_F	0.083	0.066 + 0.009*SL	0.069 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.197	0.184 + 0.007*SL	0.192 + 0.005*SL	0.214 + 0.004*SL
	t_{PHL}	0.218	0.205 + 0.007*SL	0.214 + 0.005*SL	0.232 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Cell Data

Input Load (SL)												Gate Count			
AD3DH			*AD3*			*AD3D2*			*AD3D4*			*AD3DH*	*AD3*	*AD3D2*	*AD3D4*
A	B	C	A	B	C	A	B	C	A	B	C				
0.5	0.5	0.5	0.8	0.9	0.9	1.1	1.1	1.1	1.1	1.1	1.1	1.67	1.67	2.00	2.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AD3DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.218	0.082 + 0.068*SL	0.069 + 0.071*SL	0.048 + 0.072*SL
	t_F	0.159	0.055 + 0.052*SL	0.046 + 0.054*SL	0.031 + 0.055*SL
	t_{PLH}	0.242	0.171 + 0.035*SL	0.181 + 0.033*SL	0.182 + 0.033*SL
	t_{PHL}	0.229	0.167 + 0.031*SL	0.175 + 0.029*SL	0.176 + 0.029*SL
B to Y	t_R	0.219	0.083 + 0.068*SL	0.069 + 0.071*SL	0.048 + 0.072*SL
	t_F	0.162	0.060 + 0.051*SL	0.047 + 0.054*SL	0.031 + 0.055*SL
	t_{PLH}	0.237	0.167 + 0.035*SL	0.177 + 0.033*SL	0.178 + 0.033*SL
	t_{PHL}	0.243	0.180 + 0.031*SL	0.189 + 0.029*SL	0.190 + 0.029*SL
C to Y	t_R	0.219	0.083 + 0.068*SL	0.069 + 0.071*SL	0.048 + 0.072*SL
	t_F	0.165	0.063 + 0.051*SL	0.050 + 0.054*SL	0.031 + 0.055*SL
	t_{PLH}	0.232	0.161 + 0.035*SL	0.171 + 0.033*SL	0.173 + 0.033*SL
	t_{PHL}	0.256	0.193 + 0.032*SL	0.203 + 0.029*SL	0.204 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

AD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.158	0.085 + 0.036*SL	0.079 + 0.038*SL	0.055 + 0.039*SL
	t_F	0.123	0.061 + 0.031*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.215	0.173 + 0.021*SL	0.186 + 0.018*SL	0.192 + 0.017*SL
	t_{PHL}	0.205	0.165 + 0.020*SL	0.174 + 0.018*SL	0.177 + 0.018*SL
B to Y	t_R	0.159	0.087 + 0.036*SL	0.080 + 0.038*SL	0.055 + 0.039*SL
	t_F	0.125	0.062 + 0.032*SL	0.056 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.212	0.170 + 0.021*SL	0.183 + 0.018*SL	0.189 + 0.017*SL
	t_{PHL}	0.220	0.179 + 0.020*SL	0.189 + 0.018*SL	0.192 + 0.018*SL
C to Y	t_R	0.159	0.087 + 0.036*SL	0.080 + 0.038*SL	0.055 + 0.039*SL
	t_F	0.129	0.066 + 0.032*SL	0.060 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.206	0.164 + 0.021*SL	0.177 + 0.018*SL	0.184 + 0.017*SL
	t_{PHL}	0.232	0.192 + 0.020*SL	0.202 + 0.018*SL	0.206 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.116	0.079 + 0.019*SL	0.077 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.086	0.054 + 0.016*SL	0.052 + 0.017*SL	0.028 + 0.017*SL
	t_{PLH}	0.202	0.178 + 0.012*SL	0.191 + 0.009*SL	0.208 + 0.009*SL
	t_{PHL}	0.196	0.172 + 0.012*SL	0.183 + 0.009*SL	0.193 + 0.009*SL
B to Y	t_R	0.118	0.080 + 0.019*SL	0.079 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.090	0.056 + 0.017*SL	0.057 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.199	0.175 + 0.012*SL	0.188 + 0.009*SL	0.204 + 0.009*SL
	t_{PHL}	0.211	0.187 + 0.012*SL	0.199 + 0.009*SL	0.209 + 0.009*SL
C to Y	t_R	0.117	0.080 + 0.019*SL	0.079 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.095	0.061 + 0.017*SL	0.063 + 0.016*SL	0.030 + 0.017*SL
	t_{PLH}	0.193	0.169 + 0.012*SL	0.182 + 0.009*SL	0.199 + 0.009*SL
	t_{PHL}	0.223	0.199 + 0.012*SL	0.212 + 0.009*SL	0.223 + 0.009*SL

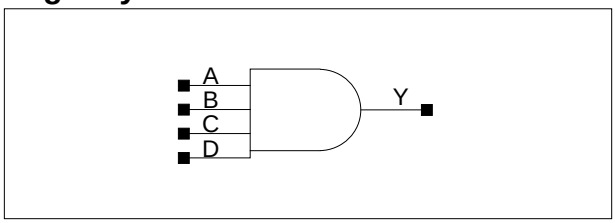
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AD3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.124	0.105 + 0.009*SL	0.105 + 0.009*SL	0.089 + 0.010*SL
	t_F	0.087	0.070 + 0.009*SL	0.072 + 0.008*SL	0.053 + 0.008*SL
	t_{PLH}	0.247	0.231 + 0.008*SL	0.242 + 0.005*SL	0.278 + 0.004*SL
	t_{PHL}	0.230	0.216 + 0.007*SL	0.226 + 0.005*SL	0.250 + 0.004*SL
B to Y	t_R	0.123	0.106 + 0.009*SL	0.103 + 0.009*SL	0.088 + 0.010*SL
	t_F	0.093	0.075 + 0.009*SL	0.079 + 0.008*SL	0.055 + 0.008*SL
	t_{PLH}	0.243	0.227 + 0.008*SL	0.239 + 0.005*SL	0.274 + 0.004*SL
	t_{PHL}	0.244	0.229 + 0.007*SL	0.239 + 0.005*SL	0.265 + 0.004*SL
C to Y	t_R	0.124	0.106 + 0.009*SL	0.105 + 0.009*SL	0.088 + 0.010*SL
	t_F	0.098	0.081 + 0.008*SL	0.083 + 0.008*SL	0.059 + 0.008*SL
	t_{PLH}	0.237	0.222 + 0.008*SL	0.233 + 0.005*SL	0.269 + 0.004*SL
	t_{PHL}	0.256	0.241 + 0.008*SL	0.252 + 0.005*SL	0.279 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Cell Data

Input Load (SL)															
AD4DH				*AD4*				*AD4D2*				*AD4D4*			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.4	0.4	0.4	0.5	0.7	0.7	0.7	0.7	0.9	0.9	0.9	1.0	0.9	0.9	0.9	1.0

Gate Counts			
AD4DH	*AD4*	*AD4D2*	*AD4D4*
2.00	2.00	2.00	2.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AD4DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.231	0.097 + 0.067*SL	0.087 + 0.070*SL	0.055 + 0.071*SL
	t_F	0.165	0.062 + 0.052*SL	0.052 + 0.054*SL	0.033 + 0.055*SL
	t_{PLH}	0.272	0.199 + 0.037*SL	0.217 + 0.032*SL	0.221 + 0.032*SL
	t_{PHL}	0.246	0.182 + 0.032*SL	0.193 + 0.029*SL	0.194 + 0.029*SL
B to Y	t_R	0.232	0.098 + 0.067*SL	0.088 + 0.070*SL	0.055 + 0.071*SL
	t_F	0.168	0.066 + 0.051*SL	0.054 + 0.054*SL	0.034 + 0.055*SL
	t_{PLH}	0.274	0.201 + 0.036*SL	0.219 + 0.032*SL	0.223 + 0.032*SL
	t_{PHL}	0.261	0.197 + 0.032*SL	0.208 + 0.029*SL	0.209 + 0.029*SL
C to Y	t_R	0.232	0.098 + 0.067*SL	0.088 + 0.070*SL	0.055 + 0.071*SL
	t_F	0.173	0.072 + 0.050*SL	0.057 + 0.054*SL	0.034 + 0.055*SL
	t_{PLH}	0.275	0.202 + 0.037*SL	0.219 + 0.032*SL	0.224 + 0.032*SL
	t_{PHL}	0.274	0.210 + 0.032*SL	0.222 + 0.029*SL	0.224 + 0.029*SL
D to Y	t_R	0.232	0.098 + 0.067*SL	0.087 + 0.070*SL	0.055 + 0.071*SL
	t_F	0.177	0.075 + 0.051*SL	0.062 + 0.054*SL	0.035 + 0.055*SL
	t_{PLH}	0.273	0.200 + 0.037*SL	0.218 + 0.032*SL	0.222 + 0.032*SL
	t_{PHL}	0.286	0.220 + 0.033*SL	0.234 + 0.029*SL	0.237 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

AD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.173	0.099 + 0.037*SL	0.097 + 0.037*SL	0.069 + 0.038*SL
	t_F	0.128	0.066 + 0.031*SL	0.061 + 0.032*SL	0.040 + 0.033*SL
	t_{PLH}	0.236	0.192 + 0.022*SL	0.209 + 0.018*SL	0.222 + 0.017*SL
	t_{PHL}	0.223	0.183 + 0.020*SL	0.193 + 0.017*SL	0.198 + 0.017*SL
B to Y	t_R	0.173	0.099 + 0.037*SL	0.099 + 0.037*SL	0.069 + 0.038*SL
	t_F	0.131	0.069 + 0.031*SL	0.063 + 0.032*SL	0.041 + 0.033*SL
	t_{PLH}	0.240	0.196 + 0.022*SL	0.213 + 0.018*SL	0.226 + 0.017*SL
	t_{PHL}	0.240	0.200 + 0.020*SL	0.211 + 0.017*SL	0.215 + 0.017*SL
C to Y	t_R	0.174	0.100 + 0.037*SL	0.099 + 0.037*SL	0.069 + 0.038*SL
	t_F	0.137	0.076 + 0.030*SL	0.069 + 0.032*SL	0.042 + 0.033*SL
	t_{PLH}	0.242	0.198 + 0.022*SL	0.215 + 0.018*SL	0.228 + 0.017*SL
	t_{PHL}	0.256	0.215 + 0.020*SL	0.227 + 0.017*SL	0.232 + 0.017*SL
D to Y	t_R	0.173	0.099 + 0.037*SL	0.098 + 0.037*SL	0.069 + 0.038*SL
	t_F	0.141	0.081 + 0.030*SL	0.074 + 0.032*SL	0.046 + 0.033*SL
	t_{PLH}	0.241	0.198 + 0.022*SL	0.214 + 0.018*SL	0.228 + 0.017*SL
	t_{PHL}	0.268	0.226 + 0.021*SL	0.240 + 0.017*SL	0.248 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.132	0.094 + 0.019*SL	0.095 + 0.019*SL	0.064 + 0.019*SL
	t_F	0.093	0.059 + 0.017*SL	0.061 + 0.016*SL	0.032 + 0.017*SL
	t_{PLH}	0.228	0.201 + 0.013*SL	0.218 + 0.009*SL	0.247 + 0.009*SL
	t_{PHL}	0.217	0.193 + 0.012*SL	0.205 + 0.009*SL	0.218 + 0.009*SL
B to Y	t_R	0.134	0.096 + 0.019*SL	0.097 + 0.019*SL	0.064 + 0.019*SL
	t_F	0.099	0.067 + 0.016*SL	0.065 + 0.016*SL	0.033 + 0.017*SL
	t_{PLH}	0.233	0.206 + 0.013*SL	0.222 + 0.009*SL	0.251 + 0.009*SL
	t_{PHL}	0.234	0.209 + 0.012*SL	0.223 + 0.009*SL	0.236 + 0.009*SL
C to Y	t_R	0.135	0.097 + 0.019*SL	0.097 + 0.019*SL	0.064 + 0.019*SL
	t_F	0.105	0.071 + 0.017*SL	0.073 + 0.016*SL	0.035 + 0.017*SL
	t_{PLH}	0.235	0.209 + 0.013*SL	0.225 + 0.009*SL	0.254 + 0.009*SL
	t_{PHL}	0.249	0.224 + 0.013*SL	0.239 + 0.009*SL	0.254 + 0.009*SL
D to Y	t_R	0.134	0.097 + 0.019*SL	0.095 + 0.019*SL	0.065 + 0.019*SL
	t_F	0.111	0.077 + 0.017*SL	0.079 + 0.016*SL	0.039 + 0.017*SL
	t_{PLH}	0.236	0.209 + 0.013*SL	0.226 + 0.009*SL	0.255 + 0.009*SL
	t_{PHL}	0.263	0.236 + 0.013*SL	0.253 + 0.009*SL	0.272 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AD4D4

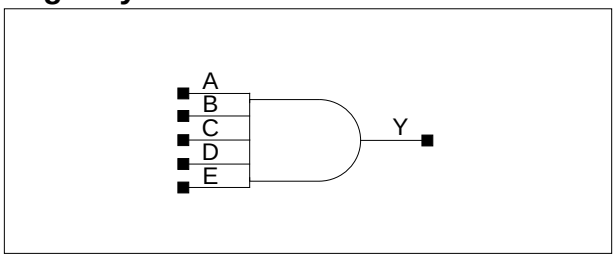
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.148	0.129 + 0.009*SL	0.130 + 0.009*SL	0.119 + 0.009*SL
	t_F	0.100	0.084 + 0.008*SL	0.085 + 0.008*SL	0.065 + 0.008*SL
	t_{PLH}	0.284	0.267 + 0.008*SL	0.281 + 0.005*SL	0.330 + 0.004*SL
	t_{PHL}	0.260	0.245 + 0.007*SL	0.256 + 0.005*SL	0.286 + 0.004*SL
B to Y	t_R	0.149	0.130 + 0.009*SL	0.130 + 0.009*SL	0.119 + 0.009*SL
	t_F	0.106	0.088 + 0.009*SL	0.092 + 0.008*SL	0.069 + 0.008*SL
	t_{PLH}	0.289	0.272 + 0.008*SL	0.285 + 0.005*SL	0.334 + 0.004*SL
	t_{PHL}	0.276	0.261 + 0.008*SL	0.272 + 0.005*SL	0.304 + 0.004*SL
C to Y	t_R	0.149	0.131 + 0.009*SL	0.130 + 0.009*SL	0.119 + 0.009*SL
	t_F	0.113	0.096 + 0.009*SL	0.100 + 0.008*SL	0.074 + 0.008*SL
	t_{PLH}	0.291	0.274 + 0.008*SL	0.288 + 0.005*SL	0.337 + 0.004*SL
	t_{PHL}	0.291	0.275 + 0.008*SL	0.287 + 0.005*SL	0.322 + 0.004*SL
D to Y	t_R	0.149	0.131 + 0.009*SL	0.130 + 0.009*SL	0.119 + 0.009*SL
	t_F	0.120	0.101 + 0.009*SL	0.107 + 0.008*SL	0.081 + 0.008*SL
	t_{PLH}	0.292	0.275 + 0.008*SL	0.288 + 0.005*SL	0.337 + 0.004*SL
	t_{PHL}	0.305	0.288 + 0.008*SL	0.301 + 0.005*SL	0.339 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AD5/AD5D2/AD5D4

5-Input AND with 1X/2X/4XDrive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	x	x	x	0
x	0	x	x	x	0
x	x	0	x	x	0
x	x	x	0	x	0
x	x	x	x	0	0
1	1	1	1	1	1

Cell Data

Input Load (SL)														
AD5					*AD5D2*					*AD5D4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.6	0.6	0.6	0.6	0.6	0.7	0.8	0.8	0.8	0.8	0.7	0.7	0.8	0.7	0.8
Gate Count														
AD5					*AD5D2*					*AD5D4*				
2.67					3.00					4.33				

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.272	0.129 + 0.071*SL	0.120 + 0.074*SL	0.109 + 0.074*SL
	t_F	0.156	0.100 + 0.028*SL	0.094 + 0.029*SL	0.067 + 0.030*SL
	t_{PLH}	0.248	0.180 + 0.034*SL	0.186 + 0.033*SL	0.189 + 0.033*SL
	t_{PHL}	0.262	0.224 + 0.019*SL	0.235 + 0.016*SL	0.243 + 0.016*SL
B to Y	t_R	0.273	0.130 + 0.071*SL	0.121 + 0.074*SL	0.109 + 0.074*SL
	t_F	0.164	0.109 + 0.027*SL	0.101 + 0.029*SL	0.068 + 0.030*SL
	t_{PLH}	0.247	0.179 + 0.034*SL	0.184 + 0.033*SL	0.187 + 0.033*SL
	t_{PHL}	0.286	0.248 + 0.019*SL	0.260 + 0.016*SL	0.268 + 0.016*SL
C to Y	t_R	0.272	0.130 + 0.071*SL	0.120 + 0.074*SL	0.109 + 0.074*SL
	t_F	0.173	0.120 + 0.027*SL	0.110 + 0.029*SL	0.071 + 0.030*SL
	t_{PLH}	0.243	0.175 + 0.034*SL	0.181 + 0.033*SL	0.184 + 0.033*SL
	t_{PHL}	0.309	0.270 + 0.020*SL	0.284 + 0.016*SL	0.293 + 0.016*SL
D to Y	t_R	0.263	0.119 + 0.072*SL	0.113 + 0.074*SL	0.108 + 0.074*SL
	t_F	0.120	0.064 + 0.028*SL	0.060 + 0.029*SL	0.039 + 0.030*SL
	t_{PLH}	0.193	0.126 + 0.033*SL	0.128 + 0.033*SL	0.130 + 0.033*SL
	t_{PHL}	0.234	0.197 + 0.018*SL	0.208 + 0.016*SL	0.213 + 0.016*SL
E to Y	t_R	0.263	0.119 + 0.072*SL	0.112 + 0.074*SL	0.108 + 0.074*SL
	t_F	0.127	0.073 + 0.027*SL	0.066 + 0.029*SL	0.041 + 0.030*SL
	t_{PLH}	0.185	0.119 + 0.033*SL	0.121 + 0.033*SL	0.123 + 0.033*SL
	t_{PHL}	0.258	0.220 + 0.019*SL	0.233 + 0.016*SL	0.239 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AD5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.192	0.121 + 0.035*SL	0.115 + 0.037*SL	0.094 + 0.037*SL
	t_F	0.143	0.115 + 0.014*SL	0.113 + 0.014*SL	0.072 + 0.015*SL
	t_{PLH}	0.229	0.193 + 0.018*SL	0.200 + 0.016*SL	0.207 + 0.016*SL
	t_{PHL}	0.281	0.258 + 0.011*SL	0.271 + 0.008*SL	0.292 + 0.008*SL
B to Y	t_R	0.192	0.122 + 0.035*SL	0.114 + 0.037*SL	0.094 + 0.037*SL
	t_F	0.154	0.127 + 0.014*SL	0.125 + 0.014*SL	0.075 + 0.015*SL
	t_{PLH}	0.227	0.191 + 0.018*SL	0.199 + 0.016*SL	0.205 + 0.016*SL
	t_{PHL}	0.307	0.284 + 0.012*SL	0.298 + 0.008*SL	0.320 + 0.008*SL
C to Y	t_R	0.192	0.123 + 0.034*SL	0.114 + 0.037*SL	0.094 + 0.037*SL
	t_F	0.165	0.138 + 0.014*SL	0.136 + 0.014*SL	0.079 + 0.015*SL
	t_{PLH}	0.222	0.185 + 0.018*SL	0.193 + 0.016*SL	0.200 + 0.016*SL
	t_{PHL}	0.331	0.307 + 0.012*SL	0.323 + 0.008*SL	0.348 + 0.008*SL
D to Y	t_R	0.178	0.107 + 0.036*SL	0.102 + 0.037*SL	0.092 + 0.037*SL
	t_F	0.104	0.075 + 0.015*SL	0.075 + 0.015*SL	0.043 + 0.015*SL
	t_{PLH}	0.170	0.135 + 0.017*SL	0.139 + 0.016*SL	0.141 + 0.016*SL
	t_{PHL}	0.251	0.227 + 0.012*SL	0.241 + 0.008*SL	0.259 + 0.008*SL
E to Y	t_R	0.178	0.107 + 0.035*SL	0.102 + 0.037*SL	0.093 + 0.037*SL
	t_F	0.114	0.085 + 0.015*SL	0.085 + 0.014*SL	0.046 + 0.015*SL
	t_{PLH}	0.162	0.127 + 0.017*SL	0.132 + 0.016*SL	0.133 + 0.016*SL
	t_{PHL}	0.276	0.251 + 0.012*SL	0.268 + 0.008*SL	0.288 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

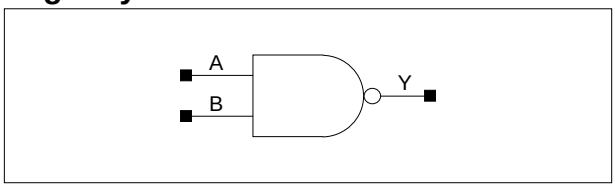
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AD5D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.093	0.075 + 0.009*SL	0.074 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.078	0.061 + 0.008*SL	0.062 + 0.008*SL	0.041 + 0.008*SL
	t_{PLH}	0.415	0.403 + 0.006*SL	0.410 + 0.005*SL	0.420 + 0.004*SL
	t_{PHL}	0.382	0.369 + 0.007*SL	0.377 + 0.005*SL	0.395 + 0.004*SL
B to Y	t_R	0.093	0.076 + 0.008*SL	0.073 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.078	0.061 + 0.008*SL	0.063 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.412	0.400 + 0.006*SL	0.407 + 0.005*SL	0.417 + 0.004*SL
	t_{PHL}	0.400	0.387 + 0.007*SL	0.395 + 0.005*SL	0.412 + 0.004*SL
C to Y	t_R	0.093	0.076 + 0.009*SL	0.073 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.078	0.062 + 0.008*SL	0.061 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.406	0.394 + 0.006*SL	0.401 + 0.005*SL	0.410 + 0.004*SL
	t_{PHL}	0.416	0.402 + 0.007*SL	0.411 + 0.005*SL	0.428 + 0.004*SL
D to Y	t_R	0.093	0.076 + 0.009*SL	0.073 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.077	0.061 + 0.008*SL	0.061 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.358	0.346 + 0.006*SL	0.352 + 0.005*SL	0.362 + 0.004*SL
	t_{PHL}	0.354	0.340 + 0.007*SL	0.349 + 0.005*SL	0.366 + 0.004*SL
E to Y	t_R	0.093	0.076 + 0.009*SL	0.073 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.076	0.058 + 0.009*SL	0.062 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.349	0.336 + 0.006*SL	0.343 + 0.005*SL	0.353 + 0.004*SL
	t_{PHL}	0.372	0.358 + 0.007*SL	0.366 + 0.005*SL	0.384 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Cell Data

Input Load (SL)								Gate Count			
ND2DH		*ND2*		*ND2D2*		*ND2D4*		*ND2DH*	*ND2*	*ND2D2*	*ND2D4*
A	B	A	B	A	B	A	B				
0.6	0.6	1.1	1.1	2.2	2.2	4.4	4.4	1.00	1.00	1.67	2.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND2DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.231	0.107 + 0.062*SL	0.075 + 0.070*SL	0.053 + 0.071*SL
	t_F	0.240	0.106 + 0.067*SL	0.076 + 0.075*SL	0.053 + 0.075*SL
	t_{PLH}	0.149	0.084 + 0.033*SL	0.088 + 0.032*SL	0.084 + 0.032*SL
	t_{PHL}	0.142	0.067 + 0.038*SL	0.073 + 0.036*SL	0.070 + 0.036*SL
B to Y	t_R	0.244	0.120 + 0.062*SL	0.088 + 0.070*SL	0.065 + 0.071*SL
	t_F	0.232	0.094 + 0.069*SL	0.070 + 0.075*SL	0.053 + 0.075*SL
	t_{PLH}	0.159	0.095 + 0.032*SL	0.095 + 0.032*SL	0.091 + 0.032*SL
	t_{PHL}	0.128	0.053 + 0.037*SL	0.058 + 0.036*SL	0.056 + 0.036*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

ND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.175	0.111 + 0.032*SL	0.087 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.184	0.108 + 0.038*SL	0.089 + 0.043*SL	0.055 + 0.044*SL
	t_{PLH}	0.116	0.076 + 0.020*SL	0.088 + 0.017*SL	0.084 + 0.017*SL
	t_{PHL}	0.109	0.061 + 0.024*SL	0.074 + 0.021*SL	0.071 + 0.021*SL
B to Y	t_R	0.190	0.127 + 0.031*SL	0.102 + 0.038*SL	0.065 + 0.039*SL
	t_F	0.176	0.101 + 0.038*SL	0.080 + 0.043*SL	0.055 + 0.044*SL
	t_{PLH}	0.128	0.090 + 0.019*SL	0.097 + 0.017*SL	0.092 + 0.017*SL
	t_{PHL}	0.097	0.051 + 0.023*SL	0.059 + 0.021*SL	0.057 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.144	0.114 + 0.015*SL	0.100 + 0.019*SL	0.053 + 0.019*SL
	t_F	0.147	0.109 + 0.019*SL	0.100 + 0.021*SL	0.057 + 0.022*SL
	t_{PLH}	0.096	0.073 + 0.012*SL	0.084 + 0.009*SL	0.085 + 0.009*SL
	t_{PHL}	0.086	0.059 + 0.013*SL	0.071 + 0.010*SL	0.072 + 0.010*SL
B to Y	t_R	0.160	0.131 + 0.015*SL	0.115 + 0.019*SL	0.067 + 0.019*SL
	t_F	0.139	0.102 + 0.019*SL	0.091 + 0.021*SL	0.057 + 0.022*SL
	t_{PLH}	0.110	0.089 + 0.011*SL	0.096 + 0.009*SL	0.093 + 0.009*SL
	t_{PHL}	0.074	0.050 + 0.012*SL	0.057 + 0.010*SL	0.058 + 0.010*SL

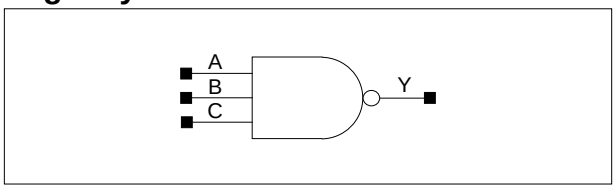
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

ND2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.126	0.110 + 0.008*SL	0.106 + 0.009*SL	0.059 + 0.010*SL
	t_F	0.123	0.102 + 0.011*SL	0.103 + 0.010*SL	0.061 + 0.011*SL
	t_{PLH}	0.082	0.068 + 0.007*SL	0.077 + 0.004*SL	0.085 + 0.004*SL
	t_{PHL}	0.070	0.055 + 0.007*SL	0.063 + 0.005*SL	0.072 + 0.005*SL
B to Y	t_R	0.143	0.129 + 0.007*SL	0.122 + 0.009*SL	0.073 + 0.010*SL
	t_F	0.118	0.098 + 0.010*SL	0.095 + 0.010*SL	0.061 + 0.011*SL
	t_{PLH}	0.097	0.085 + 0.006*SL	0.091 + 0.004*SL	0.093 + 0.004*SL
	t_{PHL}	0.060	0.047 + 0.007*SL	0.052 + 0.005*SL	0.057 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Cell Data

Input Load (SL)											
ND3DH			*ND3*			*ND3D2*			*ND3D4*		
A	B	C	A	B	C	A	B	C	A	B	C
0.6	0.6	0.6	1.0	1.1	1.1	2.2	2.2	2.1	4.6	4.5	4.3
Gate Count											
ND3DH			*ND3*			*ND3D2*			*ND3D4*		
1.33			1.33			2.33			4.00		

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND3DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.255	0.129 + 0.063*SL	0.102 + 0.070*SL	0.083 + 0.071*SL
	t_F	0.307	0.147 + 0.080*SL	0.124 + 0.086*SL	0.107 + 0.086*SL
	t_{PLH}	0.165	0.101 + 0.032*SL	0.102 + 0.032*SL	0.099 + 0.032*SL
	t_{PHL}	0.167	0.088 + 0.040*SL	0.089 + 0.039*SL	0.087 + 0.040*SL
B to Y	t_R	0.273	0.146 + 0.064*SL	0.120 + 0.070*SL	0.102 + 0.071*SL
	t_F	0.302	0.141 + 0.081*SL	0.121 + 0.086*SL	0.107 + 0.086*SL
	t_{PLH}	0.179	0.115 + 0.032*SL	0.114 + 0.032*SL	0.112 + 0.032*SL
	t_{PHL}	0.164	0.084 + 0.040*SL	0.086 + 0.040*SL	0.085 + 0.040*SL
C to Y	t_R	0.294	0.168 + 0.063*SL	0.141 + 0.070*SL	0.120 + 0.071*SL
	t_F	0.295	0.131 + 0.082*SL	0.117 + 0.086*SL	0.107 + 0.086*SL
	t_{PLH}	0.189	0.126 + 0.032*SL	0.125 + 0.032*SL	0.123 + 0.032*SL
	t_{PHL}	0.157	0.077 + 0.040*SL	0.079 + 0.040*SL	0.079 + 0.040*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

ND3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.200	0.129 + 0.036*SL	0.107 + 0.041*SL	0.078 + 0.042*SL
	t_F	0.242	0.148 + 0.047*SL	0.129 + 0.052*SL	0.103 + 0.053*SL
	t_{PLH}	0.135	0.094 + 0.021*SL	0.100 + 0.019*SL	0.098 + 0.019*SL
	t_{PHL}	0.133	0.082 + 0.025*SL	0.088 + 0.024*SL	0.085 + 0.024*SL
B to Y	t_R	0.220	0.148 + 0.036*SL	0.126 + 0.041*SL	0.096 + 0.042*SL
	t_F	0.238	0.142 + 0.048*SL	0.125 + 0.052*SL	0.103 + 0.053*SL
	t_{PLH}	0.149	0.110 + 0.019*SL	0.112 + 0.019*SL	0.110 + 0.019*SL
	t_{PHL}	0.130	0.079 + 0.025*SL	0.084 + 0.024*SL	0.083 + 0.024*SL
C to Y	t_R	0.242	0.170 + 0.036*SL	0.148 + 0.041*SL	0.116 + 0.042*SL
	t_F	0.230	0.132 + 0.049*SL	0.119 + 0.052*SL	0.103 + 0.053*SL
	t_{PLH}	0.160	0.122 + 0.019*SL	0.123 + 0.019*SL	0.121 + 0.019*SL
	t_{PHL}	0.123	0.073 + 0.025*SL	0.077 + 0.024*SL	0.077 + 0.024*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.196	0.163 + 0.017*SL	0.147 + 0.020*SL	0.102 + 0.021*SL
	t_F	0.167	0.120 + 0.024*SL	0.109 + 0.026*SL	0.086 + 0.027*SL
	t_{PLH}	0.134	0.113 + 0.011*SL	0.117 + 0.009*SL	0.115 + 0.010*SL
	t_{PHL}	0.089	0.063 + 0.013*SL	0.067 + 0.012*SL	0.069 + 0.012*SL
B to Y	t_R	0.172	0.139 + 0.017*SL	0.124 + 0.021*SL	0.082 + 0.021*SL
	t_F	0.177	0.132 + 0.023*SL	0.118 + 0.026*SL	0.086 + 0.027*SL
	t_{PLH}	0.122	0.100 + 0.011*SL	0.106 + 0.009*SL	0.103 + 0.010*SL
	t_{PHL}	0.095	0.067 + 0.014*SL	0.074 + 0.012*SL	0.075 + 0.012*SL
C to Y	t_R	0.154	0.120 + 0.017*SL	0.105 + 0.021*SL	0.064 + 0.021*SL
	t_F	0.181	0.135 + 0.023*SL	0.123 + 0.026*SL	0.086 + 0.027*SL
	t_{PLH}	0.106	0.081 + 0.012*SL	0.092 + 0.010*SL	0.091 + 0.010*SL
	t_{PHL}	0.097	0.068 + 0.014*SL	0.078 + 0.012*SL	0.077 + 0.012*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

ND3D4

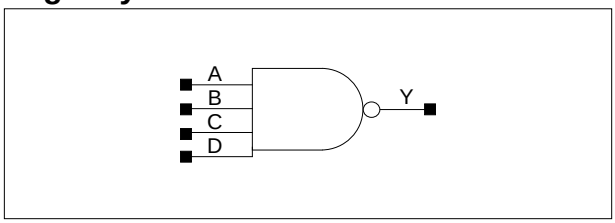
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.181	0.166 + 0.008*SL	0.157 + 0.010*SL	0.109 + 0.011*SL
	t_F	0.145	0.122 + 0.012*SL	0.116 + 0.013*SL	0.092 + 0.013*SL
	t_{PLH}	0.124	0.113 + 0.006*SL	0.116 + 0.005*SL	0.117 + 0.005*SL
	t_{PHL}	0.077	0.063 + 0.007*SL	0.066 + 0.006*SL	0.070 + 0.006*SL
B to Y	t_R	0.158	0.142 + 0.008*SL	0.134 + 0.010*SL	0.088 + 0.011*SL
	t_F	0.155	0.133 + 0.011*SL	0.126 + 0.013*SL	0.092 + 0.013*SL
	t_{PLH}	0.111	0.099 + 0.006*SL	0.104 + 0.005*SL	0.105 + 0.005*SL
	t_{PHL}	0.081	0.067 + 0.007*SL	0.071 + 0.006*SL	0.075 + 0.006*SL
C to Y	t_R	0.138	0.121 + 0.008*SL	0.115 + 0.010*SL	0.069 + 0.011*SL
	t_F	0.158	0.134 + 0.012*SL	0.132 + 0.013*SL	0.090 + 0.013*SL
	t_{PLH}	0.094	0.080 + 0.007*SL	0.087 + 0.005*SL	0.093 + 0.005*SL
	t_{PHL}	0.083	0.067 + 0.008*SL	0.074 + 0.006*SL	0.078 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

ND4DH/ND4/ND4D2/ND4D2B/ND4D4

4-Input NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Cell Data

Input Load (SL)																			
ND4DH				*ND4*				*ND4D2*				*ND4D2B*				*ND4D4*			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.6	0.6	0.6	0.6	0.9	0.9	0.9	1.0	1.8	1.9	2.0	2.0	0.7	0.7	0.8	0.8	0.7	0.7	0.7	0.7

Gate Count				
ND4DH	*ND4*	*ND4D2*	*ND4D2B*	*ND4D4*
1.67	1.67	2.67	2.67	3.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND4DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.264	0.128 + 0.068*SL	0.105 + 0.074*SL	0.089 + 0.074*SL
	t_F	0.358	0.173 + 0.093*SL	0.150 + 0.098*SL	0.138 + 0.099*SL
	t_{PLH}	0.174	0.106 + 0.034*SL	0.106 + 0.034*SL	0.105 + 0.034*SL
	t_{PHL}	0.178	0.090 + 0.044*SL	0.090 + 0.044*SL	0.087 + 0.044*SL
B to Y	t_R	0.284	0.148 + 0.068*SL	0.124 + 0.074*SL	0.109 + 0.074*SL
	t_F	0.357	0.170 + 0.094*SL	0.151 + 0.098*SL	0.138 + 0.099*SL
	t_{PLH}	0.188	0.121 + 0.033*SL	0.120 + 0.034*SL	0.118 + 0.034*SL
	t_{PHL}	0.181	0.092 + 0.044*SL	0.093 + 0.044*SL	0.092 + 0.044*SL
C to Y	t_R	0.309	0.175 + 0.067*SL	0.148 + 0.074*SL	0.131 + 0.074*SL
	t_F	0.352	0.162 + 0.095*SL	0.148 + 0.098*SL	0.138 + 0.099*SL
	t_{PLH}	0.201	0.134 + 0.034*SL	0.133 + 0.034*SL	0.132 + 0.034*SL
	t_{PHL}	0.182	0.093 + 0.045*SL	0.094 + 0.044*SL	0.095 + 0.044*SL
D to Y	t_R	0.335	0.201 + 0.067*SL	0.174 + 0.074*SL	0.153 + 0.074*SL
	t_F	0.347	0.156 + 0.096*SL	0.145 + 0.098*SL	0.138 + 0.099*SL
	t_{PLH}	0.211	0.143 + 0.034*SL	0.144 + 0.034*SL	0.146 + 0.034*SL
	t_{PHL}	0.181	0.092 + 0.045*SL	0.094 + 0.044*SL	0.095 + 0.044*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.220	0.127 + 0.046*SL	0.107 + 0.051*SL	0.085 + 0.052*SL
	t_F	0.299	0.174 + 0.063*SL	0.154 + 0.067*SL	0.135 + 0.068*SL
	t_{PLH}	0.150	0.102 + 0.024*SL	0.105 + 0.023*SL	0.104 + 0.023*SL
	t_{PHL}	0.146	0.084 + 0.031*SL	0.087 + 0.030*SL	0.084 + 0.030*SL
B to Y	t_R	0.243	0.150 + 0.046*SL	0.131 + 0.051*SL	0.108 + 0.052*SL
	t_F	0.297	0.171 + 0.063*SL	0.153 + 0.067*SL	0.135 + 0.068*SL
	t_{PLH}	0.167	0.121 + 0.023*SL	0.121 + 0.023*SL	0.119 + 0.023*SL
	t_{PHL}	0.150	0.088 + 0.031*SL	0.091 + 0.030*SL	0.091 + 0.030*SL
C to Y	t_R	0.271	0.180 + 0.045*SL	0.158 + 0.051*SL	0.133 + 0.052*SL
	t_F	0.291	0.162 + 0.064*SL	0.149 + 0.068*SL	0.135 + 0.068*SL
	t_{PLH}	0.181	0.135 + 0.023*SL	0.135 + 0.023*SL	0.134 + 0.023*SL
	t_{PHL}	0.153	0.091 + 0.031*SL	0.094 + 0.030*SL	0.095 + 0.030*SL
D to Y	t_R	0.300	0.210 + 0.045*SL	0.187 + 0.051*SL	0.158 + 0.052*SL
	t_F	0.285	0.156 + 0.065*SL	0.145 + 0.068*SL	0.135 + 0.068*SL
	t_{PLH}	0.192	0.144 + 0.024*SL	0.146 + 0.023*SL	0.148 + 0.023*SL
	t_{PHL}	0.152	0.090 + 0.031*SL	0.093 + 0.030*SL	0.094 + 0.030*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

ND4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.172	0.130 + 0.021*SL	0.112 + 0.025*SL	0.080 + 0.026*SL
	t_F	0.230	0.168 + 0.031*SL	0.156 + 0.034*SL	0.129 + 0.034*SL
	t_{PLH}	0.122	0.095 + 0.014*SL	0.103 + 0.012*SL	0.101 + 0.012*SL
	t_{PHL}	0.112	0.078 + 0.017*SL	0.084 + 0.015*SL	0.082 + 0.015*SL
B to Y	t_R	0.196	0.153 + 0.022*SL	0.137 + 0.025*SL	0.104 + 0.026*SL
	t_F	0.229	0.169 + 0.030*SL	0.154 + 0.034*SL	0.129 + 0.034*SL
	t_{PLH}	0.141	0.116 + 0.012*SL	0.119 + 0.012*SL	0.116 + 0.012*SL
	t_{PHL}	0.116	0.083 + 0.017*SL	0.089 + 0.015*SL	0.089 + 0.015*SL
C to Y	t_R	0.223	0.179 + 0.022*SL	0.164 + 0.025*SL	0.128 + 0.026*SL
	t_F	0.222	0.160 + 0.031*SL	0.149 + 0.034*SL	0.129 + 0.034*SL
	t_{PLH}	0.155	0.131 + 0.012*SL	0.133 + 0.012*SL	0.132 + 0.012*SL
	t_{PHL}	0.120	0.086 + 0.017*SL	0.092 + 0.015*SL	0.093 + 0.015*SL
D to Y	t_R	0.251	0.207 + 0.022*SL	0.193 + 0.025*SL	0.153 + 0.026*SL
	t_F	0.217	0.154 + 0.031*SL	0.143 + 0.034*SL	0.129 + 0.034*SL
	t_{PLH}	0.165	0.141 + 0.012*SL	0.142 + 0.012*SL	0.146 + 0.012*SL
	t_{PHL}	0.119	0.087 + 0.016*SL	0.090 + 0.015*SL	0.092 + 0.015*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND4D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.092	0.056 + 0.018*SL	0.050 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.081	0.048 + 0.017*SL	0.048 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.273	0.253 + 0.010*SL	0.259 + 0.009*SL	0.261 + 0.009*SL
	t_{PHL}	0.289	0.267 + 0.011*SL	0.276 + 0.009*SL	0.283 + 0.009*SL
B to Y	t_R	0.093	0.058 + 0.017*SL	0.050 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.083	0.052 + 0.015*SL	0.047 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.291	0.271 + 0.010*SL	0.277 + 0.009*SL	0.279 + 0.009*SL
	t_{PHL}	0.294	0.272 + 0.011*SL	0.281 + 0.009*SL	0.288 + 0.009*SL
C to Y	t_R	0.093	0.059 + 0.017*SL	0.050 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.083	0.052 + 0.015*SL	0.047 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.306	0.286 + 0.010*SL	0.292 + 0.009*SL	0.294 + 0.009*SL
	t_{PHL}	0.295	0.272 + 0.011*SL	0.282 + 0.009*SL	0.288 + 0.009*SL
D to Y	t_R	0.094	0.059 + 0.017*SL	0.051 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.083	0.051 + 0.016*SL	0.048 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.319	0.298 + 0.010*SL	0.304 + 0.009*SL	0.306 + 0.009*SL
	t_{PHL}	0.293	0.270 + 0.011*SL	0.280 + 0.009*SL	0.287 + 0.009*SL

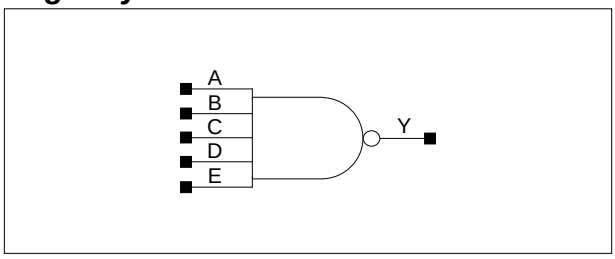
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

ND4D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.091	0.073 + 0.009*SL	0.072 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.084	0.068 + 0.008*SL	0.068 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.322	0.309 + 0.006*SL	0.316 + 0.005*SL	0.326 + 0.004*SL
	t_{PHL}	0.317	0.304 + 0.007*SL	0.312 + 0.005*SL	0.330 + 0.004*SL
B to Y	t_R	0.092	0.073 + 0.009*SL	0.073 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.084	0.068 + 0.008*SL	0.068 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.343	0.330 + 0.006*SL	0.337 + 0.005*SL	0.347 + 0.004*SL
	t_{PHL}	0.323	0.309 + 0.007*SL	0.318 + 0.005*SL	0.335 + 0.004*SL
C to Y	t_R	0.093	0.076 + 0.009*SL	0.073 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.084	0.068 + 0.008*SL	0.068 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.361	0.349 + 0.006*SL	0.356 + 0.005*SL	0.365 + 0.004*SL
	t_{PHL}	0.324	0.310 + 0.007*SL	0.319 + 0.005*SL	0.337 + 0.004*SL
D to Y	t_R	0.094	0.077 + 0.009*SL	0.074 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.084	0.068 + 0.008*SL	0.068 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.377	0.365 + 0.006*SL	0.371 + 0.005*SL	0.381 + 0.004*SL
	t_{PHL}	0.322	0.309 + 0.007*SL	0.317 + 0.005*SL	0.335 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	x	x	x	1
x	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
1	1	1	1	1	0

Cell Data

Input Load (SL)															Gate Count		
ND5					*ND5D2*					*ND5D4*					*ND5*	*ND5D2*	*ND5D4*
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E			
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	3.00	3.33	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.132	0.060 + 0.036*SL	0.051 + 0.038*SL	0.042 + 0.038*SL
	t_F	0.131	0.066 + 0.032*SL	0.064 + 0.033*SL	0.041 + 0.033*SL
	t_{PLH}	0.300	0.264 + 0.018*SL	0.267 + 0.017*SL	0.267 + 0.017*SL
	t_{PHL}	0.313	0.270 + 0.022*SL	0.285 + 0.018*SL	0.294 + 0.018*SL
B to Y	t_R	0.132	0.061 + 0.036*SL	0.051 + 0.038*SL	0.042 + 0.038*SL
	t_F	0.131	0.067 + 0.032*SL	0.064 + 0.033*SL	0.041 + 0.033*SL
	t_{PLH}	0.320	0.284 + 0.018*SL	0.287 + 0.017*SL	0.287 + 0.017*SL
	t_{PHL}	0.311	0.268 + 0.022*SL	0.282 + 0.018*SL	0.291 + 0.018*SL
C to Y	t_R	0.132	0.061 + 0.036*SL	0.052 + 0.038*SL	0.042 + 0.038*SL
	t_F	0.131	0.067 + 0.032*SL	0.064 + 0.033*SL	0.041 + 0.033*SL
	t_{PLH}	0.338	0.302 + 0.018*SL	0.305 + 0.017*SL	0.305 + 0.017*SL
	t_{PHL}	0.305	0.262 + 0.022*SL	0.276 + 0.018*SL	0.285 + 0.018*SL
D to Y	t_R	0.128	0.055 + 0.036*SL	0.048 + 0.038*SL	0.042 + 0.038*SL
	t_F	0.128	0.063 + 0.033*SL	0.062 + 0.033*SL	0.040 + 0.033*SL
	t_{PLH}	0.270	0.234 + 0.018*SL	0.237 + 0.017*SL	0.237 + 0.017*SL
	t_{PHL}	0.254	0.211 + 0.021*SL	0.225 + 0.018*SL	0.234 + 0.018*SL
E to Y	t_R	0.128	0.055 + 0.036*SL	0.048 + 0.038*SL	0.042 + 0.038*SL
	t_F	0.129	0.064 + 0.032*SL	0.062 + 0.033*SL	0.040 + 0.034*SL
	t_{PLH}	0.291	0.255 + 0.018*SL	0.258 + 0.017*SL	0.258 + 0.017*SL
	t_{PHL}	0.247	0.204 + 0.021*SL	0.218 + 0.018*SL	0.227 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.096	0.062 + 0.017*SL	0.052 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.105	0.071 + 0.017*SL	0.073 + 0.016*SL	0.043 + 0.017*SL
	t_{PLH}	0.299	0.278 + 0.010*SL	0.284 + 0.009*SL	0.286 + 0.009*SL
	t_{PHL}	0.325	0.298 + 0.013*SL	0.314 + 0.009*SL	0.337 + 0.009*SL
B to Y	t_R	0.096	0.062 + 0.017*SL	0.053 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.105	0.072 + 0.017*SL	0.072 + 0.016*SL	0.042 + 0.017*SL
	t_{PLH}	0.319	0.299 + 0.010*SL	0.305 + 0.009*SL	0.307 + 0.009*SL
	t_{PHL}	0.322	0.296 + 0.013*SL	0.312 + 0.009*SL	0.335 + 0.009*SL
C to Y	t_R	0.096	0.060 + 0.018*SL	0.054 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.105	0.070 + 0.017*SL	0.073 + 0.016*SL	0.043 + 0.017*SL
	t_{PLH}	0.337	0.317 + 0.010*SL	0.323 + 0.009*SL	0.325 + 0.009*SL
	t_{PHL}	0.316	0.290 + 0.013*SL	0.306 + 0.009*SL	0.329 + 0.009*SL
D to Y	t_R	0.091	0.056 + 0.017*SL	0.048 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.103	0.069 + 0.017*SL	0.072 + 0.016*SL	0.042 + 0.017*SL
	t_{PLH}	0.270	0.249 + 0.010*SL	0.255 + 0.009*SL	0.257 + 0.009*SL
	t_{PHL}	0.264	0.238 + 0.013*SL	0.254 + 0.009*SL	0.277 + 0.009*SL
E to Y	t_R	0.091	0.056 + 0.017*SL	0.049 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.103	0.069 + 0.017*SL	0.072 + 0.016*SL	0.042 + 0.017*SL
	t_{PLH}	0.291	0.271 + 0.010*SL	0.277 + 0.009*SL	0.278 + 0.009*SL
	t_{PHL}	0.257	0.231 + 0.013*SL	0.247 + 0.009*SL	0.270 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND5D4

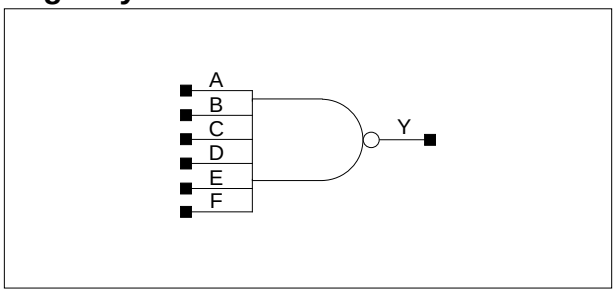
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.093	0.076 + 0.009*SL	0.073 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.123	0.104 + 0.009*SL	0.109 + 0.008*SL	0.094 + 0.008*SL
	t_{PLH}	0.329	0.317 + 0.006*SL	0.324 + 0.004*SL	0.333 + 0.004*SL
	t_{PHL}	0.390	0.373 + 0.008*SL	0.386 + 0.005*SL	0.430 + 0.004*SL
B to Y	t_R	0.094	0.077 + 0.009*SL	0.074 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.122	0.103 + 0.009*SL	0.109 + 0.008*SL	0.094 + 0.008*SL
	t_{PLH}	0.350	0.338 + 0.006*SL	0.345 + 0.004*SL	0.354 + 0.004*SL
	t_{PHL}	0.388	0.371 + 0.008*SL	0.384 + 0.005*SL	0.428 + 0.004*SL
C to Y	t_R	0.093	0.076 + 0.009*SL	0.074 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.122	0.104 + 0.009*SL	0.109 + 0.008*SL	0.093 + 0.008*SL
	t_{PLH}	0.369	0.356 + 0.006*SL	0.363 + 0.004*SL	0.372 + 0.004*SL
	t_{PHL}	0.382	0.365 + 0.008*SL	0.377 + 0.005*SL	0.422 + 0.004*SL
D to Y	t_R	0.088	0.071 + 0.009*SL	0.068 + 0.009*SL	0.044 + 0.010*SL
	t_F	0.121	0.102 + 0.009*SL	0.108 + 0.008*SL	0.093 + 0.008*SL
	t_{PLH}	0.301	0.288 + 0.006*SL	0.295 + 0.004*SL	0.304 + 0.004*SL
	t_{PHL}	0.328	0.312 + 0.008*SL	0.324 + 0.005*SL	0.369 + 0.004*SL
E to Y	t_R	0.088	0.071 + 0.009*SL	0.068 + 0.009*SL	0.044 + 0.010*SL
	t_F	0.121	0.103 + 0.009*SL	0.108 + 0.008*SL	0.093 + 0.008*SL
	t_{PLH}	0.322	0.310 + 0.006*SL	0.317 + 0.004*SL	0.325 + 0.004*SL
	t_{PHL}	0.321	0.305 + 0.008*SL	0.317 + 0.005*SL	0.362 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

ND6/ND6D2/ND6D4

6-Input NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	1	1	1	0
Other States						1

Cell Data

Input Load (SL)																	
ND6						*ND6D2*						*ND6D4*					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7

Gate Count		
ND6	*ND6D2*	*ND6D4*
3.33	3.67	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.132	0.060 + 0.036*SL	0.051 + 0.038*SL	0.042 + 0.038*SL
	t_F	0.129	0.065 + 0.032*SL	0.064 + 0.032*SL	0.041 + 0.033*SL
	t_{PLH}	0.300	0.264 + 0.018*SL	0.267 + 0.017*SL	0.267 + 0.017*SL
	t_{PHL}	0.313	0.270 + 0.021*SL	0.285 + 0.018*SL	0.295 + 0.017*SL
B to Y	t_R	0.131	0.060 + 0.036*SL	0.051 + 0.038*SL	0.042 + 0.038*SL
	t_F	0.129	0.066 + 0.032*SL	0.064 + 0.032*SL	0.041 + 0.033*SL
	t_{PLH}	0.320	0.284 + 0.018*SL	0.287 + 0.017*SL	0.287 + 0.017*SL
	t_{PHL}	0.310	0.268 + 0.021*SL	0.282 + 0.018*SL	0.292 + 0.017*SL
C to Y	t_R	0.133	0.062 + 0.035*SL	0.051 + 0.038*SL	0.042 + 0.038*SL
	t_F	0.128	0.064 + 0.032*SL	0.064 + 0.032*SL	0.041 + 0.033*SL
	t_{PLH}	0.338	0.302 + 0.018*SL	0.305 + 0.017*SL	0.305 + 0.017*SL
	t_{PHL}	0.304	0.262 + 0.021*SL	0.276 + 0.018*SL	0.286 + 0.017*SL
D to Y	t_R	0.128	0.056 + 0.036*SL	0.048 + 0.038*SL	0.042 + 0.038*SL
	t_F	0.129	0.065 + 0.032*SL	0.064 + 0.032*SL	0.041 + 0.033*SL
	t_{PLH}	0.282	0.246 + 0.018*SL	0.249 + 0.017*SL	0.249 + 0.017*SL
	t_{PHL}	0.297	0.254 + 0.021*SL	0.269 + 0.018*SL	0.278 + 0.017*SL
E to Y	t_R	0.129	0.056 + 0.036*SL	0.049 + 0.038*SL	0.042 + 0.038*SL
	t_F	0.127	0.063 + 0.032*SL	0.063 + 0.032*SL	0.041 + 0.033*SL
	t_{PLH}	0.301	0.265 + 0.018*SL	0.268 + 0.017*SL	0.268 + 0.017*SL
	t_{PHL}	0.295	0.253 + 0.021*SL	0.267 + 0.018*SL	0.277 + 0.017*SL
F to Y	t_R	0.129	0.056 + 0.036*SL	0.049 + 0.038*SL	0.042 + 0.038*SL
	t_F	0.127	0.064 + 0.032*SL	0.063 + 0.032*SL	0.041 + 0.033*SL
	t_{PLH}	0.317	0.281 + 0.018*SL	0.284 + 0.017*SL	0.284 + 0.017*SL
	t_{PHL}	0.287	0.245 + 0.021*SL	0.259 + 0.018*SL	0.269 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.095	0.059 + 0.018*SL	0.053 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.105	0.071 + 0.017*SL	0.074 + 0.016*SL	0.043 + 0.017*SL
	t_{PLH}	0.299	0.278 + 0.010*SL	0.285 + 0.009*SL	0.287 + 0.009*SL
	t_{PHL}	0.326	0.300 + 0.013*SL	0.315 + 0.009*SL	0.339 + 0.009*SL
B to Y	t_R	0.096	0.062 + 0.017*SL	0.053 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.105	0.072 + 0.017*SL	0.073 + 0.016*SL	0.043 + 0.017*SL
	t_{PLH}	0.319	0.299 + 0.010*SL	0.305 + 0.009*SL	0.307 + 0.009*SL
	t_{PHL}	0.324	0.298 + 0.013*SL	0.313 + 0.009*SL	0.337 + 0.009*SL
C to Y	t_R	0.097	0.063 + 0.017*SL	0.054 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.105	0.071 + 0.017*SL	0.073 + 0.016*SL	0.043 + 0.017*SL
	t_{PLH}	0.338	0.317 + 0.010*SL	0.323 + 0.009*SL	0.325 + 0.009*SL
	t_{PHL}	0.318	0.292 + 0.013*SL	0.307 + 0.009*SL	0.331 + 0.009*SL
D to Y	t_R	0.090	0.054 + 0.018*SL	0.049 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.104	0.070 + 0.017*SL	0.073 + 0.016*SL	0.043 + 0.017*SL
	t_{PLH}	0.282	0.261 + 0.010*SL	0.267 + 0.009*SL	0.269 + 0.009*SL
	t_{PHL}	0.310	0.284 + 0.013*SL	0.299 + 0.009*SL	0.323 + 0.009*SL
E to Y	t_R	0.092	0.057 + 0.017*SL	0.049 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.104	0.071 + 0.017*SL	0.072 + 0.016*SL	0.043 + 0.017*SL
	t_{PLH}	0.302	0.281 + 0.010*SL	0.287 + 0.009*SL	0.289 + 0.009*SL
	t_{PHL}	0.308	0.282 + 0.013*SL	0.297 + 0.009*SL	0.321 + 0.009*SL
F to Y	t_R	0.093	0.058 + 0.017*SL	0.050 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.104	0.070 + 0.017*SL	0.073 + 0.016*SL	0.043 + 0.017*SL
	t_{PLH}	0.318	0.298 + 0.010*SL	0.304 + 0.009*SL	0.306 + 0.009*SL
	t_{PHL}	0.301	0.274 + 0.013*SL	0.290 + 0.009*SL	0.313 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND6D4

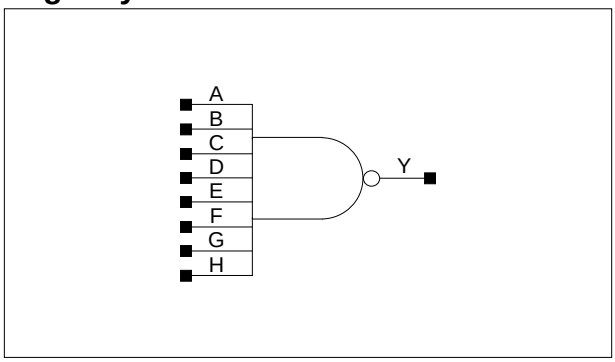
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.093	0.076 + 0.008*SL	0.073 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.123	0.105 + 0.009*SL	0.110 + 0.008*SL	0.095 + 0.008*SL
	t_{PLH}	0.331	0.319 + 0.006*SL	0.325 + 0.005*SL	0.335 + 0.004*SL
	t_{PHL}	0.393	0.377 + 0.008*SL	0.389 + 0.005*SL	0.434 + 0.004*SL
B to Y	t_R	0.094	0.076 + 0.009*SL	0.074 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.123	0.105 + 0.009*SL	0.109 + 0.008*SL	0.095 + 0.008*SL
	t_{PLH}	0.352	0.339 + 0.006*SL	0.346 + 0.004*SL	0.355 + 0.004*SL
	t_{PHL}	0.391	0.374 + 0.008*SL	0.387 + 0.005*SL	0.432 + 0.004*SL
C to Y	t_R	0.094	0.076 + 0.009*SL	0.074 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.122	0.103 + 0.009*SL	0.109 + 0.008*SL	0.095 + 0.008*SL
	t_{PLH}	0.370	0.358 + 0.006*SL	0.365 + 0.004*SL	0.374 + 0.004*SL
	t_{PHL}	0.385	0.369 + 0.008*SL	0.381 + 0.005*SL	0.426 + 0.004*SL
D to Y	t_R	0.089	0.072 + 0.009*SL	0.069 + 0.009*SL	0.044 + 0.010*SL
	t_F	0.122	0.103 + 0.009*SL	0.109 + 0.008*SL	0.094 + 0.008*SL
	t_{PLH}	0.314	0.302 + 0.006*SL	0.309 + 0.004*SL	0.318 + 0.004*SL
	t_{PHL}	0.375	0.359 + 0.008*SL	0.371 + 0.005*SL	0.416 + 0.004*SL
E to Y	t_R	0.089	0.072 + 0.008*SL	0.068 + 0.009*SL	0.044 + 0.010*SL
	t_F	0.123	0.105 + 0.009*SL	0.109 + 0.008*SL	0.094 + 0.008*SL
	t_{PLH}	0.335	0.322 + 0.006*SL	0.329 + 0.004*SL	0.338 + 0.004*SL
	t_{PHL}	0.374	0.357 + 0.008*SL	0.370 + 0.005*SL	0.414 + 0.004*SL
F to Y	t_R	0.089	0.071 + 0.009*SL	0.070 + 0.009*SL	0.044 + 0.010*SL
	t_F	0.122	0.103 + 0.010*SL	0.109 + 0.008*SL	0.094 + 0.008*SL
	t_{PLH}	0.352	0.340 + 0.006*SL	0.346 + 0.004*SL	0.355 + 0.004*SL
	t_{PHL}	0.367	0.350 + 0.008*SL	0.363 + 0.005*SL	0.407 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

ND8/ND8D2/ND8D4

8-Input NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	1	1	1	1	1	1	0
Other States								1

Cell Data

Input Load (SL)								Gate Count
ND8								*ND8*
A	B	C	D	E	F	G	H	
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	4.00
ND8D2								*ND8D2*
A	B	C	D	E	F	G	H	
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	4.33
ND8D4								*ND8D4*
A	B	C	D	E	F	G	H	
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	4.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.136	0.065 + 0.036*SL	0.055 + 0.038*SL	0.046 + 0.038*SL
	t_F	0.133	0.070 + 0.032*SL	0.068 + 0.032*SL	0.045 + 0.033*SL
	t_{PLH}	0.328	0.292 + 0.018*SL	0.295 + 0.017*SL	0.295 + 0.017*SL
	t_{PHL}	0.309	0.267 + 0.021*SL	0.281 + 0.018*SL	0.291 + 0.017*SL
B to Y	t_R	0.137	0.065 + 0.036*SL	0.057 + 0.038*SL	0.046 + 0.038*SL
	t_F	0.133	0.071 + 0.031*SL	0.068 + 0.032*SL	0.045 + 0.033*SL
	t_{PLH}	0.361	0.325 + 0.018*SL	0.328 + 0.017*SL	0.328 + 0.017*SL
	t_{PHL}	0.318	0.276 + 0.021*SL	0.290 + 0.018*SL	0.300 + 0.017*SL
C to Y	t_R	0.139	0.068 + 0.035*SL	0.057 + 0.038*SL	0.047 + 0.038*SL
	t_F	0.133	0.070 + 0.032*SL	0.068 + 0.032*SL	0.045 + 0.033*SL
	t_{PLH}	0.389	0.353 + 0.018*SL	0.356 + 0.017*SL	0.356 + 0.017*SL
	t_{PHL}	0.322	0.280 + 0.021*SL	0.294 + 0.018*SL	0.304 + 0.017*SL
D to Y	t_R	0.139	0.069 + 0.035*SL	0.058 + 0.038*SL	0.047 + 0.038*SL
	t_F	0.132	0.068 + 0.032*SL	0.068 + 0.032*SL	0.045 + 0.033*SL
	t_{PLH}	0.414	0.378 + 0.018*SL	0.380 + 0.017*SL	0.380 + 0.017*SL
	t_{PHL}	0.322	0.280 + 0.021*SL	0.294 + 0.018*SL	0.304 + 0.017*SL
E to Y	t_R	0.133	0.061 + 0.036*SL	0.052 + 0.038*SL	0.046 + 0.038*SL
	t_F	0.133	0.069 + 0.032*SL	0.068 + 0.032*SL	0.045 + 0.033*SL
	t_{PLH}	0.309	0.273 + 0.018*SL	0.276 + 0.017*SL	0.276 + 0.017*SL
	t_{PHL}	0.298	0.256 + 0.021*SL	0.270 + 0.018*SL	0.280 + 0.017*SL
F to Y	t_R	0.134	0.062 + 0.036*SL	0.053 + 0.038*SL	0.046 + 0.038*SL
	t_F	0.132	0.069 + 0.032*SL	0.067 + 0.032*SL	0.045 + 0.033*SL
	t_{PLH}	0.340	0.304 + 0.018*SL	0.307 + 0.017*SL	0.307 + 0.017*SL
	t_{PHL}	0.308	0.266 + 0.021*SL	0.280 + 0.018*SL	0.290 + 0.017*SL
G to Y	t_R	0.135	0.064 + 0.036*SL	0.054 + 0.038*SL	0.046 + 0.038*SL
	t_F	0.132	0.068 + 0.032*SL	0.067 + 0.032*SL	0.045 + 0.033*SL
	t_{PLH}	0.367	0.331 + 0.018*SL	0.334 + 0.017*SL	0.334 + 0.017*SL
	t_{PHL}	0.311	0.269 + 0.021*SL	0.283 + 0.018*SL	0.293 + 0.017*SL
H to Y	t_R	0.136	0.065 + 0.035*SL	0.055 + 0.038*SL	0.046 + 0.038*SL
	t_F	0.132	0.067 + 0.032*SL	0.067 + 0.032*SL	0.045 + 0.033*SL
	t_{PLH}	0.389	0.354 + 0.018*SL	0.356 + 0.017*SL	0.356 + 0.017*SL
	t_{PHL}	0.310	0.268 + 0.021*SL	0.281 + 0.018*SL	0.291 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.098	0.065 + 0.017*SL	0.056 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.107	0.074 + 0.017*SL	0.077 + 0.016*SL	0.046 + 0.016*SL
	t_{PLH}	0.327	0.306 + 0.010*SL	0.313 + 0.009*SL	0.315 + 0.009*SL
	t_{PHL}	0.322	0.296 + 0.013*SL	0.311 + 0.009*SL	0.336 + 0.009*SL
B to Y	t_R	0.099	0.065 + 0.017*SL	0.057 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.107	0.074 + 0.016*SL	0.076 + 0.016*SL	0.046 + 0.016*SL
	t_{PLH}	0.361	0.340 + 0.010*SL	0.346 + 0.009*SL	0.348 + 0.009*SL
	t_{PHL}	0.331	0.305 + 0.013*SL	0.320 + 0.009*SL	0.345 + 0.009*SL
C to Y	t_R	0.101	0.067 + 0.017*SL	0.059 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.107	0.075 + 0.016*SL	0.076 + 0.016*SL	0.046 + 0.016*SL
	t_{PLH}	0.389	0.369 + 0.010*SL	0.375 + 0.009*SL	0.377 + 0.009*SL
	t_{PHL}	0.334	0.309 + 0.013*SL	0.324 + 0.009*SL	0.348 + 0.009*SL
D to Y	t_R	0.102	0.069 + 0.017*SL	0.059 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.107	0.074 + 0.017*SL	0.077 + 0.016*SL	0.046 + 0.016*SL
	t_{PLH}	0.415	0.394 + 0.010*SL	0.401 + 0.009*SL	0.402 + 0.009*SL
	t_{PHL}	0.334	0.308 + 0.013*SL	0.324 + 0.009*SL	0.348 + 0.009*SL
E to Y	t_R	0.093	0.058 + 0.018*SL	0.052 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.106	0.074 + 0.016*SL	0.075 + 0.016*SL	0.046 + 0.016*SL
	t_{PLH}	0.309	0.289 + 0.010*SL	0.295 + 0.009*SL	0.297 + 0.009*SL
	t_{PHL}	0.311	0.286 + 0.013*SL	0.301 + 0.009*SL	0.325 + 0.009*SL
F to Y	t_R	0.095	0.061 + 0.017*SL	0.052 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.107	0.074 + 0.017*SL	0.077 + 0.016*SL	0.046 + 0.016*SL
	t_{PLH}	0.341	0.321 + 0.010*SL	0.327 + 0.009*SL	0.329 + 0.009*SL
	t_{PHL}	0.321	0.295 + 0.013*SL	0.310 + 0.009*SL	0.335 + 0.009*SL
G to Y	t_R	0.096	0.062 + 0.017*SL	0.055 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.107	0.074 + 0.017*SL	0.076 + 0.016*SL	0.046 + 0.016*SL
	t_{PLH}	0.369	0.349 + 0.010*SL	0.354 + 0.009*SL	0.356 + 0.009*SL
	t_{PHL}	0.324	0.299 + 0.013*SL	0.314 + 0.009*SL	0.338 + 0.009*SL
H to Y	t_R	0.098	0.064 + 0.017*SL	0.055 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.107	0.073 + 0.017*SL	0.076 + 0.016*SL	0.046 + 0.016*SL
	t_{PLH}	0.392	0.372 + 0.010*SL	0.378 + 0.009*SL	0.380 + 0.009*SL
	t_{PHL}	0.323	0.297 + 0.013*SL	0.312 + 0.009*SL	0.336 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

ND8D4

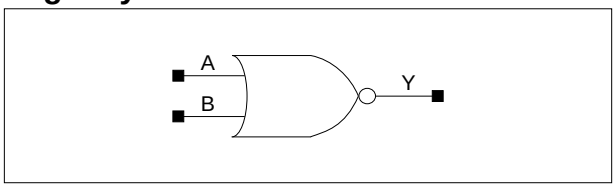
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.096	0.079 + 0.009*SL	0.076 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.124	0.105 + 0.010*SL	0.111 + 0.008*SL	0.095 + 0.008*SL
	t_{PLH}	0.357	0.345 + 0.006*SL	0.352 + 0.004*SL	0.361 + 0.004*SL
	t_{PHL}	0.387	0.370 + 0.008*SL	0.383 + 0.005*SL	0.427 + 0.004*SL
B to Y	t_R	0.095	0.078 + 0.009*SL	0.076 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.125	0.106 + 0.009*SL	0.111 + 0.008*SL	0.095 + 0.008*SL
	t_{PLH}	0.391	0.379 + 0.006*SL	0.386 + 0.004*SL	0.395 + 0.004*SL
	t_{PHL}	0.396	0.379 + 0.008*SL	0.392 + 0.005*SL	0.436 + 0.004*SL
C to Y	t_R	0.098	0.081 + 0.008*SL	0.077 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.125	0.107 + 0.009*SL	0.111 + 0.008*SL	0.095 + 0.008*SL
	t_{PLH}	0.421	0.409 + 0.006*SL	0.416 + 0.004*SL	0.425 + 0.004*SL
	t_{PHL}	0.400	0.383 + 0.008*SL	0.396 + 0.005*SL	0.440 + 0.004*SL
D to Y	t_R	0.099	0.083 + 0.008*SL	0.079 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.125	0.107 + 0.009*SL	0.111 + 0.008*SL	0.095 + 0.008*SL
	t_{PLH}	0.448	0.435 + 0.006*SL	0.442 + 0.004*SL	0.451 + 0.004*SL
	t_{PHL}	0.399	0.383 + 0.008*SL	0.395 + 0.005*SL	0.440 + 0.004*SL
E to Y	t_R	0.090	0.072 + 0.009*SL	0.070 + 0.009*SL	0.045 + 0.010*SL
	t_F	0.123	0.104 + 0.010*SL	0.111 + 0.008*SL	0.095 + 0.008*SL
	t_{PLH}	0.341	0.329 + 0.006*SL	0.335 + 0.004*SL	0.344 + 0.004*SL
	t_{PHL}	0.377	0.361 + 0.008*SL	0.373 + 0.005*SL	0.417 + 0.004*SL
F to Y	t_R	0.091	0.074 + 0.009*SL	0.071 + 0.009*SL	0.045 + 0.010*SL
	t_F	0.123	0.104 + 0.009*SL	0.111 + 0.008*SL	0.095 + 0.008*SL
	t_{PLH}	0.374	0.361 + 0.006*SL	0.368 + 0.004*SL	0.377 + 0.004*SL
	t_{PHL}	0.386	0.370 + 0.008*SL	0.382 + 0.005*SL	0.426 + 0.004*SL
G to Y	t_R	0.092	0.074 + 0.009*SL	0.072 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.123	0.104 + 0.010*SL	0.111 + 0.008*SL	0.095 + 0.008*SL
	t_{PLH}	0.402	0.390 + 0.006*SL	0.397 + 0.004*SL	0.405 + 0.004*SL
	t_{PHL}	0.389	0.373 + 0.008*SL	0.385 + 0.005*SL	0.429 + 0.004*SL
H to Y	t_R	0.094	0.077 + 0.009*SL	0.074 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.124	0.105 + 0.010*SL	0.111 + 0.008*SL	0.095 + 0.008*SL
	t_{PLH}	0.427	0.415 + 0.006*SL	0.422 + 0.004*SL	0.431 + 0.004*SL
	t_{PHL}	0.388	0.371 + 0.008*SL	0.384 + 0.005*SL	0.428 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NR2DH/NR2/NR2D2/NR2D2B/NR2D4

2-Input NOR with 0.5X/1X/2X/2X(Buffered)/4X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Cell Data

Input Load (SL)									
NR2DH		*NR2*		*NR2D2*		*NR2D2B*		*NR2D4*	
A	B	A	B	A	B	A	B	A	B
0.5	0.6	1.0	1.0	2.1	2.1	0.7	0.7	0.7	0.7

Gate Count				
NR2DH	*NR2*	*NR2D2*	*NR2D2B*	*NR2D4*
1.00	1.00	1.67	2.33	2.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR2DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.394	0.136 + 0.129*SL	0.112 + 0.135*SL	0.105 + 0.135*SL
	t_F	0.174	0.088 + 0.043*SL	0.062 + 0.050*SL	0.030 + 0.051*SL
	t_{PLH}	0.223	0.107 + 0.058*SL	0.100 + 0.060*SL	0.095 + 0.060*SL
	t_{PHL}	0.110	0.048 + 0.031*SL	0.064 + 0.027*SL	0.063 + 0.027*SL
B to Y	t_R	0.391	0.130 + 0.130*SL	0.112 + 0.135*SL	0.105 + 0.135*SL
	t_F	0.198	0.113 + 0.042*SL	0.084 + 0.050*SL	0.050 + 0.051*SL
	t_{PLH}	0.223	0.104 + 0.059*SL	0.101 + 0.060*SL	0.100 + 0.060*SL
	t_{PHL}	0.125	0.066 + 0.029*SL	0.076 + 0.027*SL	0.076 + 0.027*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

NR2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.277	0.141 + 0.068*SL	0.122 + 0.073*SL	0.104 + 0.073*SL
	t_F	0.138	0.087 + 0.026*SL	0.073 + 0.029*SL	0.032 + 0.030*SL
	t_{PLH}	0.166	0.103 + 0.032*SL	0.100 + 0.032*SL	0.094 + 0.032*SL
	t_{PHL}	0.086	0.044 + 0.021*SL	0.063 + 0.016*SL	0.064 + 0.016*SL
B to Y	t_R	0.273	0.136 + 0.069*SL	0.119 + 0.073*SL	0.104 + 0.073*SL
	t_F	0.169	0.119 + 0.025*SL	0.103 + 0.029*SL	0.056 + 0.030*SL
	t_{PLH}	0.166	0.102 + 0.032*SL	0.102 + 0.032*SL	0.100 + 0.032*SL
	t_{PHL}	0.105	0.066 + 0.019*SL	0.079 + 0.016*SL	0.080 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.212	0.146 + 0.033*SL	0.133 + 0.036*SL	0.106 + 0.037*SL
	t_F	0.111	0.083 + 0.014*SL	0.082 + 0.014*SL	0.033 + 0.015*SL
	t_{PLH}	0.134	0.100 + 0.017*SL	0.103 + 0.016*SL	0.095 + 0.016*SL
	t_{PHL}	0.064	0.040 + 0.012*SL	0.056 + 0.008*SL	0.065 + 0.008*SL
B to Y	t_R	0.207	0.141 + 0.033*SL	0.128 + 0.036*SL	0.106 + 0.037*SL
	t_F	0.144	0.118 + 0.013*SL	0.112 + 0.014*SL	0.057 + 0.015*SL
	t_{PLH}	0.134	0.100 + 0.017*SL	0.104 + 0.016*SL	0.101 + 0.016*SL
	t_{PHL}	0.085	0.063 + 0.011*SL	0.075 + 0.008*SL	0.080 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NR2D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.094	0.060 + 0.017*SL	0.051 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.074	0.040 + 0.017*SL	0.041 + 0.017*SL	0.024 + 0.017*SL
	t_{PLH}	0.314	0.293 + 0.010*SL	0.299 + 0.009*SL	0.301 + 0.009*SL
	t_{PHL}	0.198	0.176 + 0.011*SL	0.184 + 0.009*SL	0.190 + 0.009*SL
B to Y	t_R	0.094	0.060 + 0.017*SL	0.052 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.077	0.045 + 0.016*SL	0.041 + 0.017*SL	0.023 + 0.017*SL
	t_{PLH}	0.316	0.295 + 0.010*SL	0.302 + 0.009*SL	0.304 + 0.009*SL
	t_{PHL}	0.218	0.195 + 0.011*SL	0.204 + 0.009*SL	0.210 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NR2D4

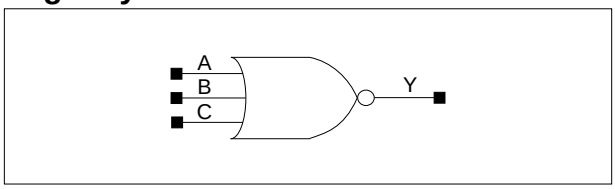
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.093	0.077 + 0.008*SL	0.073 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.076	0.059 + 0.009*SL	0.061 + 0.008*SL	0.041 + 0.008*SL
	t_{PLH}	0.352	0.340 + 0.006*SL	0.347 + 0.005*SL	0.357 + 0.004*SL
	t_{PHL}	0.229	0.215 + 0.007*SL	0.224 + 0.005*SL	0.241 + 0.004*SL
B to Y	t_R	0.093	0.077 + 0.008*SL	0.073 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.076	0.057 + 0.009*SL	0.062 + 0.008*SL	0.041 + 0.008*SL
	t_{PLH}	0.351	0.338 + 0.006*SL	0.345 + 0.005*SL	0.355 + 0.004*SL
	t_{PHL}	0.247	0.233 + 0.007*SL	0.242 + 0.005*SL	0.259 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NR3DH/NR3/NR3D2/NR3D2B/NR3D4

3-Input NOR with 0.5X/1X/2X/2X(Buffered)/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	1
Other States			0

Cell Data

Input Load (SL)														
NR3DH			*NR3*			*NR3D2*			*NR3D2B*			*NR3D4*		
A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
0.5	0.5	0.5	1.0	1.0	1.0	2.0	2.0	1.9	0.7	0.7	0.8	0.7	0.7	0.8
Gate Count														
NR3DH			*NR3*			*NR3D2*			*NR3D2B*			*NR3D4*		
1.33			1.33			2.00			2.33			3.00		

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR3DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.618	0.224 + 0.197*SL	0.208 + 0.201*SL	0.210 + 0.201*SL
	t_F	0.191	0.094 + 0.049*SL	0.067 + 0.055*SL	0.041 + 0.056*SL
	t_{PLH}	0.299	0.126 + 0.087*SL	0.119 + 0.088*SL	0.114 + 0.089*SL
	t_{PHL}	0.127	0.062 + 0.033*SL	0.073 + 0.030*SL	0.071 + 0.030*SL
B to Y	t_R	0.624	0.231 + 0.196*SL	0.214 + 0.200*SL	0.210 + 0.201*SL
	t_F	0.216	0.120 + 0.048*SL	0.091 + 0.055*SL	0.064 + 0.056*SL
	t_{PLH}	0.325	0.149 + 0.088*SL	0.148 + 0.089*SL	0.149 + 0.089*SL
	t_{PHL}	0.145	0.081 + 0.032*SL	0.088 + 0.030*SL	0.088 + 0.030*SL
C to Y	t_R	0.620	0.226 + 0.197*SL	0.213 + 0.200*SL	0.210 + 0.201*SL
	t_F	0.239	0.140 + 0.049*SL	0.117 + 0.055*SL	0.087 + 0.056*SL
	t_{PLH}	0.335	0.158 + 0.089*SL	0.158 + 0.089*SL	0.161 + 0.089*SL
	t_{PHL}	0.152	0.088 + 0.032*SL	0.096 + 0.030*SL	0.102 + 0.030*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.434	0.227 + 0.104*SL	0.209 + 0.108*SL	0.206 + 0.108*SL
	t_F	0.156	0.095 + 0.030*SL	0.078 + 0.035*SL	0.044 + 0.036*SL
	t_{PLH}	0.213	0.121 + 0.046*SL	0.114 + 0.048*SL	0.108 + 0.048*SL
	t_{PHL}	0.105	0.060 + 0.022*SL	0.075 + 0.019*SL	0.074 + 0.019*SL
B to Y	t_R	0.441	0.232 + 0.105*SL	0.217 + 0.108*SL	0.206 + 0.108*SL
	t_F	0.188	0.129 + 0.030*SL	0.110 + 0.034*SL	0.073 + 0.036*SL
	t_{PLH}	0.240	0.145 + 0.048*SL	0.145 + 0.048*SL	0.145 + 0.048*SL
	t_{PHL}	0.127	0.085 + 0.021*SL	0.094 + 0.019*SL	0.095 + 0.019*SL
C to Y	t_R	0.437	0.227 + 0.105*SL	0.214 + 0.108*SL	0.205 + 0.108*SL
	t_F	0.217	0.155 + 0.031*SL	0.141 + 0.034*SL	0.105 + 0.035*SL
	t_{PLH}	0.252	0.156 + 0.048*SL	0.157 + 0.048*SL	0.160 + 0.048*SL
	t_{PHL}	0.136	0.094 + 0.021*SL	0.102 + 0.019*SL	0.111 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

NR3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.324	0.222 + 0.051*SL	0.210 + 0.054*SL	0.199 + 0.054*SL
	t_F	0.120	0.087 + 0.017*SL	0.085 + 0.017*SL	0.041 + 0.018*SL
	t_{PLH}	0.163	0.118 + 0.022*SL	0.112 + 0.024*SL	0.104 + 0.024*SL
	t_{PHL}	0.080	0.053 + 0.013*SL	0.068 + 0.009*SL	0.073 + 0.009*SL
B to Y	t_R	0.332	0.230 + 0.051*SL	0.217 + 0.054*SL	0.199 + 0.054*SL
	t_F	0.156	0.126 + 0.015*SL	0.118 + 0.017*SL	0.071 + 0.018*SL
	t_{PLH}	0.189	0.139 + 0.025*SL	0.142 + 0.024*SL	0.143 + 0.024*SL
	t_{PHL}	0.104	0.081 + 0.012*SL	0.090 + 0.009*SL	0.094 + 0.009*SL
C to Y	t_R	0.327	0.224 + 0.052*SL	0.213 + 0.054*SL	0.199 + 0.054*SL
	t_F	0.185	0.154 + 0.015*SL	0.146 + 0.017*SL	0.103 + 0.018*SL
	t_{PLH}	0.200	0.151 + 0.025*SL	0.154 + 0.024*SL	0.157 + 0.024*SL
	t_{PHL}	0.113	0.089 + 0.012*SL	0.099 + 0.010*SL	0.110 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR3D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.102	0.068 + 0.017*SL	0.059 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.078	0.045 + 0.017*SL	0.046 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.372	0.351 + 0.010*SL	0.357 + 0.009*SL	0.359 + 0.009*SL
	t_{PHL}	0.220	0.199 + 0.011*SL	0.207 + 0.009*SL	0.212 + 0.009*SL
B to Y	t_R	0.102	0.068 + 0.017*SL	0.059 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.078	0.045 + 0.016*SL	0.046 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.396	0.376 + 0.010*SL	0.382 + 0.009*SL	0.384 + 0.009*SL
	t_{PHL}	0.242	0.220 + 0.011*SL	0.229 + 0.009*SL	0.234 + 0.009*SL
C to Y	t_R	0.102	0.067 + 0.017*SL	0.060 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.081	0.050 + 0.016*SL	0.047 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.408	0.387 + 0.010*SL	0.394 + 0.009*SL	0.395 + 0.009*SL
	t_{PHL}	0.253	0.231 + 0.011*SL	0.240 + 0.009*SL	0.246 + 0.009*SL

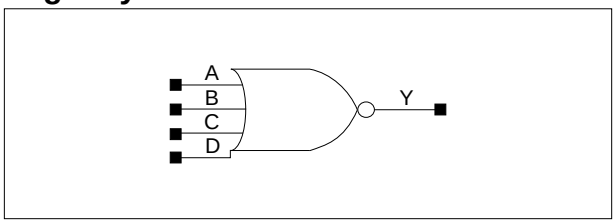
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NR3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.087 + 0.008*SL	0.083 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.079	0.062 + 0.009*SL	0.065 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.420	0.407 + 0.006*SL	0.414 + 0.004*SL	0.425 + 0.004*SL
	t_{PHL}	0.254	0.241 + 0.007*SL	0.249 + 0.005*SL	0.266 + 0.004*SL
B to Y	t_R	0.104	0.087 + 0.008*SL	0.083 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.080	0.064 + 0.008*SL	0.065 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.444	0.432 + 0.006*SL	0.439 + 0.004*SL	0.449 + 0.004*SL
	t_{PHL}	0.276	0.263 + 0.007*SL	0.271 + 0.005*SL	0.288 + 0.004*SL
C to Y	t_R	0.104	0.088 + 0.008*SL	0.084 + 0.009*SL	0.054 + 0.010*SL
	t_F	0.081	0.066 + 0.008*SL	0.066 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.456	0.443 + 0.006*SL	0.450 + 0.004*SL	0.461 + 0.004*SL
	t_{PHL}	0.288	0.275 + 0.007*SL	0.283 + 0.005*SL	0.301 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	0	1
Other States				0

Cell Data

Input Load (SL)																			
NR4DH				*NR4*				*NR4D2*				*NR4D2B*				*NR4D4*			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.5	0.5	0.5	0.5	0.9	0.9	0.9	0.9	1.8	1.8	1.9	2.0	0.8	0.8	0.8	0.8	0.8	0.7	0.7	0.8

Gate Count				
NR4DH	*NR4*	*NR4D2*	*NR4D2B*	*NR4D4*
1.67	1.67	2.67	2.67	3.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR4DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.850	0.319 + 0.265*SL	0.314 + 0.267*SL	0.327 + 0.266*SL
	t_F	0.198	0.094 + 0.052*SL	0.068 + 0.059*SL	0.044 + 0.059*SL
	t_{PLH}	0.355	0.125 + 0.115*SL	0.116 + 0.117*SL	0.112 + 0.117*SL
	t_{PHL}	0.135	0.067 + 0.034*SL	0.076 + 0.032*SL	0.074 + 0.032*SL
B to Y	t_R	0.870	0.345 + 0.263*SL	0.330 + 0.266*SL	0.327 + 0.266*SL
	t_F	0.225	0.120 + 0.052*SL	0.094 + 0.059*SL	0.069 + 0.059*SL
	t_{PLH}	0.411	0.175 + 0.118*SL	0.176 + 0.118*SL	0.180 + 0.118*SL
	t_{PHL}	0.155	0.089 + 0.033*SL	0.094 + 0.032*SL	0.095 + 0.032*SL
C to Y	t_R	0.871	0.347 + 0.262*SL	0.331 + 0.266*SL	0.327 + 0.266*SL
	t_F	0.252	0.145 + 0.053*SL	0.124 + 0.059*SL	0.097 + 0.059*SL
	t_{PLH}	0.455	0.217 + 0.119*SL	0.221 + 0.118*SL	0.227 + 0.118*SL
	t_{PHL}	0.165	0.097 + 0.034*SL	0.105 + 0.032*SL	0.113 + 0.032*SL
D to Y	t_R	0.870	0.344 + 0.263*SL	0.331 + 0.266*SL	0.327 + 0.266*SL
	t_F	0.270	0.160 + 0.055*SL	0.146 + 0.059*SL	0.126 + 0.059*SL
	t_{PLH}	0.471	0.233 + 0.119*SL	0.238 + 0.118*SL	0.243 + 0.118*SL
	t_{PHL}	0.167	0.097 + 0.035*SL	0.108 + 0.032*SL	0.127 + 0.032*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.596	0.314 + 0.141*SL	0.300 + 0.144*SL	0.318 + 0.144*SL
	t_F	0.167	0.096 + 0.036*SL	0.077 + 0.040*SL	0.049 + 0.041*SL
	t_{PLH}	0.237	0.118 + 0.059*SL	0.103 + 0.063*SL	0.098 + 0.063*SL
	t_{PHL}	0.119	0.070 + 0.024*SL	0.081 + 0.022*SL	0.080 + 0.022*SL
B to Y	t_R	0.622	0.341 + 0.140*SL	0.327 + 0.144*SL	0.318 + 0.144*SL
	t_F	0.203	0.132 + 0.036*SL	0.114 + 0.040*SL	0.084 + 0.041*SL
	t_{PLH}	0.292	0.164 + 0.064*SL	0.166 + 0.063*SL	0.170 + 0.063*SL
	t_{PHL}	0.146	0.100 + 0.023*SL	0.106 + 0.022*SL	0.107 + 0.022*SL
C to Y	t_R	0.625	0.347 + 0.139*SL	0.328 + 0.144*SL	0.318 + 0.144*SL
	t_F	0.240	0.167 + 0.037*SL	0.153 + 0.040*SL	0.124 + 0.041*SL
	t_{PLH}	0.340	0.211 + 0.065*SL	0.215 + 0.063*SL	0.222 + 0.063*SL
	t_{PHL}	0.160	0.112 + 0.024*SL	0.119 + 0.022*SL	0.131 + 0.022*SL
D to Y	t_R	0.622	0.343 + 0.140*SL	0.327 + 0.144*SL	0.318 + 0.144*SL
	t_F	0.266	0.188 + 0.039*SL	0.183 + 0.040*SL	0.166 + 0.041*SL
	t_{PLH}	0.359	0.229 + 0.065*SL	0.234 + 0.063*SL	0.240 + 0.063*SL
	t_{PHL}	0.162	0.112 + 0.025*SL	0.122 + 0.023*SL	0.147 + 0.022*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

NR4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.421	0.281 + 0.070*SL	0.271 + 0.072*SL	0.281 + 0.072*SL
	t_F	0.123	0.087 + 0.018*SL	0.080 + 0.020*SL	0.041 + 0.021*SL
	t_{PLH}	0.169	0.114 + 0.027*SL	0.098 + 0.031*SL	0.088 + 0.032*SL
	t_{PHL}	0.086	0.057 + 0.014*SL	0.071 + 0.011*SL	0.075 + 0.011*SL
B to Y	t_R	0.447	0.309 + 0.069*SL	0.297 + 0.072*SL	0.282 + 0.072*SL
	t_F	0.161	0.127 + 0.017*SL	0.115 + 0.020*SL	0.075 + 0.021*SL
	t_{PLH}	0.215	0.150 + 0.032*SL	0.153 + 0.032*SL	0.157 + 0.032*SL
	t_{PHL}	0.115	0.088 + 0.013*SL	0.097 + 0.011*SL	0.101 + 0.011*SL
C to Y	t_R	0.452	0.317 + 0.068*SL	0.301 + 0.072*SL	0.282 + 0.072*SL
	t_F	0.195	0.159 + 0.018*SL	0.150 + 0.020*SL	0.112 + 0.020*SL
	t_{PLH}	0.257	0.190 + 0.033*SL	0.196 + 0.032*SL	0.204 + 0.032*SL
	t_{PHL}	0.127	0.100 + 0.013*SL	0.109 + 0.011*SL	0.123 + 0.011*SL
D to Y	t_R	0.448	0.312 + 0.068*SL	0.297 + 0.072*SL	0.282 + 0.072*SL
	t_F	0.218	0.180 + 0.019*SL	0.176 + 0.020*SL	0.154 + 0.020*SL
	t_{PLH}	0.277	0.211 + 0.033*SL	0.217 + 0.032*SL	0.226 + 0.032*SL
	t_{PHL}	0.129	0.102 + 0.014*SL	0.112 + 0.011*SL	0.140 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR4D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.106	0.072 + 0.017*SL	0.063 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.081	0.050 + 0.016*SL	0.046 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.500	0.479 + 0.010*SL	0.486 + 0.009*SL	0.488 + 0.009*SL
	t_{PHL}	0.273	0.251 + 0.011*SL	0.260 + 0.009*SL	0.266 + 0.009*SL
B to Y	t_R	0.105	0.071 + 0.017*SL	0.064 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.080	0.048 + 0.016*SL	0.046 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.481	0.460 + 0.010*SL	0.467 + 0.009*SL	0.469 + 0.009*SL
	t_{PHL}	0.268	0.246 + 0.011*SL	0.255 + 0.009*SL	0.261 + 0.009*SL
C to Y	t_R	0.106	0.073 + 0.017*SL	0.063 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.079	0.047 + 0.016*SL	0.046 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.439	0.418 + 0.010*SL	0.425 + 0.009*SL	0.427 + 0.009*SL
	t_{PHL}	0.254	0.232 + 0.011*SL	0.241 + 0.009*SL	0.246 + 0.009*SL
D to Y	t_R	0.105	0.072 + 0.017*SL	0.063 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.079	0.046 + 0.016*SL	0.046 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.387	0.366 + 0.010*SL	0.374 + 0.009*SL	0.375 + 0.009*SL
	t_{PHL}	0.227	0.205 + 0.011*SL	0.214 + 0.009*SL	0.219 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NR4D4

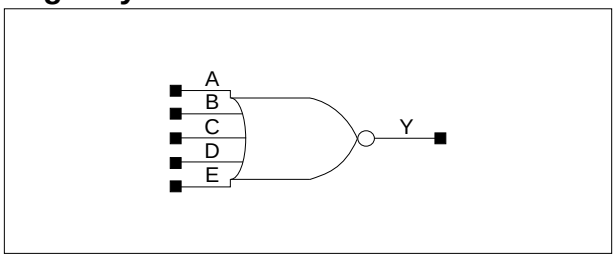
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.111	0.095 + 0.008*SL	0.090 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.078	0.062 + 0.008*SL	0.061 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.521	0.508 + 0.007*SL	0.516 + 0.005*SL	0.528 + 0.004*SL
	t_{PHL}	0.226	0.212 + 0.007*SL	0.220 + 0.005*SL	0.237 + 0.004*SL
B to Y	t_R	0.111	0.094 + 0.008*SL	0.091 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.078	0.060 + 0.009*SL	0.063 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.567	0.554 + 0.007*SL	0.563 + 0.005*SL	0.574 + 0.004*SL
	t_{PHL}	0.241	0.228 + 0.007*SL	0.236 + 0.005*SL	0.253 + 0.004*SL
C to Y	t_R	0.111	0.095 + 0.008*SL	0.091 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.079	0.063 + 0.008*SL	0.062 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.605	0.592 + 0.007*SL	0.600 + 0.005*SL	0.612 + 0.004*SL
	t_{PHL}	0.249	0.236 + 0.007*SL	0.244 + 0.005*SL	0.261 + 0.004*SL
D to Y	t_R	0.110	0.094 + 0.008*SL	0.091 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.079	0.061 + 0.009*SL	0.064 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.623	0.609 + 0.007*SL	0.618 + 0.005*SL	0.629 + 0.004*SL
	t_{PHL}	0.251	0.238 + 0.007*SL	0.246 + 0.005*SL	0.263 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NR5/NR5D2/NR5D4

5-Input NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	1
Other States					0

Cell Data

Input Load (SL)															Gate Count		
NR5					*NR5D2*					*NR5D4*					*NR5*	*NR5D2*	*NR5D4*
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E			
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	3.00	3.33	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.145	0.073 + 0.036*SL	0.064 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.112	0.047 + 0.032*SL	0.043 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.412	0.374 + 0.019*SL	0.381 + 0.017*SL	0.383 + 0.017*SL
	t_{PHL}	0.225	0.187 + 0.019*SL	0.192 + 0.018*SL	0.194 + 0.018*SL
B to Y	t_R	0.145	0.073 + 0.036*SL	0.064 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.113	0.050 + 0.032*SL	0.043 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.436	0.397 + 0.019*SL	0.405 + 0.017*SL	0.407 + 0.017*SL
	t_{PHL}	0.244	0.205 + 0.019*SL	0.211 + 0.018*SL	0.213 + 0.018*SL
C to Y	t_R	0.146	0.074 + 0.036*SL	0.065 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.113	0.048 + 0.032*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.445	0.407 + 0.019*SL	0.414 + 0.018*SL	0.416 + 0.017*SL
	t_{PHL}	0.253	0.214 + 0.019*SL	0.220 + 0.018*SL	0.222 + 0.018*SL
D to Y	t_R	0.141	0.069 + 0.036*SL	0.061 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.114	0.050 + 0.032*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.328	0.289 + 0.019*SL	0.296 + 0.017*SL	0.298 + 0.017*SL
	t_{PHL}	0.223	0.184 + 0.019*SL	0.191 + 0.018*SL	0.193 + 0.018*SL
E to Y	t_R	0.142	0.069 + 0.036*SL	0.061 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.115	0.052 + 0.031*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.327	0.289 + 0.019*SL	0.296 + 0.017*SL	0.298 + 0.017*SL
	t_{PHL}	0.242	0.204 + 0.019*SL	0.210 + 0.018*SL	0.212 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.110	0.074 + 0.018*SL	0.070 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.078	0.045 + 0.017*SL	0.045 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.421	0.399 + 0.011*SL	0.408 + 0.009*SL	0.417 + 0.009*SL
	t_{PHL}	0.222	0.199 + 0.011*SL	0.208 + 0.009*SL	0.215 + 0.009*SL
B to Y	t_R	0.110	0.074 + 0.018*SL	0.070 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.078	0.044 + 0.017*SL	0.045 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.445	0.423 + 0.011*SL	0.432 + 0.009*SL	0.441 + 0.009*SL
	t_{PHL}	0.240	0.218 + 0.011*SL	0.227 + 0.009*SL	0.234 + 0.009*SL
C to Y	t_R	0.110	0.073 + 0.018*SL	0.070 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.079	0.045 + 0.017*SL	0.046 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.455	0.432 + 0.011*SL	0.442 + 0.009*SL	0.451 + 0.009*SL
	t_{PHL}	0.249	0.227 + 0.011*SL	0.236 + 0.009*SL	0.243 + 0.009*SL
D to Y	t_R	0.105	0.069 + 0.018*SL	0.064 + 0.019*SL	0.039 + 0.019*SL
	t_F	0.080	0.047 + 0.017*SL	0.048 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.330	0.307 + 0.011*SL	0.317 + 0.009*SL	0.326 + 0.009*SL
	t_{PHL}	0.218	0.195 + 0.011*SL	0.205 + 0.009*SL	0.212 + 0.009*SL
E to Y	t_R	0.105	0.069 + 0.018*SL	0.065 + 0.019*SL	0.039 + 0.019*SL
	t_F	0.082	0.051 + 0.016*SL	0.047 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.331	0.308 + 0.011*SL	0.318 + 0.009*SL	0.327 + 0.009*SL
	t_{PHL}	0.237	0.214 + 0.012*SL	0.225 + 0.009*SL	0.232 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR5D4

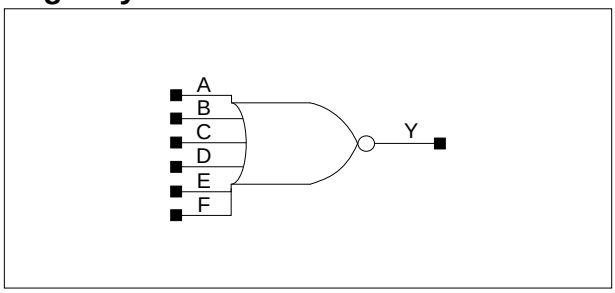
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.116	0.098 + 0.009*SL	0.096 + 0.009*SL	0.071 + 0.010*SL
	t_F	0.079	0.062 + 0.008*SL	0.063 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.472	0.458 + 0.007*SL	0.468 + 0.005*SL	0.491 + 0.004*SL
	t_{PHL}	0.254	0.241 + 0.007*SL	0.249 + 0.005*SL	0.268 + 0.004*SL
B to Y	t_R	0.116	0.099 + 0.008*SL	0.096 + 0.009*SL	0.071 + 0.010*SL
	t_F	0.079	0.063 + 0.008*SL	0.063 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.497	0.483 + 0.007*SL	0.492 + 0.005*SL	0.515 + 0.004*SL
	t_{PHL}	0.273	0.259 + 0.007*SL	0.268 + 0.005*SL	0.286 + 0.004*SL
C to Y	t_R	0.115	0.099 + 0.008*SL	0.095 + 0.009*SL	0.071 + 0.010*SL
	t_F	0.079	0.062 + 0.009*SL	0.065 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.506	0.492 + 0.007*SL	0.502 + 0.005*SL	0.525 + 0.004*SL
	t_{PHL}	0.282	0.269 + 0.007*SL	0.277 + 0.005*SL	0.296 + 0.004*SL
D to Y	t_R	0.109	0.092 + 0.009*SL	0.089 + 0.009*SL	0.068 + 0.010*SL
	t_F	0.083	0.066 + 0.008*SL	0.067 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.371	0.357 + 0.007*SL	0.367 + 0.005*SL	0.390 + 0.004*SL
	t_{PHL}	0.248	0.234 + 0.007*SL	0.243 + 0.005*SL	0.263 + 0.004*SL
E to Y	t_R	0.109	0.091 + 0.009*SL	0.090 + 0.009*SL	0.068 + 0.010*SL
	t_F	0.082	0.065 + 0.009*SL	0.068 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.371	0.357 + 0.007*SL	0.366 + 0.005*SL	0.390 + 0.004*SL
	t_{PHL}	0.267	0.253 + 0.007*SL	0.262 + 0.005*SL	0.282 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NR6/NR6D2/NR6D4

6-Input NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	0	0	0	1
Other States						0

Cell Data

Input Load (SL)																	
NR6						*NR6D2*						*NR6D4*					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7

Gate Count		
NR6	*NR6D2*	*NR6D4*
3.33	3.67	4.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.146	0.074 + 0.036*SL	0.066 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.113	0.049 + 0.032*SL	0.044 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.415	0.376 + 0.019*SL	0.383 + 0.017*SL	0.385 + 0.017*SL
	t_{PHL}	0.227	0.189 + 0.019*SL	0.194 + 0.018*SL	0.196 + 0.018*SL
B to Y	t_R	0.147	0.075 + 0.036*SL	0.066 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.114	0.051 + 0.032*SL	0.044 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.439	0.400 + 0.019*SL	0.407 + 0.017*SL	0.410 + 0.017*SL
	t_{PHL}	0.246	0.207 + 0.019*SL	0.213 + 0.018*SL	0.215 + 0.018*SL
C to Y	t_R	0.147	0.075 + 0.036*SL	0.066 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.113	0.049 + 0.032*SL	0.045 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.448	0.409 + 0.019*SL	0.417 + 0.018*SL	0.419 + 0.017*SL
	t_{PHL}	0.254	0.216 + 0.019*SL	0.222 + 0.018*SL	0.223 + 0.018*SL
D to Y	t_R	0.147	0.076 + 0.036*SL	0.066 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.115	0.052 + 0.032*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.394	0.355 + 0.020*SL	0.364 + 0.018*SL	0.366 + 0.017*SL
	t_{PHL}	0.233	0.195 + 0.019*SL	0.201 + 0.018*SL	0.203 + 0.018*SL
E to Y	t_R	0.148	0.076 + 0.036*SL	0.066 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.116	0.054 + 0.031*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.419	0.380 + 0.020*SL	0.388 + 0.018*SL	0.390 + 0.017*SL
	t_{PHL}	0.253	0.214 + 0.019*SL	0.220 + 0.018*SL	0.222 + 0.018*SL
F to Y	t_R	0.147	0.076 + 0.036*SL	0.066 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.431	0.391 + 0.020*SL	0.400 + 0.018*SL	0.402 + 0.017*SL
	t_{PHL}	0.262	0.223 + 0.019*SL	0.230 + 0.018*SL	0.232 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.110	0.074 + 0.018*SL	0.070 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.078	0.045 + 0.016*SL	0.044 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.422	0.399 + 0.011*SL	0.409 + 0.009*SL	0.418 + 0.009*SL
	t_{PHL}	0.222	0.199 + 0.011*SL	0.209 + 0.009*SL	0.215 + 0.009*SL
B to Y	t_R	0.110	0.074 + 0.018*SL	0.070 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.079	0.047 + 0.016*SL	0.045 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.446	0.423 + 0.011*SL	0.433 + 0.009*SL	0.442 + 0.009*SL
	t_{PHL}	0.241	0.218 + 0.011*SL	0.227 + 0.009*SL	0.234 + 0.009*SL
C to Y	t_R	0.110	0.075 + 0.018*SL	0.070 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.078	0.044 + 0.017*SL	0.045 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.455	0.432 + 0.011*SL	0.442 + 0.009*SL	0.451 + 0.009*SL
	t_{PHL}	0.250	0.227 + 0.011*SL	0.236 + 0.009*SL	0.243 + 0.009*SL
D to Y	t_R	0.109	0.073 + 0.018*SL	0.069 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.081	0.048 + 0.017*SL	0.048 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.397	0.375 + 0.011*SL	0.385 + 0.009*SL	0.394 + 0.009*SL
	t_{PHL}	0.227	0.204 + 0.012*SL	0.214 + 0.009*SL	0.221 + 0.009*SL
E to Y	t_R	0.109	0.073 + 0.018*SL	0.069 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.081	0.048 + 0.017*SL	0.048 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.421	0.398 + 0.011*SL	0.409 + 0.009*SL	0.418 + 0.009*SL
	t_{PHL}	0.246	0.223 + 0.012*SL	0.234 + 0.009*SL	0.241 + 0.009*SL
F to Y	t_R	0.109	0.073 + 0.018*SL	0.069 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.083	0.050 + 0.016*SL	0.049 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.433	0.411 + 0.011*SL	0.421 + 0.009*SL	0.431 + 0.009*SL
	t_{PHL}	0.257	0.234 + 0.012*SL	0.244 + 0.009*SL	0.251 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR6D4

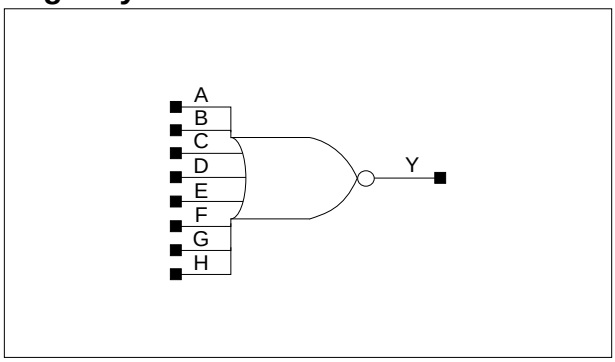
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.116	0.099 + 0.008*SL	0.096 + 0.009*SL	0.071 + 0.010*SL
	t_F	0.079	0.062 + 0.008*SL	0.063 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.474	0.459 + 0.007*SL	0.469 + 0.005*SL	0.492 + 0.004*SL
	t_{PHL}	0.255	0.241 + 0.007*SL	0.249 + 0.005*SL	0.268 + 0.004*SL
B to Y	t_R	0.116	0.099 + 0.008*SL	0.096 + 0.009*SL	0.071 + 0.010*SL
	t_F	0.079	0.063 + 0.008*SL	0.063 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.498	0.483 + 0.007*SL	0.493 + 0.005*SL	0.516 + 0.004*SL
	t_{PHL}	0.273	0.260 + 0.007*SL	0.268 + 0.005*SL	0.287 + 0.004*SL
C to Y	t_R	0.115	0.098 + 0.008*SL	0.096 + 0.009*SL	0.071 + 0.010*SL
	t_F	0.079	0.062 + 0.009*SL	0.065 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.507	0.493 + 0.007*SL	0.502 + 0.005*SL	0.526 + 0.004*SL
	t_{PHL}	0.283	0.269 + 0.007*SL	0.278 + 0.005*SL	0.296 + 0.004*SL
D to Y	t_R	0.113	0.096 + 0.008*SL	0.093 + 0.009*SL	0.071 + 0.010*SL
	t_F	0.082	0.065 + 0.009*SL	0.068 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.442	0.427 + 0.007*SL	0.437 + 0.005*SL	0.462 + 0.004*SL
	t_{PHL}	0.258	0.244 + 0.007*SL	0.253 + 0.005*SL	0.273 + 0.004*SL
E to Y	t_R	0.114	0.096 + 0.009*SL	0.094 + 0.009*SL	0.071 + 0.010*SL
	t_F	0.083	0.067 + 0.008*SL	0.068 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.466	0.452 + 0.007*SL	0.462 + 0.005*SL	0.486 + 0.004*SL
	t_{PHL}	0.277	0.263 + 0.007*SL	0.273 + 0.005*SL	0.293 + 0.004*SL
F to Y	t_R	0.114	0.096 + 0.009*SL	0.094 + 0.009*SL	0.071 + 0.010*SL
	t_F	0.084	0.066 + 0.009*SL	0.069 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.478	0.464 + 0.007*SL	0.474 + 0.005*SL	0.498 + 0.004*SL
	t_{PHL}	0.288	0.274 + 0.007*SL	0.283 + 0.005*SL	0.303 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NR8/NR8D2/NR8D4

8-Input NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	0	0	0	0	0	0	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
NR8								*NR8*
A	B	C	D	E	F	G	H	
0.6	0.7	0.7	0.7	0.7	0.7	0.7	0.7	4.00
NR8D2								*NR8D2*
A	B	C	D	E	F	G	H	
0.6	0.7	0.7	0.7	0.7	0.7	0.7	0.7	4.33
NR8D4								*NR8D4*
A	B	C	D	E	F	G	H	
0.6	0.7	0.7	0.7	0.7	0.7	0.7	0.7	5.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.152	0.081 + 0.035*SL	0.070 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.113	0.049 + 0.032*SL	0.044 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.465	0.426 + 0.020*SL	0.434 + 0.018*SL	0.437 + 0.017*SL
	t_{PHL}	0.228	0.190 + 0.019*SL	0.195 + 0.018*SL	0.197 + 0.018*SL
B to Y	t_R	0.152	0.081 + 0.035*SL	0.070 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.114	0.051 + 0.032*SL	0.044 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.516	0.477 + 0.020*SL	0.485 + 0.018*SL	0.487 + 0.017*SL
	t_{PHL}	0.248	0.210 + 0.019*SL	0.216 + 0.018*SL	0.217 + 0.018*SL
C to Y	t_R	0.152	0.081 + 0.035*SL	0.070 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.114	0.052 + 0.031*SL	0.044 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.556	0.517 + 0.020*SL	0.525 + 0.018*SL	0.528 + 0.017*SL
	t_{PHL}	0.258	0.220 + 0.019*SL	0.225 + 0.018*SL	0.227 + 0.018*SL
D to Y	t_R	0.152	0.082 + 0.035*SL	0.070 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.113	0.049 + 0.032*SL	0.045 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.572	0.532 + 0.020*SL	0.541 + 0.018*SL	0.543 + 0.017*SL
	t_{PHL}	0.260	0.222 + 0.019*SL	0.228 + 0.018*SL	0.230 + 0.018*SL
E to Y	t_R	0.152	0.082 + 0.035*SL	0.071 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.115	0.052 + 0.032*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.440	0.400 + 0.020*SL	0.410 + 0.018*SL	0.413 + 0.017*SL
	t_{PHL}	0.235	0.196 + 0.019*SL	0.203 + 0.018*SL	0.205 + 0.018*SL
F to Y	t_R	0.153	0.082 + 0.035*SL	0.071 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.115	0.052 + 0.032*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.489	0.449 + 0.020*SL	0.459 + 0.018*SL	0.462 + 0.017*SL
	t_{PHL}	0.255	0.216 + 0.019*SL	0.223 + 0.018*SL	0.225 + 0.018*SL
G to Y	t_R	0.152	0.080 + 0.036*SL	0.071 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.117	0.055 + 0.031*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.528	0.488 + 0.020*SL	0.497 + 0.018*SL	0.500 + 0.017*SL
	t_{PHL}	0.265	0.226 + 0.019*SL	0.233 + 0.018*SL	0.235 + 0.018*SL
H to Y	t_R	0.152	0.080 + 0.036*SL	0.071 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.118	0.055 + 0.031*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.544	0.504 + 0.020*SL	0.514 + 0.018*SL	0.517 + 0.017*SL
	t_{PHL}	0.268	0.229 + 0.019*SL	0.236 + 0.018*SL	0.238 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.116	0.080 + 0.018*SL	0.075 + 0.019*SL	0.042 + 0.019*SL
	t_F	0.077	0.043 + 0.017*SL	0.045 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.476	0.453 + 0.011*SL	0.463 + 0.009*SL	0.472 + 0.009*SL
	t_{PHL}	0.223	0.201 + 0.011*SL	0.210 + 0.009*SL	0.217 + 0.009*SL
B to Y	t_R	0.116	0.080 + 0.018*SL	0.075 + 0.019*SL	0.042 + 0.019*SL
	t_F	0.078	0.046 + 0.016*SL	0.044 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.526	0.503 + 0.011*SL	0.514 + 0.009*SL	0.523 + 0.009*SL
	t_{PHL}	0.244	0.221 + 0.011*SL	0.230 + 0.009*SL	0.237 + 0.009*SL
C to Y	t_R	0.116	0.080 + 0.018*SL	0.075 + 0.019*SL	0.042 + 0.019*SL
	t_F	0.080	0.048 + 0.016*SL	0.045 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.567	0.544 + 0.011*SL	0.554 + 0.009*SL	0.563 + 0.009*SL
	t_{PHL}	0.254	0.231 + 0.011*SL	0.241 + 0.009*SL	0.247 + 0.009*SL
D to Y	t_R	0.116	0.081 + 0.018*SL	0.075 + 0.019*SL	0.042 + 0.019*SL
	t_F	0.080	0.048 + 0.016*SL	0.046 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.582	0.559 + 0.011*SL	0.570 + 0.009*SL	0.579 + 0.009*SL
	t_{PHL}	0.256	0.234 + 0.011*SL	0.243 + 0.009*SL	0.250 + 0.009*SL
E to Y	t_R	0.114	0.078 + 0.018*SL	0.074 + 0.019*SL	0.042 + 0.019*SL
	t_F	0.082	0.050 + 0.016*SL	0.047 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.443	0.420 + 0.012*SL	0.431 + 0.009*SL	0.441 + 0.009*SL
	t_{PHL}	0.228	0.205 + 0.012*SL	0.215 + 0.009*SL	0.223 + 0.009*SL
F to Y	t_R	0.114	0.079 + 0.018*SL	0.074 + 0.019*SL	0.042 + 0.019*SL
	t_F	0.081	0.047 + 0.017*SL	0.048 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.492	0.469 + 0.012*SL	0.480 + 0.009*SL	0.490 + 0.009*SL
	t_{PHL}	0.249	0.225 + 0.012*SL	0.236 + 0.009*SL	0.243 + 0.009*SL
G to Y	t_R	0.114	0.079 + 0.018*SL	0.074 + 0.019*SL	0.042 + 0.019*SL
	t_F	0.082	0.049 + 0.016*SL	0.049 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.531	0.508 + 0.012*SL	0.519 + 0.009*SL	0.529 + 0.009*SL
	t_{PHL}	0.259	0.236 + 0.012*SL	0.246 + 0.009*SL	0.253 + 0.009*SL
H to Y	t_R	0.115	0.078 + 0.018*SL	0.075 + 0.019*SL	0.042 + 0.019*SL
	t_F	0.083	0.051 + 0.016*SL	0.049 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.548	0.524 + 0.012*SL	0.536 + 0.009*SL	0.546 + 0.009*SL
	t_{PHL}	0.262	0.239 + 0.012*SL	0.250 + 0.009*SL	0.257 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NR8D4

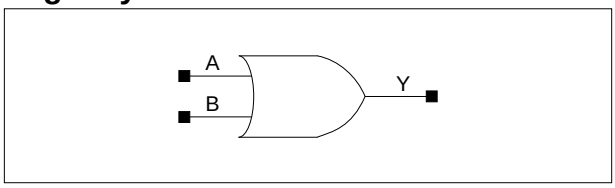
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.122	0.106 + 0.008*SL	0.102 + 0.009*SL	0.075 + 0.010*SL
	t_F	0.080	0.063 + 0.008*SL	0.063 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.534	0.519 + 0.007*SL	0.530 + 0.005*SL	0.553 + 0.004*SL
	t_{PHL}	0.257	0.243 + 0.007*SL	0.252 + 0.005*SL	0.270 + 0.004*SL
B to Y	t_R	0.122	0.105 + 0.008*SL	0.101 + 0.009*SL	0.075 + 0.010*SL
	t_F	0.079	0.061 + 0.009*SL	0.065 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.585	0.570 + 0.007*SL	0.580 + 0.005*SL	0.604 + 0.004*SL
	t_{PHL}	0.277	0.263 + 0.007*SL	0.272 + 0.005*SL	0.290 + 0.004*SL
C to Y	t_R	0.122	0.105 + 0.008*SL	0.101 + 0.009*SL	0.075 + 0.010*SL
	t_F	0.080	0.064 + 0.008*SL	0.065 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.625	0.610 + 0.007*SL	0.620 + 0.005*SL	0.644 + 0.004*SL
	t_{PHL}	0.288	0.274 + 0.007*SL	0.283 + 0.005*SL	0.301 + 0.004*SL
D to Y	t_R	0.122	0.106 + 0.008*SL	0.102 + 0.009*SL	0.075 + 0.010*SL
	t_F	0.081	0.065 + 0.008*SL	0.066 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.640	0.626 + 0.007*SL	0.636 + 0.005*SL	0.660 + 0.004*SL
	t_{PHL}	0.291	0.277 + 0.007*SL	0.286 + 0.005*SL	0.305 + 0.004*SL
E to Y	t_R	0.119	0.102 + 0.009*SL	0.099 + 0.009*SL	0.074 + 0.010*SL
	t_F	0.083	0.066 + 0.009*SL	0.068 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.489	0.475 + 0.007*SL	0.485 + 0.005*SL	0.510 + 0.004*SL
	t_{PHL}	0.259	0.245 + 0.007*SL	0.254 + 0.005*SL	0.274 + 0.004*SL
F to Y	t_R	0.119	0.102 + 0.008*SL	0.099 + 0.009*SL	0.074 + 0.010*SL
	t_F	0.083	0.067 + 0.008*SL	0.068 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.538	0.523 + 0.007*SL	0.533 + 0.005*SL	0.559 + 0.004*SL
	t_{PHL}	0.279	0.265 + 0.007*SL	0.275 + 0.005*SL	0.295 + 0.004*SL
G to Y	t_R	0.119	0.101 + 0.009*SL	0.100 + 0.009*SL	0.074 + 0.010*SL
	t_F	0.084	0.066 + 0.009*SL	0.069 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.577	0.562 + 0.007*SL	0.572 + 0.005*SL	0.597 + 0.004*SL
	t_{PHL}	0.290	0.276 + 0.007*SL	0.285 + 0.005*SL	0.306 + 0.004*SL
H to Y	t_R	0.119	0.101 + 0.009*SL	0.100 + 0.009*SL	0.074 + 0.010*SL
	t_F	0.085	0.068 + 0.008*SL	0.070 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.593	0.579 + 0.007*SL	0.589 + 0.005*SL	0.614 + 0.004*SL
	t_{PHL}	0.294	0.280 + 0.007*SL	0.290 + 0.005*SL	0.310 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OR2DH/OR2/OR2D2/OR2D4

2-Input OR with 0.5X/1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Cell Data

Input Load (SL)								Gate Count			
OR2DH		*OR2*		*OR2D2*		*OR2D4*		*OR2DH*	*OR2*	*OR2D2*	*OR2D4*
A	B	A	B	A	B	A	B				
0.4	0.5	0.7	0.7	1.0	1.1	1.0	1.1	1.33	1.33	1.67	2.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OR2DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.193	0.057 + 0.068*SL	0.047 + 0.070*SL	0.044 + 0.071*SL
	t_F	0.174	0.071 + 0.052*SL	0.062 + 0.054*SL	0.036 + 0.055*SL
	t_{PLH}	0.167	0.103 + 0.032*SL	0.103 + 0.032*SL	0.103 + 0.032*SL
	t_{PHL}	0.268	0.201 + 0.033*SL	0.217 + 0.029*SL	0.222 + 0.029*SL
B to Y	t_R	0.194	0.058 + 0.068*SL	0.048 + 0.070*SL	0.044 + 0.071*SL
	t_F	0.175	0.072 + 0.051*SL	0.062 + 0.054*SL	0.036 + 0.055*SL
	t_{PLH}	0.186	0.122 + 0.032*SL	0.122 + 0.032*SL	0.122 + 0.032*SL
	t_{PHL}	0.267	0.200 + 0.033*SL	0.217 + 0.029*SL	0.222 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

OR2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.135	0.064 + 0.036*SL	0.052 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.140	0.075 + 0.032*SL	0.073 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.142	0.106 + 0.018*SL	0.108 + 0.017*SL	0.108 + 0.017*SL
	t_{PHL}	0.256	0.212 + 0.022*SL	0.228 + 0.018*SL	0.239 + 0.018*SL
B to Y	t_R	0.137	0.065 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.141	0.076 + 0.032*SL	0.075 + 0.033*SL	0.048 + 0.033*SL
	t_{PLH}	0.162	0.125 + 0.018*SL	0.128 + 0.017*SL	0.128 + 0.017*SL
	t_{PHL}	0.257	0.213 + 0.022*SL	0.229 + 0.018*SL	0.240 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OR2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.093	0.060 + 0.017*SL	0.049 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.102	0.068 + 0.017*SL	0.070 + 0.016*SL	0.041 + 0.017*SL
	t_{PLH}	0.138	0.118 + 0.010*SL	0.124 + 0.009*SL	0.124 + 0.009*SL
	t_{PHL}	0.232	0.207 + 0.013*SL	0.221 + 0.009*SL	0.243 + 0.009*SL
B to Y	t_R	0.095	0.061 + 0.017*SL	0.053 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.103	0.070 + 0.017*SL	0.070 + 0.016*SL	0.041 + 0.017*SL
	t_{PLH}	0.161	0.141 + 0.010*SL	0.146 + 0.009*SL	0.148 + 0.009*SL
	t_{PHL}	0.235	0.209 + 0.013*SL	0.224 + 0.009*SL	0.245 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OR2D4

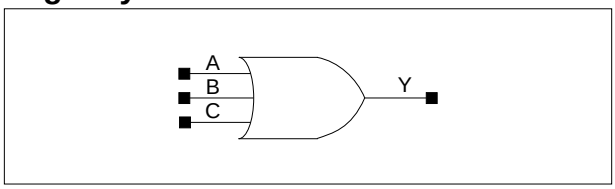
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.088	0.070 + 0.009*SL	0.068 + 0.009*SL	0.043 + 0.010*SL
	t_F	0.121	0.103 + 0.009*SL	0.107 + 0.008*SL	0.091 + 0.008*SL
	t_{PLH}	0.171	0.159 + 0.006*SL	0.166 + 0.004*SL	0.173 + 0.004*SL
	t_{PHL}	0.293	0.277 + 0.008*SL	0.289 + 0.005*SL	0.333 + 0.004*SL
B to Y	t_R	0.092	0.076 + 0.008*SL	0.070 + 0.009*SL	0.045 + 0.010*SL
	t_F	0.121	0.103 + 0.009*SL	0.107 + 0.008*SL	0.091 + 0.008*SL
	t_{PLH}	0.191	0.178 + 0.006*SL	0.185 + 0.004*SL	0.194 + 0.004*SL
	t_{PHL}	0.297	0.281 + 0.008*SL	0.293 + 0.005*SL	0.336 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OR3DH/OR3/OR3D2/OR3D4

3-Input OR with 0.5X/1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
1	x	x	1
x	1	x	1
x	x	1	1

Cell Data

Input Load (SL)											
OR3DH			*OR3*			*OR3D2*			*OR3D4*		
A	B	C	A	B	C	A	B	C	A	B	C
0.5	0.5	0.5	0.7	0.7	0.8	1.0	1.0	1.0	1.0	1.0	1.0
Gate Count											
OR3DH			*OR3*			*OR3D2*			*OR3D4*		
1.67			1.67			2.00			2.33		

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OR3DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.198	0.060 + 0.069*SL	0.049 + 0.072*SL	0.045 + 0.072*SL
	t_F	0.199	0.092 + 0.054*SL	0.093 + 0.053*SL	0.053 + 0.054*SL
	t_{PLH}	0.184	0.118 + 0.033*SL	0.119 + 0.033*SL	0.119 + 0.033*SL
	t_{PHL}	0.311	0.237 + 0.037*SL	0.266 + 0.030*SL	0.286 + 0.029*SL
B to Y	t_R	0.200	0.061 + 0.069*SL	0.050 + 0.072*SL	0.046 + 0.072*SL
	t_F	0.201	0.094 + 0.053*SL	0.095 + 0.053*SL	0.054 + 0.054*SL
	t_{PLH}	0.207	0.141 + 0.033*SL	0.142 + 0.033*SL	0.142 + 0.033*SL
	t_{PHL}	0.335	0.261 + 0.037*SL	0.291 + 0.030*SL	0.311 + 0.029*SL
C to Y	t_R	0.204	0.066 + 0.069*SL	0.055 + 0.072*SL	0.047 + 0.072*SL
	t_F	0.201	0.094 + 0.053*SL	0.094 + 0.053*SL	0.054 + 0.054*SL
	t_{PLH}	0.219	0.152 + 0.033*SL	0.154 + 0.033*SL	0.156 + 0.033*SL
	t_{PHL}	0.349	0.275 + 0.037*SL	0.304 + 0.030*SL	0.324 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

OR3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.137	0.066 + 0.036*SL	0.055 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.166	0.099 + 0.034*SL	0.103 + 0.032*SL	0.076 + 0.033*SL
	t_{PLH}	0.156	0.120 + 0.018*SL	0.123 + 0.017*SL	0.123 + 0.017*SL
	t_{PHL}	0.302	0.253 + 0.024*SL	0.277 + 0.019*SL	0.308 + 0.018*SL
B to Y	t_R	0.138	0.066 + 0.036*SL	0.057 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.168	0.101 + 0.034*SL	0.106 + 0.032*SL	0.077 + 0.033*SL
	t_{PLH}	0.178	0.141 + 0.018*SL	0.145 + 0.017*SL	0.145 + 0.017*SL
	t_{PHL}	0.326	0.278 + 0.024*SL	0.301 + 0.019*SL	0.332 + 0.018*SL
C to Y	t_R	0.143	0.072 + 0.036*SL	0.062 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.168	0.101 + 0.033*SL	0.105 + 0.032*SL	0.076 + 0.033*SL
	t_{PLH}	0.189	0.152 + 0.019*SL	0.156 + 0.018*SL	0.159 + 0.017*SL
	t_{PHL}	0.338	0.290 + 0.024*SL	0.313 + 0.019*SL	0.344 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OR3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.097	0.063 + 0.017*SL	0.055 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.134	0.098 + 0.018*SL	0.105 + 0.016*SL	0.078 + 0.017*SL
	t_{PLH}	0.161	0.140 + 0.010*SL	0.146 + 0.009*SL	0.148 + 0.009*SL
	t_{PHL}	0.289	0.259 + 0.015*SL	0.280 + 0.010*SL	0.330 + 0.009*SL
B to Y	t_R	0.101	0.066 + 0.018*SL	0.061 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.137	0.101 + 0.018*SL	0.107 + 0.016*SL	0.079 + 0.017*SL
	t_{PLH}	0.185	0.165 + 0.010*SL	0.171 + 0.009*SL	0.174 + 0.009*SL
	t_{PHL}	0.317	0.287 + 0.015*SL	0.308 + 0.010*SL	0.358 + 0.009*SL
C to Y	t_R	0.106	0.072 + 0.017*SL	0.063 + 0.019*SL	0.039 + 0.019*SL
	t_F	0.136	0.100 + 0.018*SL	0.106 + 0.016*SL	0.079 + 0.017*SL
	t_{PLH}	0.198	0.176 + 0.011*SL	0.185 + 0.009*SL	0.192 + 0.009*SL
	t_{PHL}	0.331	0.301 + 0.015*SL	0.322 + 0.010*SL	0.372 + 0.009*SL

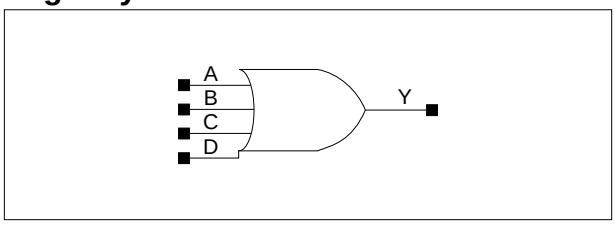
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OR3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.097	0.082 + 0.007*SL	0.075 + 0.009*SL	0.049 + 0.010*SL
	t_F	0.171	0.151 + 0.010*SL	0.158 + 0.008*SL	0.157 + 0.008*SL
	t_{PLH}	0.197	0.183 + 0.007*SL	0.192 + 0.005*SL	0.202 + 0.004*SL
	t_{PHL}	0.383	0.364 + 0.009*SL	0.379 + 0.006*SL	0.447 + 0.005*SL
B to Y	t_R	0.101	0.084 + 0.009*SL	0.081 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.171	0.150 + 0.010*SL	0.160 + 0.008*SL	0.158 + 0.008*SL
	t_{PLH}	0.221	0.208 + 0.006*SL	0.215 + 0.005*SL	0.227 + 0.004*SL
	t_{PHL}	0.414	0.395 + 0.009*SL	0.411 + 0.006*SL	0.478 + 0.005*SL
C to Y	t_R	0.106	0.089 + 0.009*SL	0.086 + 0.009*SL	0.059 + 0.010*SL
	t_F	0.171	0.150 + 0.010*SL	0.159 + 0.008*SL	0.157 + 0.008*SL
	t_{PLH}	0.235	0.222 + 0.007*SL	0.230 + 0.005*SL	0.245 + 0.004*SL
	t_{PHL}	0.429	0.410 + 0.009*SL	0.425 + 0.006*SL	0.493 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

Cell Data

Input Load (SL)															
OR4DH				*OR4*				*OR4D2*				*OR4D4*			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.5	0.5	0.5	0.5	0.8	0.8	0.8	0.8	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9

Gate Count			
OR4DH	*OR4*	*OR4D2*	*OR4D4*
2.00	2.00	2.33	2.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OR4DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.198	0.062 + 0.068*SL	0.052 + 0.070*SL	0.047 + 0.071*SL
	t_F	0.225	0.113 + 0.056*SL	0.125 + 0.053*SL	0.085 + 0.054*SL
	t_{PLH}	0.187	0.122 + 0.032*SL	0.123 + 0.032*SL	0.123 + 0.032*SL
	t_{PHL}	0.346	0.266 + 0.040*SL	0.305 + 0.030*SL	0.349 + 0.029*SL
B to Y	t_R	0.199	0.064 + 0.068*SL	0.053 + 0.070*SL	0.047 + 0.071*SL
	t_F	0.230	0.119 + 0.055*SL	0.129 + 0.053*SL	0.086 + 0.054*SL
	t_{PLH}	0.210	0.145 + 0.032*SL	0.146 + 0.032*SL	0.146 + 0.032*SL
	t_{PHL}	0.388	0.308 + 0.040*SL	0.347 + 0.030*SL	0.390 + 0.029*SL
C to Y	t_R	0.203	0.068 + 0.068*SL	0.058 + 0.070*SL	0.049 + 0.071*SL
	t_F	0.230	0.120 + 0.055*SL	0.129 + 0.053*SL	0.086 + 0.054*SL
	t_{PLH}	0.224	0.158 + 0.033*SL	0.161 + 0.032*SL	0.163 + 0.032*SL
	t_{PHL}	0.431	0.351 + 0.040*SL	0.390 + 0.030*SL	0.434 + 0.029*SL
D to Y	t_R	0.209	0.075 + 0.067*SL	0.062 + 0.070*SL	0.054 + 0.071*SL
	t_F	0.230	0.119 + 0.055*SL	0.129 + 0.053*SL	0.086 + 0.054*SL
	t_{PLH}	0.228	0.161 + 0.033*SL	0.166 + 0.032*SL	0.172 + 0.032*SL
	t_{PHL}	0.447	0.367 + 0.040*SL	0.406 + 0.030*SL	0.449 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

OR4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.139	0.067 + 0.036*SL	0.057 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.185	0.114 + 0.036*SL	0.126 + 0.033*SL	0.112 + 0.033*SL
	t_{PLH}	0.165	0.128 + 0.018*SL	0.131 + 0.017*SL	0.131 + 0.017*SL
	t_{PHL}	0.317	0.264 + 0.026*SL	0.293 + 0.019*SL	0.347 + 0.018*SL
B to Y	t_R	0.142	0.071 + 0.035*SL	0.059 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.191	0.121 + 0.035*SL	0.132 + 0.032*SL	0.114 + 0.033*SL
	t_{PLH}	0.190	0.154 + 0.018*SL	0.157 + 0.017*SL	0.157 + 0.017*SL
	t_{PHL}	0.364	0.312 + 0.026*SL	0.340 + 0.019*SL	0.394 + 0.018*SL
C to Y	t_R	0.149	0.080 + 0.035*SL	0.065 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.192	0.124 + 0.034*SL	0.132 + 0.032*SL	0.114 + 0.033*SL
	t_{PLH}	0.205	0.167 + 0.019*SL	0.173 + 0.018*SL	0.176 + 0.017*SL
	t_{PHL}	0.411	0.359 + 0.026*SL	0.387 + 0.019*SL	0.441 + 0.018*SL
D to Y	t_R	0.151	0.080 + 0.036*SL	0.070 + 0.038*SL	0.059 + 0.039*SL
	t_F	0.191	0.122 + 0.035*SL	0.131 + 0.032*SL	0.114 + 0.033*SL
	t_{PLH}	0.210	0.171 + 0.019*SL	0.178 + 0.018*SL	0.186 + 0.017*SL
	t_{PHL}	0.429	0.376 + 0.026*SL	0.404 + 0.019*SL	0.459 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OR4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.100	0.065 + 0.017*SL	0.058 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.164	0.126 + 0.019*SL	0.136 + 0.016*SL	0.125 + 0.016*SL
	t_{PLH}	0.177	0.156 + 0.011*SL	0.163 + 0.009*SL	0.166 + 0.009*SL
	t_{PHL}	0.322	0.290 + 0.016*SL	0.315 + 0.010*SL	0.396 + 0.009*SL
B to Y	t_R	0.105	0.071 + 0.017*SL	0.063 + 0.019*SL	0.037 + 0.020*SL
	t_F	0.169	0.130 + 0.019*SL	0.142 + 0.016*SL	0.127 + 0.016*SL
	t_{PLH}	0.205	0.184 + 0.011*SL	0.192 + 0.009*SL	0.195 + 0.009*SL
	t_{PHL}	0.376	0.343 + 0.016*SL	0.369 + 0.010*SL	0.449 + 0.009*SL
C to Y	t_R	0.112	0.076 + 0.018*SL	0.071 + 0.019*SL	0.042 + 0.019*SL
	t_F	0.169	0.130 + 0.019*SL	0.143 + 0.016*SL	0.127 + 0.016*SL
	t_{PLH}	0.224	0.202 + 0.011*SL	0.211 + 0.009*SL	0.219 + 0.009*SL
	t_{PHL}	0.426	0.393 + 0.016*SL	0.418 + 0.010*SL	0.499 + 0.009*SL
D to Y	t_R	0.117	0.082 + 0.017*SL	0.075 + 0.019*SL	0.051 + 0.019*SL
	t_F	0.170	0.132 + 0.019*SL	0.142 + 0.016*SL	0.127 + 0.016*SL
	t_{PLH}	0.231	0.208 + 0.012*SL	0.218 + 0.009*SL	0.233 + 0.009*SL
	t_{PHL}	0.443	0.411 + 0.016*SL	0.436 + 0.010*SL	0.516 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OR4D4

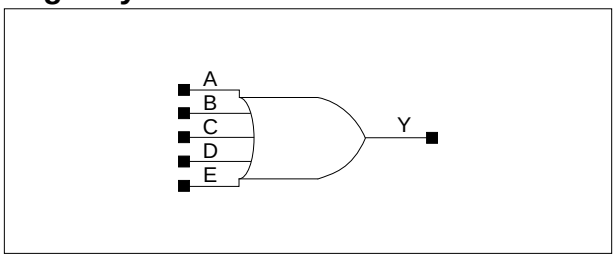
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.101	0.083 + 0.009*SL	0.081 + 0.009*SL	0.054 + 0.010*SL
	t_F	0.216	0.193 + 0.011*SL	0.206 + 0.008*SL	0.220 + 0.008*SL
	t_{PLH}	0.218	0.205 + 0.006*SL	0.212 + 0.005*SL	0.226 + 0.004*SL
	t_{PHL}	0.448	0.427 + 0.010*SL	0.445 + 0.006*SL	0.530 + 0.005*SL
B to Y	t_R	0.108	0.091 + 0.008*SL	0.088 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.218	0.195 + 0.011*SL	0.207 + 0.008*SL	0.222 + 0.008*SL
	t_{PLH}	0.246	0.232 + 0.007*SL	0.241 + 0.005*SL	0.255 + 0.004*SL
	t_{PHL}	0.506	0.485 + 0.010*SL	0.503 + 0.006*SL	0.587 + 0.005*SL
C to Y	t_R	0.117	0.099 + 0.009*SL	0.097 + 0.009*SL	0.066 + 0.010*SL
	t_F	0.217	0.195 + 0.011*SL	0.207 + 0.008*SL	0.222 + 0.008*SL
	t_{PLH}	0.266	0.252 + 0.007*SL	0.262 + 0.005*SL	0.280 + 0.004*SL
	t_{PHL}	0.557	0.536 + 0.011*SL	0.554 + 0.006*SL	0.638 + 0.005*SL
D to Y	t_R	0.124	0.107 + 0.008*SL	0.103 + 0.009*SL	0.074 + 0.010*SL
	t_F	0.217	0.196 + 0.011*SL	0.206 + 0.008*SL	0.221 + 0.008*SL
	t_{PLH}	0.275	0.261 + 0.007*SL	0.271 + 0.005*SL	0.293 + 0.004*SL
	t_{PHL}	0.575	0.554 + 0.010*SL	0.571 + 0.006*SL	0.657 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OR5/OR5D2/OR5D4

5-Input OR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	0
1	x	x	x	x	1
x	1	x	x	x	1
x	x	1	x	x	1
x	x	x	1	x	1
x	x	x	x	1	1

Cell Data

Input Load (SL)															Gate Count		
OR5					*OR5D2*					*OR5D4*					*OR5*	*OR5D2*	*OR5D4*
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E			
0.8	0.7	0.8	0.7	0.8	1.0	1.0	1.1	1.0	1.1	1.0	1.0	1.1	1.0	1.1	2.67	3.33	4.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OR5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.146	0.073 + 0.036*SL	0.064 + 0.038*SL	0.055 + 0.039*SL
	t_F	0.211	0.123 + 0.044*SL	0.125 + 0.043*SL	0.097 + 0.044*SL
	t_{PLH}	0.168	0.131 + 0.018*SL	0.134 + 0.017*SL	0.135 + 0.017*SL
	t_{PHL}	0.329	0.275 + 0.027*SL	0.296 + 0.022*SL	0.323 + 0.021*SL
B to Y	t_R	0.148	0.077 + 0.036*SL	0.067 + 0.038*SL	0.056 + 0.039*SL
	t_F	0.212	0.125 + 0.043*SL	0.126 + 0.043*SL	0.098 + 0.044*SL
	t_{PLH}	0.190	0.153 + 0.018*SL	0.156 + 0.017*SL	0.157 + 0.017*SL
	t_{PHL}	0.355	0.300 + 0.027*SL	0.322 + 0.022*SL	0.348 + 0.021*SL
C to Y	t_R	0.152	0.081 + 0.036*SL	0.071 + 0.038*SL	0.059 + 0.039*SL
	t_F	0.212	0.124 + 0.044*SL	0.126 + 0.043*SL	0.098 + 0.044*SL
	t_{PLH}	0.200	0.162 + 0.019*SL	0.167 + 0.018*SL	0.170 + 0.017*SL
	t_{PHL}	0.366	0.311 + 0.027*SL	0.333 + 0.022*SL	0.359 + 0.021*SL
D to Y	t_R	0.161	0.090 + 0.036*SL	0.078 + 0.038*SL	0.069 + 0.039*SL
	t_F	0.176	0.091 + 0.042*SL	0.084 + 0.044*SL	0.071 + 0.045*SL
	t_{PLH}	0.168	0.132 + 0.018*SL	0.134 + 0.017*SL	0.134 + 0.017*SL
	t_{PHL}	0.262	0.215 + 0.023*SL	0.222 + 0.021*SL	0.229 + 0.021*SL
E to Y	t_R	0.163	0.092 + 0.036*SL	0.080 + 0.038*SL	0.070 + 0.039*SL
	t_F	0.176	0.091 + 0.043*SL	0.085 + 0.044*SL	0.071 + 0.045*SL
	t_{PLH}	0.190	0.154 + 0.018*SL	0.156 + 0.017*SL	0.156 + 0.017*SL
	t_{PHL}	0.262	0.215 + 0.023*SL	0.223 + 0.021*SL	0.230 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OR5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.110	0.076 + 0.017*SL	0.068 + 0.019*SL	0.052 + 0.019*SL
	t_F	0.178	0.133 + 0.022*SL	0.135 + 0.022*SL	0.107 + 0.022*SL
	t_{PLH}	0.165	0.145 + 0.010*SL	0.150 + 0.009*SL	0.152 + 0.009*SL
	t_{PHL}	0.333	0.301 + 0.016*SL	0.319 + 0.011*SL	0.363 + 0.011*SL
B to Y	t_R	0.114	0.079 + 0.017*SL	0.072 + 0.019*SL	0.053 + 0.019*SL
	t_F	0.180	0.136 + 0.022*SL	0.137 + 0.022*SL	0.108 + 0.022*SL
	t_{PLH}	0.188	0.167 + 0.010*SL	0.173 + 0.009*SL	0.175 + 0.009*SL
	t_{PHL}	0.363	0.332 + 0.016*SL	0.349 + 0.011*SL	0.393 + 0.011*SL
C to Y	t_R	0.119	0.084 + 0.017*SL	0.077 + 0.019*SL	0.057 + 0.019*SL
	t_F	0.179	0.135 + 0.022*SL	0.136 + 0.022*SL	0.108 + 0.022*SL
	t_{PLH}	0.198	0.177 + 0.010*SL	0.183 + 0.009*SL	0.189 + 0.009*SL
	t_{PHL}	0.375	0.344 + 0.016*SL	0.361 + 0.011*SL	0.406 + 0.011*SL
D to Y	t_R	0.127	0.094 + 0.017*SL	0.085 + 0.019*SL	0.067 + 0.019*SL
	t_F	0.140	0.099 + 0.020*SL	0.092 + 0.022*SL	0.072 + 0.022*SL
	t_{PLH}	0.169	0.150 + 0.010*SL	0.154 + 0.009*SL	0.154 + 0.009*SL
	t_{PHL}	0.262	0.237 + 0.013*SL	0.243 + 0.011*SL	0.257 + 0.011*SL
E to Y	t_R	0.130	0.097 + 0.017*SL	0.088 + 0.019*SL	0.067 + 0.019*SL
	t_F	0.141	0.100 + 0.020*SL	0.093 + 0.022*SL	0.072 + 0.022*SL
	t_{PLH}	0.191	0.172 + 0.010*SL	0.175 + 0.009*SL	0.176 + 0.009*SL
	t_{PHL}	0.264	0.239 + 0.013*SL	0.246 + 0.011*SL	0.259 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OR5D4

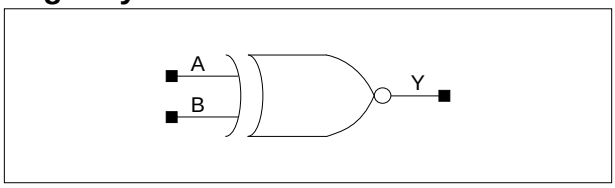
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.109	0.094 + 0.008*SL	0.087 + 0.009*SL	0.064 + 0.010*SL
	t_F	0.213	0.192 + 0.011*SL	0.192 + 0.011*SL	0.179 + 0.011*SL
	t_{PLH}	0.199	0.187 + 0.006*SL	0.193 + 0.004*SL	0.202 + 0.004*SL
	t_{PHL}	0.433	0.414 + 0.009*SL	0.426 + 0.006*SL	0.486 + 0.005*SL
B to Y	t_R	0.113	0.096 + 0.008*SL	0.093 + 0.009*SL	0.066 + 0.010*SL
	t_F	0.213	0.191 + 0.011*SL	0.193 + 0.011*SL	0.180 + 0.011*SL
	t_{PLH}	0.220	0.209 + 0.006*SL	0.214 + 0.004*SL	0.223 + 0.004*SL
	t_{PHL}	0.465	0.446 + 0.009*SL	0.458 + 0.006*SL	0.518 + 0.005*SL
C to Y	t_R	0.118	0.102 + 0.008*SL	0.098 + 0.009*SL	0.071 + 0.010*SL
	t_F	0.214	0.192 + 0.011*SL	0.193 + 0.011*SL	0.180 + 0.011*SL
	t_{PLH}	0.232	0.220 + 0.006*SL	0.225 + 0.005*SL	0.238 + 0.004*SL
	t_{PHL}	0.478	0.459 + 0.009*SL	0.471 + 0.006*SL	0.531 + 0.005*SL
D to Y	t_R	0.128	0.111 + 0.008*SL	0.108 + 0.009*SL	0.080 + 0.010*SL
	t_F	0.160	0.142 + 0.009*SL	0.135 + 0.011*SL	0.107 + 0.011*SL
	t_{PLH}	0.208	0.198 + 0.005*SL	0.201 + 0.004*SL	0.207 + 0.004*SL
	t_{PHL}	0.329	0.314 + 0.007*SL	0.321 + 0.006*SL	0.344 + 0.005*SL
E to Y	t_R	0.132	0.116 + 0.008*SL	0.112 + 0.009*SL	0.082 + 0.010*SL
	t_F	0.160	0.141 + 0.009*SL	0.136 + 0.011*SL	0.107 + 0.011*SL
	t_{PLH}	0.228	0.218 + 0.005*SL	0.221 + 0.004*SL	0.227 + 0.004*SL
	t_{PHL}	0.333	0.318 + 0.007*SL	0.325 + 0.006*SL	0.348 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

XN2/XN2D2/XN2D4

2-Input Exclusive-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Cell Data

Input Load (SL)						Gate Count		
XN2		*XN2D2*		*XN2D4*		*XN2*	*XN2D2*	*XN2D4*
A	B	A	B	A	B			
1.0	2.0	1.0	2.0	1.0	2.0	2.33	2.67	3.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

XN2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.153	0.081 + 0.036*SL	0.072 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.136	0.073 + 0.032*SL	0.071 + 0.032*SL	0.046 + 0.033*SL
	t_{PLH}	0.304	0.265 + 0.020*SL	0.274 + 0.018*SL	0.277 + 0.017*SL
	t_{PHL}	0.299	0.257 + 0.021*SL	0.272 + 0.018*SL	0.282 + 0.017*SL
B to Y	t_R	0.152	0.081 + 0.036*SL	0.071 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.147	0.078 + 0.034*SL	0.088 + 0.032*SL	0.064 + 0.033*SL
	t_{PLH}	0.257	0.218 + 0.020*SL	0.227 + 0.018*SL	0.229 + 0.017*SL
	t_{PHL}	0.241	0.194 + 0.023*SL	0.215 + 0.018*SL	0.240 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

XN2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.118	0.081 + 0.018*SL	0.079 + 0.019*SL	0.045 + 0.019*SL
	t_F	0.111	0.078 + 0.016*SL	0.080 + 0.016*SL	0.047 + 0.016*SL
	t_{PLH}	0.309	0.286 + 0.012*SL	0.298 + 0.009*SL	0.309 + 0.009*SL
	t_{PHL}	0.307	0.281 + 0.013*SL	0.298 + 0.009*SL	0.324 + 0.009*SL
B to Y	t_R	0.118	0.082 + 0.018*SL	0.077 + 0.019*SL	0.045 + 0.019*SL
	t_F	0.123	0.085 + 0.019*SL	0.097 + 0.016*SL	0.080 + 0.016*SL
	t_{PLH}	0.262	0.238 + 0.012*SL	0.250 + 0.009*SL	0.261 + 0.009*SL
	t_{PHL}	0.238	0.208 + 0.015*SL	0.230 + 0.009*SL	0.284 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

XN2D4

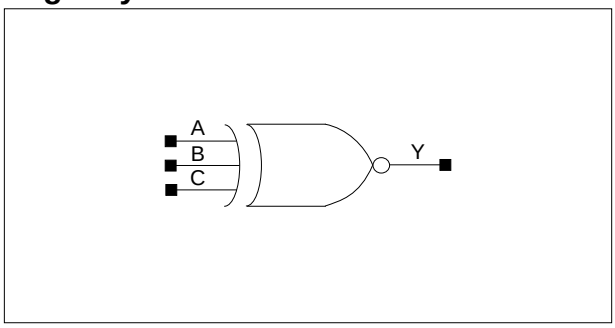
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.127	0.110 + 0.009*SL	0.107 + 0.009*SL	0.082 + 0.010*SL
	t_F	0.129	0.109 + 0.010*SL	0.117 + 0.008*SL	0.100 + 0.008*SL
	t_{PLH}	0.357	0.342 + 0.008*SL	0.353 + 0.005*SL	0.383 + 0.004*SL
	t_{PHL}	0.370	0.353 + 0.009*SL	0.367 + 0.005*SL	0.415 + 0.004*SL
B to Y	t_R	0.126	0.109 + 0.008*SL	0.107 + 0.009*SL	0.082 + 0.010*SL
	t_F	0.129	0.110 + 0.009*SL	0.115 + 0.008*SL	0.100 + 0.008*SL
	t_{PLH}	0.308	0.292 + 0.008*SL	0.304 + 0.005*SL	0.333 + 0.004*SL
	t_{PHL}	0.300	0.283 + 0.008*SL	0.296 + 0.005*SL	0.344 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

XN3/XN3D2/XN3D4

3-Input Exclusive-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Data

Input Load (SL)									Gate Count		
XN3			*XN3D2*			*XN3D4*			*XN3*	*XN3D2*	*XN3D4*
A	B	C	A	B	C	A	B	C			
1.5	1.0	2.0	1.5	1.0	2.0	1.5	1.0	2.0	4.00	4.33	5.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

XN3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.173	0.094 + 0.039*SL	0.101 + 0.038*SL	0.077 + 0.038*SL
	t_F	0.178	0.099 + 0.040*SL	0.124 + 0.033*SL	0.141 + 0.033*SL
	t_{PLH}	0.283	0.237 + 0.023*SL	0.257 + 0.018*SL	0.282 + 0.017*SL
	t_{PHL}	0.275	0.219 + 0.028*SL	0.251 + 0.020*SL	0.329 + 0.018*SL
B to Y	t_R	0.181	0.108 + 0.037*SL	0.105 + 0.037*SL	0.070 + 0.038*SL
	t_F	0.137	0.073 + 0.032*SL	0.070 + 0.033*SL	0.044 + 0.033*SL
	t_{PLH}	0.433	0.388 + 0.023*SL	0.407 + 0.018*SL	0.423 + 0.017*SL
	t_{PHL}	0.463	0.420 + 0.022*SL	0.435 + 0.018*SL	0.445 + 0.018*SL
C to Y	t_R	0.181	0.107 + 0.037*SL	0.105 + 0.037*SL	0.070 + 0.038*SL
	t_F	0.138	0.073 + 0.032*SL	0.071 + 0.033*SL	0.044 + 0.033*SL
	t_{PLH}	0.387	0.341 + 0.023*SL	0.360 + 0.018*SL	0.377 + 0.017*SL
	t_{PHL}	0.417	0.374 + 0.022*SL	0.389 + 0.018*SL	0.398 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

XN3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.148	0.109 + 0.019*SL	0.111 + 0.019*SL	0.087 + 0.019*SL
	t_F	0.163	0.115 + 0.024*SL	0.142 + 0.017*SL	0.190 + 0.016*SL
	t_{PLH}	0.294	0.265 + 0.015*SL	0.286 + 0.009*SL	0.334 + 0.009*SL
	t_{PHL}	0.282	0.245 + 0.019*SL	0.276 + 0.011*SL	0.406 + 0.009*SL
B to Y	t_R	0.150	0.114 + 0.018*SL	0.111 + 0.019*SL	0.074 + 0.019*SL
	t_F	0.112	0.078 + 0.017*SL	0.080 + 0.016*SL	0.045 + 0.017*SL
	t_{PLH}	0.443	0.415 + 0.014*SL	0.434 + 0.009*SL	0.470 + 0.009*SL
	t_{PHL}	0.472	0.445 + 0.013*SL	0.462 + 0.009*SL	0.487 + 0.009*SL
C to Y	t_R	0.149	0.112 + 0.019*SL	0.111 + 0.019*SL	0.075 + 0.019*SL
	t_F	0.112	0.078 + 0.017*SL	0.080 + 0.016*SL	0.045 + 0.017*SL
	t_{PLH}	0.396	0.368 + 0.014*SL	0.387 + 0.009*SL	0.423 + 0.009*SL
	t_{PHL}	0.426	0.399 + 0.013*SL	0.416 + 0.009*SL	0.441 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

XN3D4

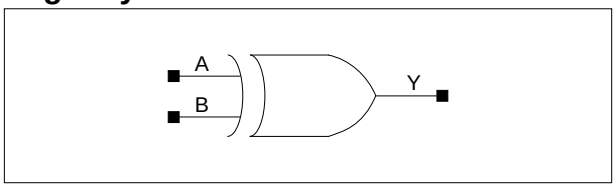
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.185	0.166 + 0.009*SL	0.167 + 0.009*SL	0.160 + 0.009*SL
	t_F	0.222	0.195 + 0.014*SL	0.212 + 0.009*SL	0.291 + 0.008*SL
	t_{PLH}	0.366	0.347 + 0.010*SL	0.364 + 0.006*SL	0.431 + 0.005*SL
	t_{PHL}	0.368	0.343 + 0.012*SL	0.364 + 0.007*SL	0.489 + 0.005*SL
B to Y	t_R	0.169	0.151 + 0.009*SL	0.150 + 0.009*SL	0.136 + 0.009*SL
	t_F	0.130	0.111 + 0.009*SL	0.117 + 0.008*SL	0.100 + 0.008*SL
	t_{PLH}	0.509	0.491 + 0.009*SL	0.506 + 0.005*SL	0.561 + 0.004*SL
	t_{PHL}	0.536	0.519 + 0.009*SL	0.532 + 0.005*SL	0.580 + 0.004*SL
C to Y	t_R	0.168	0.150 + 0.009*SL	0.150 + 0.009*SL	0.137 + 0.009*SL
	t_F	0.129	0.110 + 0.010*SL	0.116 + 0.008*SL	0.100 + 0.008*SL
	t_{PLH}	0.462	0.443 + 0.009*SL	0.458 + 0.005*SL	0.514 + 0.004*SL
	t_{PHL}	0.489	0.472 + 0.008*SL	0.486 + 0.005*SL	0.533 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

XO2/XO2D2/XO2D4

2-Input Exclusive-OR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Cell Data

Input Load (SL)						Gate Count		
XO2		*XO2D2*		*XO2D4*		*XO2*	*XO2D2*	*XO2D4*
A	B	A	B	A	B			
1.0	1.5	1.0	1.5	1.0	1.5	2.33	2.67	3.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

XO2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.153	0.082 + 0.036*SL	0.072 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.137	0.074 + 0.032*SL	0.072 + 0.032*SL	0.046 + 0.033*SL
	t_{PLH}	0.306	0.266 + 0.020*SL	0.275 + 0.018*SL	0.278 + 0.017*SL
	t_{PHL}	0.302	0.260 + 0.021*SL	0.275 + 0.018*SL	0.286 + 0.017*SL
B to Y	t_R	0.150	0.077 + 0.036*SL	0.071 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.136	0.073 + 0.032*SL	0.071 + 0.032*SL	0.046 + 0.033*SL
	t_{PLH}	0.258	0.218 + 0.020*SL	0.228 + 0.018*SL	0.232 + 0.017*SL
	t_{PHL}	0.267	0.224 + 0.021*SL	0.240 + 0.018*SL	0.250 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

XO2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.119	0.083 + 0.018*SL	0.079 + 0.019*SL	0.045 + 0.019*SL
	t_F	0.111	0.078 + 0.017*SL	0.081 + 0.016*SL	0.047 + 0.016*SL
	t_{PLH}	0.311	0.287 + 0.012*SL	0.299 + 0.009*SL	0.310 + 0.009*SL
	t_{PHL}	0.311	0.284 + 0.013*SL	0.301 + 0.009*SL	0.328 + 0.009*SL
B to Y	t_R	0.116	0.079 + 0.019*SL	0.077 + 0.019*SL	0.047 + 0.019*SL
	t_F	0.111	0.078 + 0.017*SL	0.081 + 0.016*SL	0.047 + 0.016*SL
	t_{PLH}	0.261	0.237 + 0.012*SL	0.250 + 0.009*SL	0.264 + 0.009*SL
	t_{PHL}	0.274	0.247 + 0.013*SL	0.265 + 0.009*SL	0.291 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

XO2D4

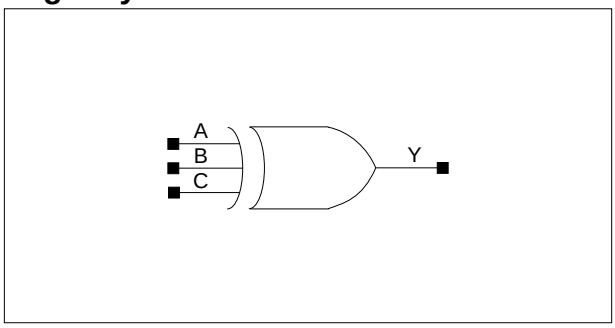
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.127	0.110 + 0.008*SL	0.107 + 0.009*SL	0.082 + 0.010*SL
	t_F	0.130	0.111 + 0.009*SL	0.117 + 0.008*SL	0.101 + 0.008*SL
	t_{PLH}	0.358	0.343 + 0.008*SL	0.354 + 0.005*SL	0.384 + 0.004*SL
	t_{PHL}	0.374	0.357 + 0.009*SL	0.370 + 0.005*SL	0.419 + 0.004*SL
B to Y	t_R	0.128	0.111 + 0.009*SL	0.108 + 0.009*SL	0.088 + 0.010*SL
	t_F	0.130	0.111 + 0.009*SL	0.117 + 0.008*SL	0.100 + 0.008*SL
	t_{PLH}	0.306	0.290 + 0.008*SL	0.302 + 0.005*SL	0.337 + 0.004*SL
	t_{PHL}	0.336	0.318 + 0.009*SL	0.332 + 0.005*SL	0.380 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

XO3/XO3D2/XO3D4

3-Input Exclusive-OR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Data

Input Load (SL)									Gate Count		
XO3			*XO3D2*			*XO3D4*			*XO3*	*XO3D2*	*XO3D4*
A	B	C	A	B	C	A	B	C			
1.9	1.0	2.0	1.9	1.0	2.0	1.9	1.0	2.0	4.00	4.33	5.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

XO3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.149	0.078 + 0.036*SL	0.069 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.191	0.112 + 0.040*SL	0.138 + 0.033*SL	0.148 + 0.033*SL
	t_{PLH}	0.251	0.211 + 0.020*SL	0.221 + 0.018*SL	0.223 + 0.017*SL
	t_{PHL}	0.282	0.224 + 0.029*SL	0.261 + 0.020*SL	0.342 + 0.018*SL
B to Y	t_R	0.182	0.109 + 0.037*SL	0.105 + 0.037*SL	0.070 + 0.038*SL
	t_F	0.138	0.073 + 0.032*SL	0.071 + 0.033*SL	0.044 + 0.033*SL
	t_{PLH}	0.437	0.392 + 0.022*SL	0.410 + 0.018*SL	0.426 + 0.017*SL
	t_{PHL}	0.460	0.416 + 0.022*SL	0.432 + 0.018*SL	0.441 + 0.018*SL
C to Y	t_R	0.182	0.108 + 0.037*SL	0.106 + 0.037*SL	0.070 + 0.038*SL
	t_F	0.137	0.073 + 0.032*SL	0.071 + 0.033*SL	0.044 + 0.033*SL
	t_{PLH}	0.390	0.345 + 0.023*SL	0.363 + 0.018*SL	0.379 + 0.017*SL
	t_{PHL}	0.414	0.371 + 0.022*SL	0.386 + 0.018*SL	0.395 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

XO3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.116	0.081 + 0.018*SL	0.076 + 0.019*SL	0.043 + 0.019*SL
	t_F	0.179	0.132 + 0.023*SL	0.159 + 0.017*SL	0.195 + 0.016*SL
	t_{PLH}	0.256	0.232 + 0.012*SL	0.244 + 0.009*SL	0.255 + 0.009*SL
	t_{PHL}	0.294	0.256 + 0.019*SL	0.288 + 0.011*SL	0.419 + 0.009*SL
B to Y	t_R	0.151	0.114 + 0.019*SL	0.114 + 0.019*SL	0.076 + 0.019*SL
	t_F	0.111	0.077 + 0.017*SL	0.080 + 0.016*SL	0.045 + 0.017*SL
	t_{PLH}	0.450	0.422 + 0.014*SL	0.441 + 0.009*SL	0.477 + 0.009*SL
	t_{PHL}	0.469	0.442 + 0.013*SL	0.459 + 0.009*SL	0.484 + 0.009*SL
C to Y	t_R	0.153	0.117 + 0.018*SL	0.114 + 0.019*SL	0.076 + 0.019*SL
	t_F	0.112	0.078 + 0.017*SL	0.080 + 0.016*SL	0.045 + 0.017*SL
	t_{PLH}	0.403	0.375 + 0.014*SL	0.395 + 0.009*SL	0.430 + 0.009*SL
	t_{PHL}	0.423	0.396 + 0.013*SL	0.413 + 0.009*SL	0.438 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

XO3D4

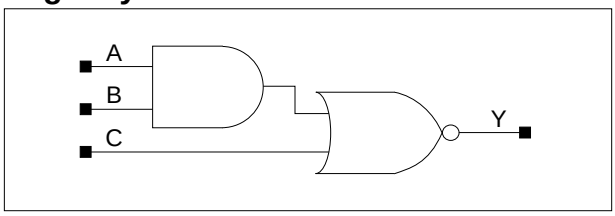
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.189	0.171 + 0.009*SL	0.170 + 0.009*SL	0.164 + 0.009*SL
	t_F	0.242	0.216 + 0.013*SL	0.232 + 0.009*SL	0.303 + 0.008*SL
	t_{PLH}	0.328	0.309 + 0.010*SL	0.326 + 0.006*SL	0.393 + 0.005*SL
	t_{PHL}	0.388	0.363 + 0.012*SL	0.384 + 0.007*SL	0.509 + 0.005*SL
B to Y	t_R	0.175	0.157 + 0.009*SL	0.156 + 0.009*SL	0.143 + 0.009*SL
	t_F	0.210	0.187 + 0.012*SL	0.200 + 0.008*SL	0.232 + 0.008*SL
	t_{PLH}	0.522	0.504 + 0.009*SL	0.519 + 0.005*SL	0.576 + 0.004*SL
	t_{PHL}	0.537	0.515 + 0.011*SL	0.534 + 0.006*SL	0.632 + 0.005*SL
C to Y	t_R	0.176	0.159 + 0.009*SL	0.157 + 0.009*SL	0.143 + 0.009*SL
	t_F	0.257	0.232 + 0.013*SL	0.247 + 0.009*SL	0.314 + 0.008*SL
	t_{PLH}	0.475	0.456 + 0.009*SL	0.472 + 0.005*SL	0.529 + 0.004*SL
	t_{PHL}	0.500	0.476 + 0.012*SL	0.496 + 0.007*SL	0.620 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO21/AO21D2/AO21D2B/AO21D4

2-AND into 2-NOR with 1X/2X/2X(Bufferd)/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	0	1
x	0	0	1
Other States			0

Cell Data

Input Load (SL)											
AO21			*AO21D2*			*AO21D2B*			*AO21D4*		
A	B	C	A	B	C	A	B	C	A	B	C
0.9	0.9	0.9	1.8	1.9	2.0	0.9	0.9	1.0	0.9	0.9	0.9

Gate Count			
AO21	*AO21D2*	*AO21D2B*	*AO21D4*
1.33	2.33	2.33	3.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.308	0.171 + 0.069*SL	0.147 + 0.075*SL	0.131 + 0.075*SL
	t_F	0.238	0.120 + 0.059*SL	0.100 + 0.064*SL	0.082 + 0.064*SL
	t_{PLH}	0.166	0.100 + 0.033*SL	0.099 + 0.033*SL	0.097 + 0.033*SL
	t_{PHL}	0.155	0.091 + 0.032*SL	0.095 + 0.031*SL	0.095 + 0.031*SL
B to Y	t_R	0.322	0.187 + 0.067*SL	0.163 + 0.073*SL	0.146 + 0.074*SL
	t_F	0.232	0.113 + 0.060*SL	0.096 + 0.064*SL	0.082 + 0.064*SL
	t_{PLH}	0.176	0.112 + 0.032*SL	0.109 + 0.032*SL	0.105 + 0.033*SL
	t_{PHL}	0.141	0.077 + 0.032*SL	0.081 + 0.031*SL	0.081 + 0.031*SL
C to Y	t_R	0.313	0.173 + 0.070*SL	0.159 + 0.074*SL	0.146 + 0.074*SL
	t_F	0.230	0.158 + 0.036*SL	0.144 + 0.039*SL	0.117 + 0.040*SL
	t_{PLH}	0.203	0.138 + 0.033*SL	0.139 + 0.033*SL	0.139 + 0.033*SL
	t_{PHL}	0.169	0.125 + 0.022*SL	0.128 + 0.021*SL	0.131 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

AO21D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.240	0.174 + 0.033*SL	0.157 + 0.037*SL	0.129 + 0.038*SL
	t_F	0.179	0.122 + 0.029*SL	0.109 + 0.032*SL	0.082 + 0.032*SL
	t_{PLH}	0.133	0.098 + 0.018*SL	0.102 + 0.017*SL	0.098 + 0.017*SL
	t_{PHL}	0.122	0.087 + 0.018*SL	0.096 + 0.015*SL	0.095 + 0.015*SL
B to Y	t_R	0.253	0.189 + 0.032*SL	0.172 + 0.037*SL	0.143 + 0.037*SL
	t_F	0.174	0.117 + 0.028*SL	0.103 + 0.032*SL	0.082 + 0.032*SL
	t_{PLH}	0.144	0.111 + 0.017*SL	0.112 + 0.016*SL	0.106 + 0.016*SL
	t_{PHL}	0.109	0.075 + 0.017*SL	0.081 + 0.015*SL	0.082 + 0.015*SL
C to Y	t_R	0.240	0.173 + 0.034*SL	0.162 + 0.037*SL	0.143 + 0.037*SL
	t_F	0.188	0.153 + 0.018*SL	0.146 + 0.019*SL	0.110 + 0.020*SL
	t_{PLH}	0.164	0.131 + 0.017*SL	0.133 + 0.016*SL	0.133 + 0.016*SL
	t_{PHL}	0.143	0.120 + 0.011*SL	0.123 + 0.011*SL	0.126 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO21D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.095	0.061 + 0.017*SL	0.052 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.081	0.049 + 0.016*SL	0.046 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.274	0.253 + 0.010*SL	0.259 + 0.009*SL	0.261 + 0.009*SL
	t_{PHL}	0.267	0.245 + 0.011*SL	0.254 + 0.009*SL	0.259 + 0.009*SL
B to Y	t_R	0.095	0.061 + 0.017*SL	0.052 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.083	0.052 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.290	0.269 + 0.010*SL	0.275 + 0.009*SL	0.277 + 0.009*SL
	t_{PHL}	0.251	0.229 + 0.011*SL	0.238 + 0.009*SL	0.246 + 0.009*SL
C to Y	t_R	0.096	0.061 + 0.017*SL	0.053 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.078	0.045 + 0.017*SL	0.044 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.316	0.295 + 0.010*SL	0.301 + 0.009*SL	0.303 + 0.009*SL
	t_{PHL}	0.288	0.266 + 0.011*SL	0.275 + 0.009*SL	0.280 + 0.009*SL

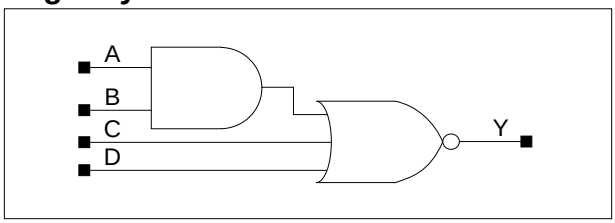
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO21D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.093	0.076 + 0.009*SL	0.072 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.080	0.064 + 0.008*SL	0.064 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.316	0.303 + 0.006*SL	0.310 + 0.005*SL	0.319 + 0.004*SL
	t_{PHL}	0.304	0.290 + 0.007*SL	0.299 + 0.005*SL	0.316 + 0.004*SL
B to Y	t_R	0.093	0.076 + 0.009*SL	0.073 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.079	0.062 + 0.009*SL	0.065 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.328	0.315 + 0.006*SL	0.322 + 0.004*SL	0.332 + 0.004*SL
	t_{PHL}	0.290	0.277 + 0.007*SL	0.285 + 0.005*SL	0.302 + 0.004*SL
C to Y	t_R	0.093	0.076 + 0.008*SL	0.072 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.078	0.062 + 0.008*SL	0.062 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.353	0.341 + 0.006*SL	0.347 + 0.004*SL	0.357 + 0.004*SL
	t_{PHL}	0.320	0.307 + 0.007*SL	0.315 + 0.005*SL	0.332 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	0	0	1
x	0	0	0	1
Other States				0

Cell Data

Input Load (SL)															
AO211				*AO211D2*				*AO211D2B*				*AO211D4*			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.9	0.9	0.9	0.9	1.8	1.9	1.9	2.0	0.9	0.9	0.9	0.9	0.9	0.9	0.9	1.0

Gate Count			
AO211	*AO211D2*	*AO211D2B*	*AO211D4*
1.67	2.67	2.67	3.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.467	0.254 + 0.106*SL	0.236 + 0.111*SL	0.240 + 0.111*SL
	t_F	0.241	0.122 + 0.059*SL	0.103 + 0.064*SL	0.086 + 0.064*SL
	t_{PLH}	0.205	0.112 + 0.046*SL	0.103 + 0.048*SL	0.101 + 0.049*SL
	t_{PHL}	0.159	0.096 + 0.032*SL	0.099 + 0.031*SL	0.099 + 0.031*SL
B to Y	t_R	0.487	0.278 + 0.104*SL	0.258 + 0.109*SL	0.263 + 0.109*SL
	t_F	0.235	0.115 + 0.060*SL	0.099 + 0.064*SL	0.086 + 0.064*SL
	t_{PLH}	0.217	0.126 + 0.046*SL	0.117 + 0.048*SL	0.113 + 0.048*SL
	t_{PHL}	0.145	0.082 + 0.032*SL	0.085 + 0.031*SL	0.085 + 0.031*SL
C to Y	t_R	0.498	0.288 + 0.105*SL	0.273 + 0.109*SL	0.263 + 0.109*SL
	t_F	0.233	0.159 + 0.037*SL	0.145 + 0.040*SL	0.121 + 0.041*SL
	t_{PLH}	0.284	0.186 + 0.049*SL	0.189 + 0.048*SL	0.192 + 0.048*SL
	t_{PHL}	0.176	0.131 + 0.022*SL	0.134 + 0.022*SL	0.138 + 0.022*SL
D to Y	t_R	0.496	0.285 + 0.105*SL	0.271 + 0.109*SL	0.263 + 0.109*SL
	t_F	0.268	0.192 + 0.038*SL	0.183 + 0.040*SL	0.156 + 0.041*SL
	t_{PLH}	0.295	0.198 + 0.049*SL	0.200 + 0.048*SL	0.204 + 0.048*SL
	t_{PHL}	0.188	0.142 + 0.023*SL	0.147 + 0.022*SL	0.157 + 0.022*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

AO211D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.352	0.249 + 0.052*SL	0.234 + 0.056*SL	0.227 + 0.056*SL
	t_F	0.178	0.120 + 0.029*SL	0.108 + 0.032*SL	0.083 + 0.032*SL
	t_{PLH}	0.158	0.112 + 0.023*SL	0.106 + 0.024*SL	0.101 + 0.024*SL
	t_{PHL}	0.124	0.089 + 0.017*SL	0.097 + 0.015*SL	0.097 + 0.015*SL
B to Y	t_R	0.374	0.273 + 0.051*SL	0.257 + 0.055*SL	0.250 + 0.055*SL
	t_F	0.173	0.116 + 0.028*SL	0.102 + 0.032*SL	0.083 + 0.032*SL
	t_{PLH}	0.172	0.128 + 0.022*SL	0.121 + 0.024*SL	0.114 + 0.024*SL
	t_{PHL}	0.111	0.077 + 0.017*SL	0.083 + 0.015*SL	0.084 + 0.015*SL
C to Y	t_R	0.381	0.277 + 0.052*SL	0.267 + 0.054*SL	0.250 + 0.055*SL
	t_F	0.188	0.152 + 0.018*SL	0.144 + 0.020*SL	0.112 + 0.021*SL
	t_{PLH}	0.226	0.176 + 0.025*SL	0.179 + 0.024*SL	0.182 + 0.024*SL
	t_{PHL}	0.148	0.124 + 0.012*SL	0.128 + 0.011*SL	0.132 + 0.011*SL
D to Y	t_R	0.378	0.274 + 0.052*SL	0.263 + 0.055*SL	0.250 + 0.055*SL
	t_F	0.224	0.187 + 0.018*SL	0.180 + 0.020*SL	0.148 + 0.020*SL
	t_{PLH}	0.239	0.190 + 0.025*SL	0.192 + 0.024*SL	0.197 + 0.024*SL
	t_{PHL}	0.161	0.138 + 0.012*SL	0.141 + 0.011*SL	0.152 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO211D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.100	0.066 + 0.017*SL	0.057 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.080	0.047 + 0.017*SL	0.047 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.325	0.304 + 0.010*SL	0.311 + 0.009*SL	0.312 + 0.009*SL
	t_{PHL}	0.282	0.259 + 0.011*SL	0.268 + 0.009*SL	0.274 + 0.009*SL
B to Y	t_R	0.100	0.066 + 0.017*SL	0.058 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.082	0.050 + 0.016*SL	0.047 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.342	0.321 + 0.010*SL	0.328 + 0.009*SL	0.329 + 0.009*SL
	t_{PHL}	0.269	0.247 + 0.011*SL	0.256 + 0.009*SL	0.261 + 0.009*SL
C to Y	t_R	0.101	0.067 + 0.017*SL	0.058 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.079	0.046 + 0.016*SL	0.046 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.408	0.387 + 0.010*SL	0.394 + 0.009*SL	0.395 + 0.009*SL
	t_{PHL}	0.303	0.281 + 0.011*SL	0.290 + 0.009*SL	0.295 + 0.009*SL
D to Y	t_R	0.101	0.067 + 0.017*SL	0.058 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.081	0.049 + 0.016*SL	0.046 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.424	0.403 + 0.010*SL	0.409 + 0.009*SL	0.411 + 0.009*SL
	t_{PHL}	0.323	0.301 + 0.011*SL	0.309 + 0.009*SL	0.315 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO211D4

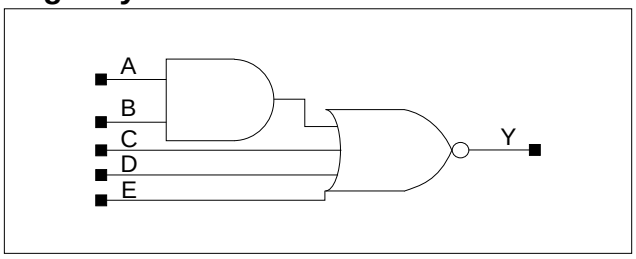
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.100	0.083 + 0.008*SL	0.080 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.081	0.065 + 0.008*SL	0.065 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.370	0.357 + 0.006*SL	0.364 + 0.005*SL	0.374 + 0.004*SL
	t_{PHL}	0.318	0.305 + 0.007*SL	0.313 + 0.005*SL	0.330 + 0.004*SL
B to Y	t_R	0.100	0.083 + 0.008*SL	0.080 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.081	0.065 + 0.008*SL	0.065 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.386	0.374 + 0.006*SL	0.381 + 0.005*SL	0.391 + 0.004*SL
	t_{PHL}	0.305	0.291 + 0.007*SL	0.299 + 0.005*SL	0.317 + 0.004*SL
C to Y	t_R	0.100	0.083 + 0.009*SL	0.080 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.079	0.062 + 0.008*SL	0.063 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.453	0.440 + 0.006*SL	0.448 + 0.005*SL	0.458 + 0.004*SL
	t_{PHL}	0.337	0.323 + 0.007*SL	0.332 + 0.005*SL	0.349 + 0.004*SL
D to Y	t_R	0.101	0.084 + 0.008*SL	0.081 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.080	0.064 + 0.008*SL	0.064 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.465	0.452 + 0.006*SL	0.459 + 0.005*SL	0.470 + 0.004*SL
	t_{PHL}	0.356	0.342 + 0.007*SL	0.351 + 0.005*SL	0.368 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO2111/AO2111D2

2-AND into 4-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	0
x	x	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0
Other states					1

Cell Data

Input Load (SL)										Gate Count	
A02111					*AO2111D2*					*AO2111*	*AO2111D2*
A	B	C	D	E	A	B	C	D	E		
0.9	0.9	0.9	0.9	0.9	1.8	1.9	1.9	2.0	2.1	2.00	3.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO2111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.667	0.379 + 0.144*SL	0.369 + 0.147*SL	0.401 + 0.146*SL
	t_F	0.253	0.133 + 0.060*SL	0.117 + 0.064*SL	0.101 + 0.064*SL
	t_{PLH}	0.241	0.121 + 0.060*SL	0.105 + 0.064*SL	0.104 + 0.064*SL
	t_{PHL}	0.167	0.105 + 0.031*SL	0.106 + 0.031*SL	0.106 + 0.031*SL
B to Y	t_R	0.696	0.412 + 0.142*SL	0.399 + 0.145*SL	0.432 + 0.144*SL
	t_F	0.248	0.127 + 0.060*SL	0.113 + 0.064*SL	0.101 + 0.064*SL
	t_{PLH}	0.257	0.137 + 0.060*SL	0.123 + 0.063*SL	0.120 + 0.063*SL
	t_{PHL}	0.153	0.090 + 0.032*SL	0.092 + 0.031*SL	0.092 + 0.031*SL
C to Y	t_R	0.736	0.455 + 0.141*SL	0.441 + 0.144*SL	0.433 + 0.144*SL
	t_F	0.241	0.166 + 0.037*SL	0.154 + 0.040*SL	0.131 + 0.041*SL
	t_{PLH}	0.367	0.237 + 0.065*SL	0.242 + 0.064*SL	0.248 + 0.063*SL
	t_{PHL}	0.183	0.138 + 0.022*SL	0.141 + 0.022*SL	0.145 + 0.022*SL
D to Y	t_R	0.739	0.459 + 0.140*SL	0.443 + 0.144*SL	0.433 + 0.144*SL
	t_F	0.276	0.200 + 0.038*SL	0.191 + 0.040*SL	0.167 + 0.041*SL
	t_{PLH}	0.409	0.279 + 0.065*SL	0.284 + 0.064*SL	0.291 + 0.063*SL
	t_{PHL}	0.197	0.150 + 0.023*SL	0.156 + 0.022*SL	0.166 + 0.022*SL
E to Y	t_R	0.737	0.456 + 0.141*SL	0.442 + 0.144*SL	0.432 + 0.144*SL
	t_F	0.307	0.228 + 0.040*SL	0.224 + 0.040*SL	0.207 + 0.041*SL
	t_{PLH}	0.429	0.299 + 0.065*SL	0.304 + 0.064*SL	0.312 + 0.063*SL
	t_{PHL}	0.204	0.155 + 0.025*SL	0.164 + 0.022*SL	0.185 + 0.022*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

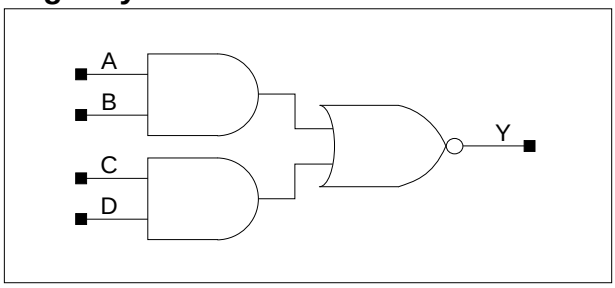
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO2111D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.539	0.397 + 0.071*SL	0.389 + 0.073*SL	0.415 + 0.073*SL
	t_F	0.203	0.145 + 0.029*SL	0.134 + 0.032*SL	0.111 + 0.032*SL
	t_{PLH}	0.193	0.138 + 0.028*SL	0.121 + 0.032*SL	0.117 + 0.032*SL
	t_{PHL}	0.140	0.107 + 0.017*SL	0.111 + 0.015*SL	0.111 + 0.015*SL
B to Y	t_R	0.568	0.428 + 0.070*SL	0.418 + 0.072*SL	0.444 + 0.072*SL
	t_F	0.198	0.139 + 0.029*SL	0.128 + 0.032*SL	0.111 + 0.032*SL
	t_{PLH}	0.209	0.153 + 0.028*SL	0.139 + 0.032*SL	0.132 + 0.032*SL
	t_{PHL}	0.125	0.093 + 0.016*SL	0.096 + 0.015*SL	0.097 + 0.015*SL
C to Y	t_R	0.606	0.467 + 0.069*SL	0.458 + 0.072*SL	0.444 + 0.072*SL
	t_F	0.202	0.167 + 0.018*SL	0.160 + 0.020*SL	0.130 + 0.020*SL
	t_{PLH}	0.305	0.240 + 0.032*SL	0.243 + 0.032*SL	0.250 + 0.032*SL
	t_{PHL}	0.157	0.135 + 0.011*SL	0.137 + 0.011*SL	0.141 + 0.011*SL
D to Y	t_R	0.609	0.470 + 0.069*SL	0.460 + 0.072*SL	0.444 + 0.072*SL
	t_F	0.236	0.200 + 0.018*SL	0.194 + 0.020*SL	0.165 + 0.020*SL
	t_{PLH}	0.348	0.282 + 0.033*SL	0.286 + 0.032*SL	0.295 + 0.032*SL
	t_{PHL}	0.172	0.149 + 0.011*SL	0.152 + 0.011*SL	0.164 + 0.011*SL
E to Y	t_R	0.606	0.467 + 0.069*SL	0.458 + 0.072*SL	0.444 + 0.072*SL
	t_F	0.265	0.227 + 0.019*SL	0.225 + 0.020*SL	0.206 + 0.020*SL
	t_{PLH}	0.371	0.305 + 0.033*SL	0.309 + 0.032*SL	0.320 + 0.032*SL
	t_{PHL}	0.178	0.154 + 0.012*SL	0.159 + 0.011*SL	0.183 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	1	1	0
0	x	0	x	1
0	x	x	0	1
x	0	x	0	1
x	0	0	x	1

Cell Data

Input Load (SL)															
AO22				*AO22D2*				*AO22D2B*				*AO22D4*			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
1.0	1.0	1.0	1.0	2.0	1.9	2.1	2.1	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

Gate Count			
AO22	*AO22D2*	*AO22D2B*	*AO22D4*
1.67	2.67	2.67	3.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.330	0.191 + 0.070*SL	0.173 + 0.074*SL	0.162 + 0.075*SL
	t_F	0.233	0.135 + 0.049*SL	0.117 + 0.053*SL	0.093 + 0.054*SL
	t_{PLH}	0.180	0.116 + 0.032*SL	0.113 + 0.033*SL	0.110 + 0.033*SL
	t_{PHL}	0.142	0.087 + 0.027*SL	0.093 + 0.026*SL	0.093 + 0.026*SL
B to Y	t_R	0.351	0.212 + 0.070*SL	0.194 + 0.074*SL	0.182 + 0.075*SL
	t_F	0.227	0.128 + 0.049*SL	0.111 + 0.054*SL	0.093 + 0.054*SL
	t_{PLH}	0.194	0.130 + 0.032*SL	0.126 + 0.033*SL	0.122 + 0.033*SL
	t_{PHL}	0.128	0.074 + 0.027*SL	0.079 + 0.026*SL	0.079 + 0.026*SL
C to Y	t_R	0.329	0.187 + 0.071*SL	0.173 + 0.074*SL	0.162 + 0.075*SL
	t_F	0.314	0.214 + 0.050*SL	0.199 + 0.053*SL	0.177 + 0.054*SL
	t_{PLH}	0.222	0.154 + 0.034*SL	0.157 + 0.033*SL	0.160 + 0.033*SL
	t_{PHL}	0.212	0.158 + 0.027*SL	0.162 + 0.026*SL	0.168 + 0.026*SL
D to Y	t_R	0.349	0.206 + 0.071*SL	0.194 + 0.074*SL	0.182 + 0.075*SL
	t_F	0.309	0.208 + 0.051*SL	0.196 + 0.054*SL	0.177 + 0.054*SL
	t_{PLH}	0.235	0.169 + 0.033*SL	0.170 + 0.033*SL	0.171 + 0.033*SL
	t_{PHL}	0.198	0.143 + 0.027*SL	0.148 + 0.026*SL	0.154 + 0.026*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

AO22D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.252	0.184 + 0.034*SL	0.171 + 0.037*SL	0.149 + 0.038*SL
	t_F	0.181	0.135 + 0.023*SL	0.121 + 0.027*SL	0.087 + 0.027*SL
	t_{PLH}	0.145	0.112 + 0.017*SL	0.113 + 0.016*SL	0.109 + 0.017*SL
	t_{PHL}	0.109	0.077 + 0.016*SL	0.088 + 0.013*SL	0.089 + 0.013*SL
B to Y	t_R	0.274	0.206 + 0.034*SL	0.193 + 0.038*SL	0.171 + 0.038*SL
	t_F	0.173	0.127 + 0.023*SL	0.112 + 0.027*SL	0.087 + 0.027*SL
	t_{PLH}	0.161	0.129 + 0.016*SL	0.127 + 0.017*SL	0.121 + 0.017*SL
	t_{PHL}	0.096	0.067 + 0.015*SL	0.073 + 0.013*SL	0.075 + 0.013*SL
C to Y	t_R	0.247	0.177 + 0.035*SL	0.167 + 0.038*SL	0.149 + 0.038*SL
	t_F	0.253	0.204 + 0.025*SL	0.195 + 0.027*SL	0.164 + 0.027*SL
	t_{PLH}	0.181	0.146 + 0.018*SL	0.149 + 0.017*SL	0.152 + 0.017*SL
	t_{PHL}	0.178	0.150 + 0.014*SL	0.153 + 0.013*SL	0.160 + 0.013*SL
D to Y	t_R	0.268	0.197 + 0.035*SL	0.188 + 0.038*SL	0.171 + 0.038*SL
	t_F	0.247	0.196 + 0.025*SL	0.190 + 0.027*SL	0.164 + 0.027*SL
	t_{PLH}	0.196	0.162 + 0.017*SL	0.163 + 0.017*SL	0.165 + 0.017*SL
	t_{PHL}	0.165	0.137 + 0.014*SL	0.140 + 0.013*SL	0.148 + 0.013*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO22D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.095	0.060 + 0.017*SL	0.052 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.081	0.049 + 0.016*SL	0.046 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.293	0.272 + 0.010*SL	0.278 + 0.009*SL	0.280 + 0.009*SL
	t_{PHL}	0.258	0.236 + 0.011*SL	0.245 + 0.009*SL	0.251 + 0.009*SL
B to Y	t_R	0.096	0.061 + 0.017*SL	0.053 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.080	0.047 + 0.016*SL	0.046 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.309	0.289 + 0.010*SL	0.295 + 0.009*SL	0.297 + 0.009*SL
	t_{PHL}	0.246	0.223 + 0.011*SL	0.232 + 0.009*SL	0.238 + 0.009*SL
C to Y	t_R	0.095	0.061 + 0.017*SL	0.053 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.080	0.046 + 0.017*SL	0.047 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.331	0.310 + 0.010*SL	0.316 + 0.009*SL	0.318 + 0.009*SL
	t_{PHL}	0.338	0.316 + 0.011*SL	0.324 + 0.009*SL	0.331 + 0.009*SL
D to Y	t_R	0.096	0.062 + 0.017*SL	0.053 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.080	0.047 + 0.017*SL	0.047 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.347	0.326 + 0.010*SL	0.333 + 0.009*SL	0.334 + 0.009*SL
	t_{PHL}	0.323	0.301 + 0.011*SL	0.310 + 0.009*SL	0.316 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO22D4

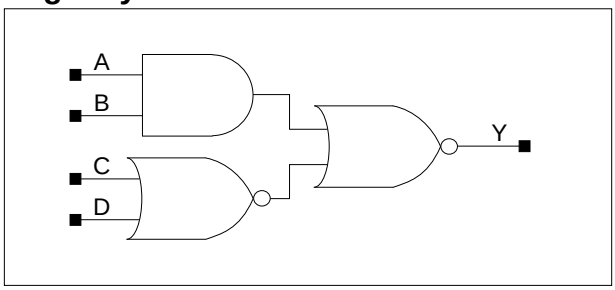
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.093	0.076 + 0.008*SL	0.073 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.080	0.064 + 0.008*SL	0.064 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.331	0.318 + 0.006*SL	0.325 + 0.005*SL	0.335 + 0.004*SL
	t_{PHL}	0.293	0.279 + 0.007*SL	0.288 + 0.005*SL	0.305 + 0.004*SL
B to Y	t_R	0.093	0.075 + 0.009*SL	0.074 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.079	0.062 + 0.009*SL	0.065 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.348	0.336 + 0.006*SL	0.343 + 0.005*SL	0.352 + 0.004*SL
	t_{PHL}	0.281	0.267 + 0.007*SL	0.275 + 0.005*SL	0.293 + 0.004*SL
C to Y	t_R	0.094	0.077 + 0.008*SL	0.073 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.081	0.064 + 0.009*SL	0.066 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.370	0.358 + 0.006*SL	0.365 + 0.005*SL	0.374 + 0.004*SL
	t_{PHL}	0.375	0.361 + 0.007*SL	0.370 + 0.005*SL	0.387 + 0.004*SL
D to Y	t_R	0.093	0.075 + 0.009*SL	0.074 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.081	0.064 + 0.009*SL	0.066 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.387	0.375 + 0.006*SL	0.381 + 0.005*SL	0.391 + 0.004*SL
	t_{PHL}	0.360	0.347 + 0.007*SL	0.355 + 0.005*SL	0.372 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO22A/AO22D2A/AO22D4A

2-AND and 2-NOR into 2-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	0	0	0
Other States				1

Cell Data

Input Load (SL)												Gate Count		
AO22A				*AO22D2A*				*AO22D4A*				*AO22A*	*AO22D2A*	*AO22D4A*
A	B	C	D	A	B	C	D	A	B	C	D			
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	2.67	3.67	4.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.325	0.185 + 0.070*SL	0.166 + 0.075*SL	0.155 + 0.075*SL
	t_F	0.229	0.132 + 0.048*SL	0.113 + 0.053*SL	0.088 + 0.054*SL
	t_{PLH}	0.178	0.114 + 0.032*SL	0.110 + 0.033*SL	0.107 + 0.033*SL
	t_{PHL}	0.138	0.083 + 0.028*SL	0.090 + 0.026*SL	0.089 + 0.026*SL
B to Y	t_R	0.346	0.206 + 0.070*SL	0.187 + 0.075*SL	0.176 + 0.075*SL
	t_F	0.223	0.125 + 0.049*SL	0.106 + 0.054*SL	0.088 + 0.054*SL
	t_{PLH}	0.191	0.128 + 0.032*SL	0.123 + 0.033*SL	0.119 + 0.033*SL
	t_{PHL}	0.124	0.070 + 0.027*SL	0.076 + 0.026*SL	0.076 + 0.026*SL
C to Y	t_R	0.314	0.169 + 0.073*SL	0.160 + 0.075*SL	0.154 + 0.075*SL
	t_F	0.295	0.190 + 0.053*SL	0.185 + 0.054*SL	0.174 + 0.054*SL
	t_{PLH}	0.281	0.213 + 0.034*SL	0.216 + 0.033*SL	0.220 + 0.033*SL
	t_{PHL}	0.283	0.227 + 0.028*SL	0.233 + 0.026*SL	0.242 + 0.026*SL
D to Y	t_R	0.335	0.189 + 0.073*SL	0.181 + 0.075*SL	0.176 + 0.075*SL
	t_F	0.294	0.189 + 0.053*SL	0.184 + 0.054*SL	0.174 + 0.054*SL
	t_{PLH}	0.290	0.223 + 0.034*SL	0.225 + 0.033*SL	0.227 + 0.033*SL
	t_{PHL}	0.278	0.222 + 0.028*SL	0.229 + 0.026*SL	0.237 + 0.026*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO22D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.094	0.060 + 0.017*SL	0.052 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.080	0.048 + 0.016*SL	0.045 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.292	0.272 + 0.010*SL	0.278 + 0.009*SL	0.280 + 0.009*SL
	t_{PHL}	0.258	0.236 + 0.011*SL	0.244 + 0.009*SL	0.250 + 0.009*SL
B to Y	t_R	0.095	0.061 + 0.017*SL	0.052 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.080	0.047 + 0.016*SL	0.045 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.309	0.289 + 0.010*SL	0.295 + 0.009*SL	0.297 + 0.009*SL
	t_{PHL}	0.245	0.223 + 0.011*SL	0.232 + 0.009*SL	0.238 + 0.009*SL
C to Y	t_R	0.094	0.060 + 0.017*SL	0.051 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.081	0.048 + 0.016*SL	0.047 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.394	0.373 + 0.010*SL	0.379 + 0.009*SL	0.381 + 0.009*SL
	t_{PHL}	0.412	0.390 + 0.011*SL	0.399 + 0.009*SL	0.405 + 0.009*SL
D to Y	t_R	0.095	0.061 + 0.017*SL	0.052 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.080	0.047 + 0.016*SL	0.046 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.404	0.383 + 0.010*SL	0.390 + 0.009*SL	0.392 + 0.009*SL
	t_{PHL}	0.406	0.384 + 0.011*SL	0.393 + 0.009*SL	0.399 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO22D4A

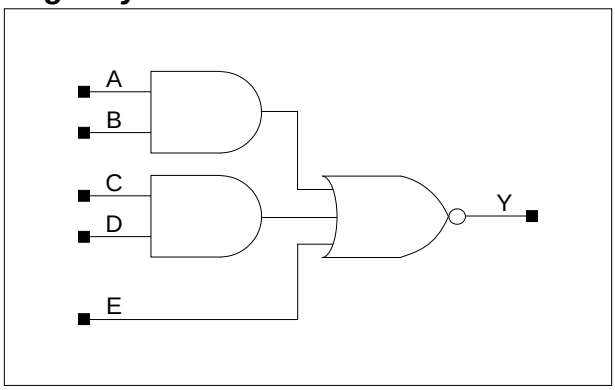
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.094	0.077 + 0.009*SL	0.074 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.080	0.063 + 0.008*SL	0.065 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.333	0.321 + 0.006*SL	0.327 + 0.005*SL	0.337 + 0.004*SL
	t_{PHL}	0.295	0.282 + 0.007*SL	0.290 + 0.005*SL	0.307 + 0.004*SL
B to Y	t_R	0.094	0.077 + 0.009*SL	0.074 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.080	0.064 + 0.008*SL	0.064 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.350	0.338 + 0.006*SL	0.344 + 0.005*SL	0.354 + 0.004*SL
	t_{PHL}	0.283	0.269 + 0.007*SL	0.278 + 0.005*SL	0.295 + 0.004*SL
C to Y	t_R	0.094	0.077 + 0.009*SL	0.074 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.082	0.065 + 0.008*SL	0.066 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.436	0.423 + 0.006*SL	0.430 + 0.005*SL	0.440 + 0.004*SL
	t_{PHL}	0.452	0.438 + 0.007*SL	0.447 + 0.005*SL	0.464 + 0.004*SL
D to Y	t_R	0.094	0.076 + 0.009*SL	0.075 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.082	0.066 + 0.008*SL	0.066 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.448	0.436 + 0.006*SL	0.443 + 0.005*SL	0.452 + 0.004*SL
	t_{PHL}	0.447	0.434 + 0.007*SL	0.442 + 0.005*SL	0.460 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO221/AO221D2/AO221D4

Two 2-ANDs into 3-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	0
x	x	1	1	x	0
x	x	x	x	1	0
Other States					1

Cell Data

Input Load (SL)														
AO221					*AO221D2*					*AO221D4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.9	0.9	0.9	0.9	0.9	1.8	1.8	1.9	1.9	1.8	0.9	0.9	0.9	0.9	0.9
Gate Count														
AO221					*AO221D2*					*AO221D4*				
2.33					3.67					3.67				

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO221

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.511	0.293 + 0.109*SL	0.279 + 0.112*SL	0.296 + 0.112*SL
	t_F	0.263	0.144 + 0.059*SL	0.126 + 0.064*SL	0.109 + 0.064*SL
	t_{PLH}	0.213	0.121 + 0.046*SL	0.108 + 0.049*SL	0.107 + 0.049*SL
	t_{PHL}	0.164	0.101 + 0.032*SL	0.104 + 0.031*SL	0.104 + 0.031*SL
B to Y	t_R	0.542	0.326 + 0.108*SL	0.309 + 0.112*SL	0.327 + 0.112*SL
	t_F	0.257	0.136 + 0.061*SL	0.121 + 0.064*SL	0.109 + 0.064*SL
	t_{PLH}	0.231	0.138 + 0.046*SL	0.128 + 0.049*SL	0.125 + 0.049*SL
	t_{PHL}	0.152	0.089 + 0.032*SL	0.092 + 0.031*SL	0.093 + 0.031*SL
C to Y	t_R	0.537	0.324 + 0.107*SL	0.309 + 0.110*SL	0.298 + 0.111*SL
	t_F	0.362	0.241 + 0.061*SL	0.227 + 0.064*SL	0.212 + 0.064*SL
	t_{PLH}	0.310	0.210 + 0.050*SL	0.215 + 0.049*SL	0.221 + 0.049*SL
	t_{PHL}	0.252	0.188 + 0.032*SL	0.193 + 0.031*SL	0.200 + 0.031*SL
D to Y	t_R	0.568	0.351 + 0.108*SL	0.337 + 0.112*SL	0.327 + 0.112*SL
	t_F	0.360	0.238 + 0.061*SL	0.227 + 0.064*SL	0.212 + 0.064*SL
	t_{PLH}	0.329	0.229 + 0.050*SL	0.233 + 0.049*SL	0.236 + 0.049*SL
	t_{PHL}	0.238	0.173 + 0.032*SL	0.179 + 0.031*SL	0.186 + 0.031*SL
E to Y	t_R	0.566	0.350 + 0.108*SL	0.337 + 0.112*SL	0.327 + 0.112*SL
	t_F	0.304	0.228 + 0.038*SL	0.223 + 0.039*SL	0.203 + 0.040*SL
	t_{PLH}	0.360	0.260 + 0.050*SL	0.264 + 0.049*SL	0.269 + 0.049*SL
	t_{PHL}	0.209	0.161 + 0.024*SL	0.170 + 0.022*SL	0.189 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO221D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.397	0.292 + 0.053*SL	0.282 + 0.055*SL	0.287 + 0.055*SL
	t_F	0.207	0.150 + 0.028*SL	0.136 + 0.032*SL	0.111 + 0.032*SL
	t_{PLH}	0.172	0.129 + 0.022*SL	0.119 + 0.024*SL	0.114 + 0.024*SL
	t_{PHL}	0.133	0.099 + 0.017*SL	0.106 + 0.015*SL	0.106 + 0.015*SL
B to Y	t_R	0.426	0.320 + 0.053*SL	0.308 + 0.056*SL	0.314 + 0.056*SL
	t_F	0.201	0.143 + 0.029*SL	0.130 + 0.032*SL	0.111 + 0.032*SL
	t_{PLH}	0.188	0.145 + 0.022*SL	0.135 + 0.024*SL	0.129 + 0.024*SL
	t_{PHL}	0.120	0.087 + 0.017*SL	0.092 + 0.015*SL	0.093 + 0.015*SL
C to Y	t_R	0.427	0.320 + 0.053*SL	0.309 + 0.056*SL	0.292 + 0.056*SL
	t_F	0.296	0.235 + 0.030*SL	0.227 + 0.032*SL	0.205 + 0.033*SL
	t_{PLH}	0.252	0.201 + 0.026*SL	0.205 + 0.025*SL	0.212 + 0.025*SL
	t_{PHL}	0.216	0.182 + 0.017*SL	0.186 + 0.016*SL	0.194 + 0.016*SL
D to Y	t_R	0.446	0.340 + 0.053*SL	0.330 + 0.055*SL	0.314 + 0.056*SL
	t_F	0.293	0.231 + 0.031*SL	0.225 + 0.032*SL	0.205 + 0.033*SL
	t_{PLH}	0.268	0.218 + 0.025*SL	0.221 + 0.024*SL	0.225 + 0.024*SL
	t_{PHL}	0.203	0.170 + 0.017*SL	0.173 + 0.016*SL	0.182 + 0.016*SL
E to Y	t_R	0.444	0.337 + 0.053*SL	0.329 + 0.055*SL	0.314 + 0.056*SL
	t_F	0.269	0.230 + 0.020*SL	0.227 + 0.020*SL	0.204 + 0.021*SL
	t_{PLH}	0.302	0.251 + 0.025*SL	0.254 + 0.024*SL	0.260 + 0.024*SL
	t_{PHL}	0.188	0.162 + 0.013*SL	0.168 + 0.011*SL	0.190 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO221D4

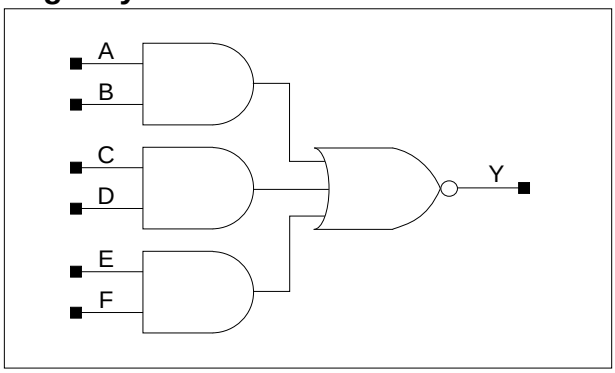
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.100	0.084 + 0.008*SL	0.080 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.081	0.064 + 0.009*SL	0.066 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.379	0.366 + 0.006*SL	0.373 + 0.005*SL	0.384 + 0.004*SL
	t_{PHL}	0.326	0.313 + 0.007*SL	0.321 + 0.005*SL	0.339 + 0.004*SL
B to Y	t_R	0.102	0.085 + 0.008*SL	0.082 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.082	0.065 + 0.008*SL	0.066 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.397	0.384 + 0.006*SL	0.392 + 0.005*SL	0.402 + 0.004*SL
	t_{PHL}	0.312	0.298 + 0.007*SL	0.307 + 0.005*SL	0.324 + 0.004*SL
C to Y	t_R	0.101	0.085 + 0.008*SL	0.080 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.083	0.066 + 0.009*SL	0.068 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.469	0.457 + 0.006*SL	0.464 + 0.005*SL	0.475 + 0.004*SL
	t_{PHL}	0.429	0.415 + 0.007*SL	0.424 + 0.005*SL	0.441 + 0.004*SL
D to Y	t_R	0.101	0.084 + 0.009*SL	0.081 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.084	0.067 + 0.008*SL	0.068 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.493	0.481 + 0.006*SL	0.488 + 0.005*SL	0.498 + 0.004*SL
	t_{PHL}	0.415	0.401 + 0.007*SL	0.410 + 0.005*SL	0.428 + 0.004*SL
E to Y	t_R	0.102	0.085 + 0.008*SL	0.081 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.081	0.065 + 0.008*SL	0.065 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.524	0.512 + 0.006*SL	0.519 + 0.005*SL	0.530 + 0.004*SL
	t_{PHL}	0.381	0.367 + 0.007*SL	0.376 + 0.005*SL	0.393 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO222/AO222D2/AO222D2B/AO222D4

Three 2-ANDs into 3-NOR with 1X/2X/2X(Buffered)/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	x	x	x	x	0
x	x	1	1	x	x	0
x	x	x	x	1	1	0
Other States						1

Cell Data

Input Load (SL)												Gate Count	
AO222						*AO222D2*						*AO222*	*AO222D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.9	0.9	0.9	0.9	0.9	0.9	1.8	1.9	1.9	1.9	1.8	1.9	2.67	4.33
AO222D2B						*AO222D4*						*AO222D2B*	*AO222D4*
A	B	C	D	E	F	A	B	C	D	E	F		
0.9	0.9	0.9	0.9	0.9	1.0	0.9	0.9	0.9	0.9	0.9	1.0	3.33	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.548	0.329 + 0.109*SL	0.317 + 0.112*SL	0.336 + 0.112*SL
	t_F	0.284	0.171 + 0.056*SL	0.152 + 0.061*SL	0.133 + 0.062*SL
	t_{PLH}	0.237	0.142 + 0.047*SL	0.135 + 0.049*SL	0.134 + 0.049*SL
	t_{PHL}	0.168	0.107 + 0.030*SL	0.110 + 0.030*SL	0.110 + 0.030*SL
B to Y	t_R	0.570	0.353 + 0.108*SL	0.340 + 0.111*SL	0.359 + 0.111*SL
	t_F	0.278	0.163 + 0.057*SL	0.147 + 0.061*SL	0.133 + 0.062*SL
	t_{PLH}	0.250	0.156 + 0.047*SL	0.149 + 0.049*SL	0.146 + 0.049*SL
	t_{PHL}	0.153	0.092 + 0.030*SL	0.095 + 0.030*SL	0.096 + 0.030*SL
C to Y	t_R	0.571	0.354 + 0.108*SL	0.341 + 0.112*SL	0.331 + 0.112*SL
	t_F	0.374	0.259 + 0.058*SL	0.244 + 0.061*SL	0.228 + 0.062*SL
	t_{PLH}	0.332	0.231 + 0.050*SL	0.236 + 0.049*SL	0.241 + 0.049*SL
	t_{PHL}	0.251	0.189 + 0.031*SL	0.193 + 0.030*SL	0.200 + 0.030*SL
D to Y	t_R	0.596	0.381 + 0.108*SL	0.369 + 0.111*SL	0.360 + 0.111*SL
	t_F	0.371	0.254 + 0.059*SL	0.243 + 0.061*SL	0.228 + 0.062*SL
	t_{PLH}	0.351	0.252 + 0.050*SL	0.255 + 0.049*SL	0.259 + 0.049*SL
	t_{PHL}	0.239	0.177 + 0.031*SL	0.181 + 0.030*SL	0.188 + 0.030*SL
E to Y	t_R	0.571	0.356 + 0.107*SL	0.343 + 0.111*SL	0.333 + 0.111*SL
	t_F	0.459	0.340 + 0.059*SL	0.334 + 0.061*SL	0.312 + 0.062*SL
	t_{PLH}	0.370	0.270 + 0.050*SL	0.275 + 0.049*SL	0.281 + 0.049*SL
	t_{PHL}	0.296	0.229 + 0.033*SL	0.240 + 0.030*SL	0.261 + 0.030*SL
F to Y	t_R	0.596	0.380 + 0.108*SL	0.369 + 0.111*SL	0.360 + 0.111*SL
	t_F	0.458	0.337 + 0.060*SL	0.335 + 0.061*SL	0.312 + 0.062*SL
	t_{PLH}	0.387	0.288 + 0.050*SL	0.291 + 0.049*SL	0.296 + 0.049*SL
	t_{PHL}	0.281	0.215 + 0.033*SL	0.226 + 0.030*SL	0.248 + 0.030*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.434	0.326 + 0.054*SL	0.317 + 0.056*SL	0.326 + 0.056*SL
	t_F	0.227	0.172 + 0.027*SL	0.159 + 0.031*SL	0.133 + 0.031*SL
	t_{PLH}	0.195	0.149 + 0.023*SL	0.141 + 0.025*SL	0.138 + 0.025*SL
	t_{PHL}	0.137	0.105 + 0.016*SL	0.110 + 0.015*SL	0.110 + 0.015*SL
B to Y	t_R	0.458	0.351 + 0.053*SL	0.342 + 0.056*SL	0.350 + 0.055*SL
	t_F	0.219	0.164 + 0.028*SL	0.152 + 0.031*SL	0.133 + 0.031*SL
	t_{PLH}	0.208	0.163 + 0.023*SL	0.156 + 0.024*SL	0.151 + 0.024*SL
	t_{PHL}	0.123	0.092 + 0.016*SL	0.096 + 0.015*SL	0.097 + 0.015*SL
C to Y	t_R	0.457	0.349 + 0.054*SL	0.340 + 0.056*SL	0.326 + 0.056*SL
	t_F	0.307	0.251 + 0.028*SL	0.241 + 0.031*SL	0.218 + 0.031*SL
	t_{PLH}	0.274	0.224 + 0.025*SL	0.227 + 0.025*SL	0.234 + 0.025*SL
	t_{PHL}	0.214	0.183 + 0.016*SL	0.185 + 0.015*SL	0.192 + 0.015*SL
D to Y	t_R	0.478	0.372 + 0.053*SL	0.363 + 0.055*SL	0.350 + 0.055*SL
	t_F	0.303	0.246 + 0.029*SL	0.238 + 0.031*SL	0.218 + 0.031*SL
	t_{PLH}	0.291	0.241 + 0.025*SL	0.243 + 0.024*SL	0.248 + 0.024*SL
	t_{PHL}	0.200	0.168 + 0.016*SL	0.171 + 0.015*SL	0.179 + 0.015*SL
E to Y	t_R	0.452	0.346 + 0.053*SL	0.338 + 0.055*SL	0.324 + 0.055*SL
	t_F	0.397	0.337 + 0.030*SL	0.333 + 0.031*SL	0.307 + 0.031*SL
	t_{PLH}	0.312	0.262 + 0.025*SL	0.265 + 0.024*SL	0.273 + 0.024*SL
	t_{PHL}	0.259	0.225 + 0.017*SL	0.232 + 0.015*SL	0.257 + 0.015*SL
F to Y	t_R	0.477	0.370 + 0.053*SL	0.363 + 0.055*SL	0.350 + 0.055*SL
	t_F	0.394	0.333 + 0.030*SL	0.332 + 0.031*SL	0.307 + 0.031*SL
	t_{PLH}	0.330	0.279 + 0.025*SL	0.282 + 0.024*SL	0.287 + 0.024*SL
	t_{PHL}	0.245	0.211 + 0.017*SL	0.218 + 0.015*SL	0.244 + 0.015*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO222D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.102	0.067 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.081	0.048 + 0.017*SL	0.048 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.367	0.346 + 0.011*SL	0.353 + 0.009*SL	0.355 + 0.009*SL
	t_{PHL}	0.303	0.281 + 0.011*SL	0.290 + 0.009*SL	0.297 + 0.009*SL
B to Y	t_R	0.102	0.067 + 0.017*SL	0.061 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.082	0.049 + 0.016*SL	0.048 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.385	0.364 + 0.011*SL	0.371 + 0.009*SL	0.373 + 0.009*SL
	t_{PHL}	0.290	0.267 + 0.011*SL	0.277 + 0.009*SL	0.283 + 0.009*SL
C to Y	t_R	0.103	0.069 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.084	0.054 + 0.015*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.460	0.439 + 0.011*SL	0.446 + 0.009*SL	0.448 + 0.009*SL
	t_{PHL}	0.398	0.376 + 0.011*SL	0.385 + 0.009*SL	0.392 + 0.009*SL
D to Y	t_R	0.104	0.070 + 0.017*SL	0.061 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.085	0.053 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.482	0.461 + 0.011*SL	0.468 + 0.009*SL	0.470 + 0.009*SL
	t_{PHL}	0.386	0.364 + 0.011*SL	0.373 + 0.009*SL	0.380 + 0.009*SL
E to Y	t_R	0.103	0.069 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.085	0.053 + 0.016*SL	0.052 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.501	0.480 + 0.011*SL	0.487 + 0.009*SL	0.489 + 0.009*SL
	t_{PHL}	0.457	0.434 + 0.011*SL	0.444 + 0.009*SL	0.450 + 0.009*SL
F to Y	t_R	0.104	0.070 + 0.017*SL	0.061 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.085	0.052 + 0.016*SL	0.052 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.520	0.499 + 0.011*SL	0.507 + 0.009*SL	0.508 + 0.009*SL
	t_{PHL}	0.442	0.420 + 0.011*SL	0.429 + 0.009*SL	0.436 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

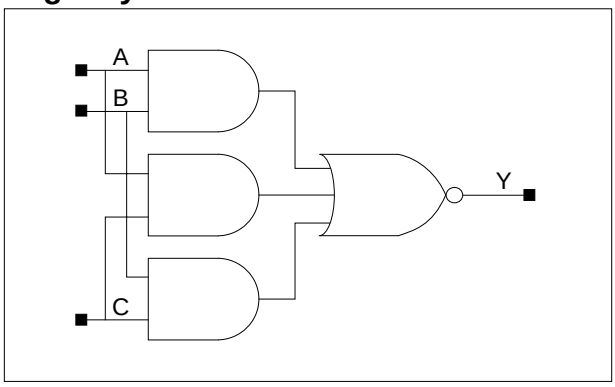
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO222D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.102	0.086 + 0.008*SL	0.081 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.083	0.066 + 0.008*SL	0.067 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.411	0.398 + 0.006*SL	0.406 + 0.005*SL	0.416 + 0.004*SL
	t_{PHL}	0.340	0.327 + 0.007*SL	0.335 + 0.005*SL	0.353 + 0.004*SL
B to Y	t_R	0.103	0.087 + 0.008*SL	0.083 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.082	0.065 + 0.009*SL	0.068 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.428	0.415 + 0.006*SL	0.423 + 0.005*SL	0.433 + 0.004*SL
	t_{PHL}	0.326	0.312 + 0.007*SL	0.321 + 0.005*SL	0.338 + 0.004*SL
C to Y	t_R	0.103	0.087 + 0.008*SL	0.082 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.084	0.067 + 0.008*SL	0.069 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.509	0.496 + 0.006*SL	0.504 + 0.005*SL	0.514 + 0.004*SL
	t_{PHL}	0.440	0.427 + 0.007*SL	0.435 + 0.005*SL	0.453 + 0.004*SL
D to Y	t_R	0.103	0.086 + 0.008*SL	0.083 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.084	0.068 + 0.008*SL	0.069 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.534	0.521 + 0.006*SL	0.529 + 0.005*SL	0.539 + 0.004*SL
	t_{PHL}	0.430	0.416 + 0.007*SL	0.424 + 0.005*SL	0.442 + 0.004*SL
E to Y	t_R	0.103	0.086 + 0.008*SL	0.083 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.086	0.069 + 0.008*SL	0.071 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.549	0.536 + 0.006*SL	0.544 + 0.005*SL	0.554 + 0.004*SL
	t_{PHL}	0.498	0.484 + 0.007*SL	0.493 + 0.005*SL	0.511 + 0.004*SL
F to Y	t_R	0.104	0.087 + 0.008*SL	0.084 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.087	0.070 + 0.008*SL	0.072 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.570	0.557 + 0.006*SL	0.565 + 0.005*SL	0.575 + 0.004*SL
	t_{PHL}	0.484	0.470 + 0.007*SL	0.479 + 0.005*SL	0.497 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	Y
1	1	x	0
1	x	1	0
x	1	1	0
0	0	x	1
0	x	0	1
x	0	0	1

Cell Data

Input Load (SL)									Gate Count		
AO222A			*AO222D2A*			*AO222D4A*			*AO222A*	*AO222D2A*	*AO222D4A*
A	B	C	A	B	C	A	B	C			
1.7	1.9	1.9	1.7	1.9	1.9	1.7	1.9	1.9	2.00	3.00	3.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO222A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.424	0.282 + 0.071*SL	0.271 + 0.074*SL	0.268 + 0.074*SL
	t_F	0.308	0.197 + 0.055*SL	0.187 + 0.058*SL	0.179 + 0.058*SL
	t_{PLH}	0.213	0.148 + 0.032*SL	0.147 + 0.033*SL	0.151 + 0.033*SL
	t_{PHL}	0.222	0.164 + 0.029*SL	0.168 + 0.028*SL	0.174 + 0.028*SL
B to Y	t_R	0.375	0.235 + 0.070*SL	0.221 + 0.074*SL	0.212 + 0.074*SL
	t_F	0.334	0.224 + 0.055*SL	0.213 + 0.058*SL	0.203 + 0.058*SL
	t_{PLH}	0.226	0.161 + 0.032*SL	0.160 + 0.033*SL	0.159 + 0.033*SL
	t_{PHL}	0.251	0.193 + 0.029*SL	0.197 + 0.028*SL	0.203 + 0.028*SL
C to Y	t_R	0.376	0.234 + 0.071*SL	0.223 + 0.074*SL	0.212 + 0.074*SL
	t_F	0.340	0.231 + 0.055*SL	0.218 + 0.058*SL	0.203 + 0.058*SL
	t_{PLH}	0.222	0.158 + 0.032*SL	0.157 + 0.033*SL	0.156 + 0.033*SL
	t_{PHL}	0.215	0.158 + 0.029*SL	0.160 + 0.028*SL	0.163 + 0.028*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO222D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.101	0.066 + 0.018*SL	0.059 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.082	0.049 + 0.016*SL	0.049 + 0.016*SL	0.026 + 0.017*SL
	t_{PLH}	0.350	0.329 + 0.010*SL	0.336 + 0.009*SL	0.338 + 0.009*SL
	t_{PHL}	0.361	0.339 + 0.011*SL	0.348 + 0.009*SL	0.355 + 0.009*SL
B to Y	t_R	0.097	0.063 + 0.017*SL	0.054 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.083	0.051 + 0.016*SL	0.049 + 0.016*SL	0.026 + 0.017*SL
	t_{PLH}	0.352	0.331 + 0.010*SL	0.338 + 0.009*SL	0.339 + 0.009*SL
	t_{PHL}	0.396	0.373 + 0.011*SL	0.383 + 0.009*SL	0.389 + 0.009*SL
C to Y	t_R	0.099	0.064 + 0.018*SL	0.057 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.081	0.048 + 0.016*SL	0.049 + 0.016*SL	0.026 + 0.017*SL
	t_{PLH}	0.354	0.333 + 0.010*SL	0.340 + 0.009*SL	0.341 + 0.009*SL
	t_{PHL}	0.361	0.339 + 0.011*SL	0.348 + 0.009*SL	0.355 + 0.009*SL

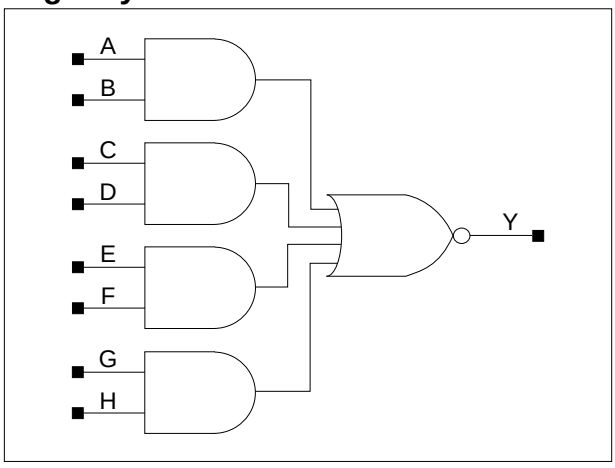
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO222D4A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.102	0.086 + 0.008*SL	0.081 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.083	0.067 + 0.008*SL	0.067 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.394	0.381 + 0.006*SL	0.389 + 0.005*SL	0.399 + 0.004*SL
	t_{PHL}	0.399	0.385 + 0.007*SL	0.394 + 0.005*SL	0.411 + 0.004*SL
B to Y	t_R	0.101	0.085 + 0.008*SL	0.081 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.083	0.066 + 0.008*SL	0.067 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.394	0.381 + 0.006*SL	0.389 + 0.005*SL	0.399 + 0.004*SL
	t_{PHL}	0.432	0.419 + 0.007*SL	0.427 + 0.005*SL	0.445 + 0.004*SL
C to Y	t_R	0.099	0.083 + 0.008*SL	0.079 + 0.009*SL	0.049 + 0.010*SL
	t_F	0.083	0.067 + 0.008*SL	0.067 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.396	0.383 + 0.006*SL	0.390 + 0.005*SL	0.400 + 0.004*SL
	t_{PHL}	0.396	0.382 + 0.007*SL	0.391 + 0.005*SL	0.408 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	x	x	x	x	x	x	0
x	x	1	1	x	x	x	x	0
x	x	x	x	1	1	x	x	0
x	x	x	x	x	x	1	1	0
Other States								1

Cell Data

Input Load (SL)								Gate Count
AO2222								*AO2222*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	3.00
AO2222D2								*AO2222D2*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	4.33
AO2222D4								*AO2222D4*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	5.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO2222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.760	0.460 + 0.150*SL	0.457 + 0.151*SL	0.521 + 0.149*SL
	t_F	0.317	0.197 + 0.060*SL	0.179 + 0.065*SL	0.162 + 0.065*SL
	t_{PLH}	0.259	0.140 + 0.059*SL	0.116 + 0.065*SL	0.116 + 0.065*SL
	t_{PHL}	0.182	0.119 + 0.031*SL	0.120 + 0.031*SL	0.120 + 0.031*SL
B to Y	t_R	0.800	0.501 + 0.149*SL	0.495 + 0.151*SL	0.560 + 0.149*SL
	t_F	0.311	0.188 + 0.061*SL	0.175 + 0.065*SL	0.162 + 0.065*SL
	t_{PLH}	0.280	0.159 + 0.060*SL	0.139 + 0.065*SL	0.137 + 0.065*SL
	t_{PHL}	0.170	0.106 + 0.032*SL	0.108 + 0.031*SL	0.109 + 0.031*SL
C to Y	t_R	0.832	0.540 + 0.146*SL	0.529 + 0.149*SL	0.522 + 0.149*SL
	t_F	0.406	0.285 + 0.061*SL	0.271 + 0.064*SL	0.257 + 0.064*SL
	t_{PLH}	0.403	0.269 + 0.067*SL	0.275 + 0.066*SL	0.286 + 0.065*SL
	t_{PHL}	0.267	0.203 + 0.032*SL	0.207 + 0.031*SL	0.213 + 0.031*SL
D to Y	t_R	0.871	0.578 + 0.146*SL	0.569 + 0.149*SL	0.563 + 0.149*SL
	t_F	0.404	0.281 + 0.061*SL	0.271 + 0.064*SL	0.257 + 0.064*SL
	t_{PLH}	0.431	0.297 + 0.067*SL	0.302 + 0.065*SL	0.309 + 0.065*SL
	t_{PHL}	0.255	0.191 + 0.032*SL	0.195 + 0.031*SL	0.202 + 0.031*SL
E to Y	t_R	0.882	0.592 + 0.145*SL	0.577 + 0.148*SL	0.563 + 0.149*SL
	t_F	0.501	0.379 + 0.061*SL	0.368 + 0.064*SL	0.348 + 0.064*SL
	t_{PLH}	0.522	0.387 + 0.067*SL	0.394 + 0.066*SL	0.405 + 0.065*SL
	t_{PHL}	0.311	0.243 + 0.034*SL	0.252 + 0.032*SL	0.270 + 0.031*SL
F to Y	t_R	0.915	0.625 + 0.145*SL	0.612 + 0.149*SL	0.598 + 0.149*SL
	t_F	0.500	0.376 + 0.062*SL	0.369 + 0.064*SL	0.348 + 0.064*SL
	t_{PLH}	0.547	0.413 + 0.067*SL	0.418 + 0.066*SL	0.426 + 0.065*SL
	t_{PHL}	0.298	0.230 + 0.034*SL	0.239 + 0.032*SL	0.258 + 0.031*SL
G to Y	t_R	0.882	0.592 + 0.145*SL	0.578 + 0.148*SL	0.563 + 0.149*SL
	t_F	0.607	0.479 + 0.064*SL	0.476 + 0.065*SL	0.468 + 0.065*SL
	t_{PLH}	0.577	0.442 + 0.067*SL	0.449 + 0.066*SL	0.460 + 0.065*SL
	t_{PHL}	0.342	0.269 + 0.037*SL	0.285 + 0.033*SL	0.327 + 0.032*SL
H to Y	t_R	0.915	0.625 + 0.145*SL	0.612 + 0.149*SL	0.598 + 0.149*SL
	t_F	0.605	0.475 + 0.065*SL	0.476 + 0.065*SL	0.468 + 0.065*SL
	t_{PLH}	0.600	0.466 + 0.067*SL	0.472 + 0.065*SL	0.479 + 0.065*SL
	t_{PHL}	0.330	0.256 + 0.037*SL	0.273 + 0.033*SL	0.316 + 0.032*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO2222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.106	0.072 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.083	0.052 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.383	0.362 + 0.011*SL	0.369 + 0.009*SL	0.372 + 0.009*SL
	t_{PHL}	0.317	0.295 + 0.011*SL	0.304 + 0.009*SL	0.311 + 0.009*SL
B to Y	t_R	0.108	0.074 + 0.017*SL	0.065 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.082	0.050 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.408	0.387 + 0.011*SL	0.395 + 0.009*SL	0.397 + 0.009*SL
	t_{PHL}	0.306	0.284 + 0.011*SL	0.293 + 0.009*SL	0.300 + 0.009*SL
C to Y	t_R	0.109	0.075 + 0.017*SL	0.066 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.085	0.053 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.527	0.506 + 0.011*SL	0.514 + 0.009*SL	0.516 + 0.009*SL
	t_{PHL}	0.418	0.395 + 0.011*SL	0.405 + 0.009*SL	0.411 + 0.009*SL
D to Y	t_R	0.110	0.076 + 0.017*SL	0.069 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.085	0.054 + 0.015*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.558	0.536 + 0.011*SL	0.544 + 0.009*SL	0.546 + 0.009*SL
	t_{PHL}	0.406	0.383 + 0.011*SL	0.393 + 0.009*SL	0.399 + 0.009*SL
E to Y	t_R	0.111	0.077 + 0.017*SL	0.068 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.087	0.056 + 0.015*SL	0.052 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.648	0.627 + 0.011*SL	0.635 + 0.009*SL	0.637 + 0.009*SL
	t_{PHL}	0.475	0.452 + 0.011*SL	0.462 + 0.009*SL	0.468 + 0.009*SL
F to Y	t_R	0.112	0.079 + 0.017*SL	0.070 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.087	0.056 + 0.016*SL	0.052 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.675	0.654 + 0.011*SL	0.662 + 0.009*SL	0.665 + 0.009*SL
	t_{PHL}	0.462	0.439 + 0.011*SL	0.448 + 0.009*SL	0.455 + 0.009*SL
G to Y	t_R	0.111	0.077 + 0.017*SL	0.068 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.090	0.059 + 0.015*SL	0.055 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.703	0.681 + 0.011*SL	0.690 + 0.009*SL	0.692 + 0.009*SL
	t_{PHL}	0.520	0.497 + 0.011*SL	0.507 + 0.009*SL	0.514 + 0.009*SL
H to Y	t_R	0.112	0.079 + 0.017*SL	0.069 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.090	0.060 + 0.015*SL	0.055 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.729	0.707 + 0.011*SL	0.716 + 0.009*SL	0.718 + 0.009*SL
	t_{PHL}	0.508	0.485 + 0.011*SL	0.495 + 0.009*SL	0.502 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

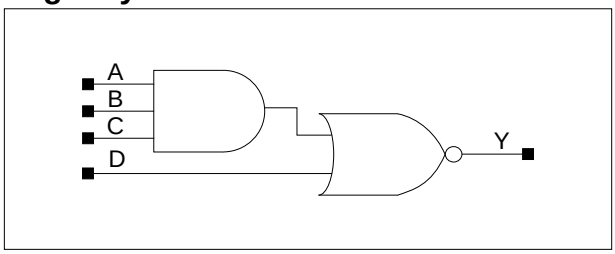
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO2222D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.108	0.093 + 0.008*SL	0.087 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.084	0.067 + 0.008*SL	0.069 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.432	0.419 + 0.007*SL	0.427 + 0.005*SL	0.439 + 0.004*SL
	t_{PHL}	0.355	0.341 + 0.007*SL	0.350 + 0.005*SL	0.367 + 0.004*SL
B to Y	t_R	0.109	0.093 + 0.008*SL	0.089 + 0.009*SL	0.054 + 0.010*SL
	t_F	0.084	0.068 + 0.008*SL	0.068 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.458	0.445 + 0.007*SL	0.453 + 0.005*SL	0.464 + 0.004*SL
	t_{PHL}	0.343	0.329 + 0.007*SL	0.338 + 0.005*SL	0.356 + 0.004*SL
C to Y	t_R	0.111	0.095 + 0.008*SL	0.090 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.085	0.068 + 0.008*SL	0.070 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.576	0.563 + 0.007*SL	0.571 + 0.005*SL	0.582 + 0.004*SL
	t_{PHL}	0.455	0.441 + 0.007*SL	0.450 + 0.005*SL	0.467 + 0.004*SL
D to Y	t_R	0.113	0.096 + 0.008*SL	0.093 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.085	0.069 + 0.008*SL	0.070 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.607	0.594 + 0.007*SL	0.603 + 0.005*SL	0.614 + 0.004*SL
	t_{PHL}	0.443	0.429 + 0.007*SL	0.438 + 0.005*SL	0.455 + 0.004*SL
E to Y	t_R	0.112	0.096 + 0.008*SL	0.092 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.088	0.072 + 0.008*SL	0.073 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.698	0.685 + 0.007*SL	0.693 + 0.005*SL	0.705 + 0.004*SL
	t_{PHL}	0.514	0.500 + 0.007*SL	0.509 + 0.005*SL	0.526 + 0.004*SL
F to Y	t_R	0.114	0.097 + 0.008*SL	0.094 + 0.009*SL	0.056 + 0.010*SL
	t_F	0.088	0.072 + 0.008*SL	0.073 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.726	0.713 + 0.007*SL	0.722 + 0.005*SL	0.733 + 0.004*SL
	t_{PHL}	0.501	0.487 + 0.007*SL	0.496 + 0.005*SL	0.513 + 0.004*SL
G to Y	t_R	0.113	0.097 + 0.008*SL	0.093 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.092	0.075 + 0.008*SL	0.077 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.753	0.739 + 0.007*SL	0.748 + 0.005*SL	0.759 + 0.004*SL
	t_{PHL}	0.562	0.548 + 0.007*SL	0.557 + 0.005*SL	0.575 + 0.004*SL
H to Y	t_R	0.114	0.097 + 0.008*SL	0.094 + 0.009*SL	0.056 + 0.010*SL
	t_F	0.093	0.076 + 0.008*SL	0.078 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.780	0.766 + 0.007*SL	0.775 + 0.005*SL	0.787 + 0.004*SL
	t_{PHL}	0.550	0.536 + 0.007*SL	0.545 + 0.005*SL	0.563 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	1	x	0
x	x	x	1	0
Other States				1

Cell Data

Input Load (SL)												Gate Count		
AO31				*AO31D2*				*AO31D4*				*AO31*	*AO31D2*	*AO31D4*
A	B	C	D	A	B	C	D	A	B	C	D			
1.0	1.0	1.0	0.9	2.0	2.1	2.1	1.9	1.0	1.0	1.0	1.0	1.67	2.67	3.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO31

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.339	0.201 + 0.069*SL	0.182 + 0.074*SL	0.169 + 0.074*SL
	t_F	0.298	0.166 + 0.066*SL	0.150 + 0.070*SL	0.136 + 0.070*SL
	t_{PLH}	0.182	0.118 + 0.032*SL	0.115 + 0.033*SL	0.114 + 0.033*SL
	t_{PHL}	0.176	0.112 + 0.032*SL	0.112 + 0.032*SL	0.112 + 0.032*SL
B to Y	t_R	0.368	0.229 + 0.070*SL	0.209 + 0.075*SL	0.196 + 0.075*SL
	t_F	0.295	0.162 + 0.067*SL	0.148 + 0.070*SL	0.136 + 0.070*SL
	t_{PLH}	0.200	0.135 + 0.032*SL	0.132 + 0.033*SL	0.130 + 0.033*SL
	t_{PHL}	0.172	0.107 + 0.033*SL	0.109 + 0.032*SL	0.110 + 0.032*SL
C to Y	t_R	0.396	0.258 + 0.069*SL	0.236 + 0.075*SL	0.221 + 0.075*SL
	t_F	0.290	0.155 + 0.068*SL	0.145 + 0.070*SL	0.136 + 0.070*SL
	t_{PLH}	0.213	0.149 + 0.032*SL	0.146 + 0.033*SL	0.144 + 0.033*SL
	t_{PHL}	0.165	0.100 + 0.033*SL	0.102 + 0.032*SL	0.104 + 0.032*SL
D to Y	t_R	0.387	0.243 + 0.072*SL	0.232 + 0.075*SL	0.221 + 0.075*SL
	t_F	0.258	0.185 + 0.036*SL	0.173 + 0.039*SL	0.152 + 0.040*SL
	t_{PLH}	0.243	0.176 + 0.033*SL	0.178 + 0.033*SL	0.180 + 0.033*SL
	t_{PHL}	0.198	0.155 + 0.022*SL	0.157 + 0.021*SL	0.159 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO31D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.271	0.205 + 0.033*SL	0.190 + 0.037*SL	0.169 + 0.037*SL
	t_F	0.234	0.169 + 0.033*SL	0.158 + 0.035*SL	0.137 + 0.036*SL
	t_{PLH}	0.148	0.115 + 0.016*SL	0.116 + 0.016*SL	0.113 + 0.016*SL
	t_{PHL}	0.145	0.110 + 0.017*SL	0.113 + 0.016*SL	0.113 + 0.016*SL
B to Y	t_R	0.297	0.229 + 0.034*SL	0.216 + 0.037*SL	0.195 + 0.038*SL
	t_F	0.230	0.165 + 0.033*SL	0.154 + 0.035*SL	0.137 + 0.036*SL
	t_{PLH}	0.166	0.134 + 0.016*SL	0.133 + 0.016*SL	0.129 + 0.017*SL
	t_{PHL}	0.140	0.105 + 0.017*SL	0.109 + 0.016*SL	0.110 + 0.016*SL
C to Y	t_R	0.324	0.258 + 0.033*SL	0.242 + 0.037*SL	0.218 + 0.038*SL
	t_F	0.225	0.158 + 0.034*SL	0.150 + 0.035*SL	0.137 + 0.036*SL
	t_{PLH}	0.180	0.148 + 0.016*SL	0.147 + 0.016*SL	0.144 + 0.017*SL
	t_{PHL}	0.134	0.100 + 0.017*SL	0.104 + 0.016*SL	0.106 + 0.016*SL
D to Y	t_R	0.312	0.241 + 0.035*SL	0.234 + 0.037*SL	0.218 + 0.038*SL
	t_F	0.222	0.186 + 0.018*SL	0.179 + 0.020*SL	0.152 + 0.020*SL
	t_{PLH}	0.208	0.174 + 0.017*SL	0.175 + 0.017*SL	0.177 + 0.017*SL
	t_{PHL}	0.176	0.154 + 0.011*SL	0.155 + 0.011*SL	0.159 + 0.011*SL

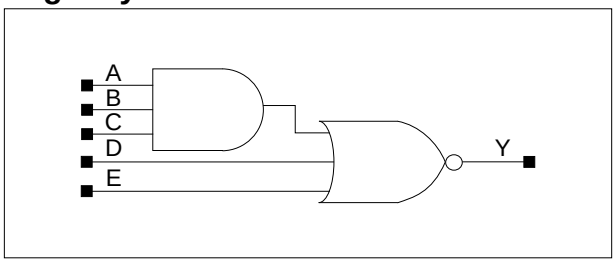
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO31D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.096	0.079 + 0.009*SL	0.076 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.083	0.066 + 0.009*SL	0.068 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.342	0.330 + 0.006*SL	0.337 + 0.005*SL	0.347 + 0.004*SL
	t_{PHL}	0.342	0.329 + 0.007*SL	0.337 + 0.005*SL	0.355 + 0.004*SL
B to Y	t_R	0.097	0.080 + 0.009*SL	0.077 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.083	0.066 + 0.008*SL	0.068 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.363	0.350 + 0.006*SL	0.357 + 0.005*SL	0.367 + 0.004*SL
	t_{PHL}	0.338	0.325 + 0.007*SL	0.333 + 0.005*SL	0.351 + 0.004*SL
C to Y	t_R	0.097	0.080 + 0.008*SL	0.076 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.084	0.067 + 0.008*SL	0.068 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.379	0.367 + 0.006*SL	0.374 + 0.005*SL	0.384 + 0.004*SL
	t_{PHL}	0.332	0.318 + 0.007*SL	0.327 + 0.005*SL	0.344 + 0.004*SL
D to Y	t_R	0.097	0.080 + 0.009*SL	0.077 + 0.009*SL	0.049 + 0.010*SL
	t_F	0.080	0.064 + 0.008*SL	0.064 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.409	0.397 + 0.006*SL	0.404 + 0.005*SL	0.414 + 0.004*SL
	t_{PHL}	0.366	0.353 + 0.007*SL	0.361 + 0.005*SL	0.378 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0
Other States					1

Cell Data

Input Load (SL)														
AO311					*AO311D2*					*AO311D4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.9	0.9	0.9	0.9	1.0	1.9	1.9	2.0	1.9	1.9	0.9	0.9	0.9	0.9	1.0

Gate Count		
AO311	*AO311D2*	*AO311D4*
2.00	3.33	3.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO311

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.525	0.313 + 0.106*SL	0.298 + 0.110*SL	0.305 + 0.110*SL
	t_F	0.362	0.194 + 0.084*SL	0.181 + 0.087*SL	0.173 + 0.088*SL
	t_{PLH}	0.224	0.130 + 0.047*SL	0.124 + 0.048*SL	0.123 + 0.048*SL
	t_{PHL}	0.218	0.137 + 0.040*SL	0.137 + 0.040*SL	0.138 + 0.040*SL
B to Y	t_R	0.557	0.344 + 0.107*SL	0.327 + 0.111*SL	0.334 + 0.111*SL
	t_F	0.360	0.191 + 0.085*SL	0.181 + 0.087*SL	0.173 + 0.088*SL
	t_{PLH}	0.242	0.147 + 0.047*SL	0.143 + 0.049*SL	0.141 + 0.049*SL
	t_{PHL}	0.213	0.132 + 0.040*SL	0.132 + 0.040*SL	0.134 + 0.040*SL
C to Y	t_R	0.588	0.376 + 0.106*SL	0.356 + 0.111*SL	0.362 + 0.111*SL
	t_F	0.358	0.187 + 0.085*SL	0.179 + 0.087*SL	0.173 + 0.088*SL
	t_{PLH}	0.258	0.163 + 0.048*SL	0.159 + 0.049*SL	0.158 + 0.049*SL
	t_{PHL}	0.207	0.126 + 0.041*SL	0.127 + 0.040*SL	0.129 + 0.040*SL
D to Y	t_R	0.599	0.384 + 0.107*SL	0.371 + 0.110*SL	0.362 + 0.111*SL
	t_F	0.258	0.186 + 0.036*SL	0.175 + 0.039*SL	0.155 + 0.039*SL
	t_{PLH}	0.338	0.239 + 0.049*SL	0.242 + 0.049*SL	0.246 + 0.049*SL
	t_{PHL}	0.200	0.157 + 0.021*SL	0.159 + 0.021*SL	0.163 + 0.021*SL
E to Y	t_R	0.597	0.381 + 0.108*SL	0.370 + 0.110*SL	0.362 + 0.111*SL
	t_F	0.292	0.219 + 0.036*SL	0.210 + 0.039*SL	0.187 + 0.039*SL
	t_{PLH}	0.349	0.250 + 0.050*SL	0.253 + 0.049*SL	0.258 + 0.049*SL
	t_{PHL}	0.214	0.170 + 0.022*SL	0.174 + 0.021*SL	0.182 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO311D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.423	0.319 + 0.052*SL	0.308 + 0.055*SL	0.308 + 0.055*SL
	t_F	0.281	0.199 + 0.041*SL	0.189 + 0.044*SL	0.175 + 0.044*SL
	t_{PLH}	0.179	0.134 + 0.022*SL	0.127 + 0.024*SL	0.125 + 0.024*SL
	t_{PHL}	0.180	0.139 + 0.020*SL	0.139 + 0.020*SL	0.140 + 0.020*SL
B to Y	t_R	0.454	0.349 + 0.052*SL	0.337 + 0.055*SL	0.337 + 0.055*SL
	t_F	0.278	0.195 + 0.042*SL	0.187 + 0.044*SL	0.175 + 0.044*SL
	t_{PLH}	0.198	0.153 + 0.023*SL	0.147 + 0.024*SL	0.144 + 0.024*SL
	t_{PHL}	0.175	0.134 + 0.020*SL	0.135 + 0.020*SL	0.138 + 0.020*SL
C to Y	t_R	0.483	0.380 + 0.052*SL	0.366 + 0.055*SL	0.363 + 0.055*SL
	t_F	0.276	0.191 + 0.042*SL	0.185 + 0.044*SL	0.175 + 0.044*SL
	t_{PLH}	0.213	0.167 + 0.023*SL	0.163 + 0.024*SL	0.161 + 0.024*SL
	t_{PHL}	0.170	0.128 + 0.021*SL	0.130 + 0.020*SL	0.133 + 0.020*SL
D to Y	t_R	0.493	0.387 + 0.053*SL	0.378 + 0.055*SL	0.363 + 0.055*SL
	t_F	0.218	0.183 + 0.017*SL	0.178 + 0.019*SL	0.151 + 0.019*SL
	t_{PLH}	0.286	0.237 + 0.025*SL	0.239 + 0.024*SL	0.244 + 0.024*SL
	t_{PHL}	0.175	0.154 + 0.010*SL	0.155 + 0.010*SL	0.159 + 0.010*SL
E to Y	t_R	0.490	0.384 + 0.053*SL	0.376 + 0.055*SL	0.363 + 0.055*SL
	t_F	0.257	0.221 + 0.018*SL	0.216 + 0.019*SL	0.188 + 0.020*SL
	t_{PLH}	0.298	0.248 + 0.025*SL	0.251 + 0.024*SL	0.256 + 0.024*SL
	t_{PHL}	0.192	0.170 + 0.011*SL	0.173 + 0.011*SL	0.182 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

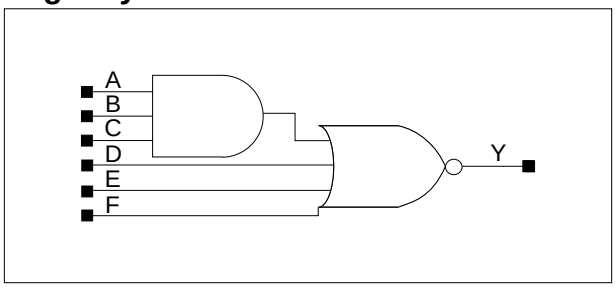
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO311D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.102	0.085 + 0.008*SL	0.081 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.085	0.069 + 0.008*SL	0.069 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.392	0.379 + 0.006*SL	0.387 + 0.005*SL	0.397 + 0.004*SL
	t_{PHL}	0.385	0.371 + 0.007*SL	0.380 + 0.005*SL	0.398 + 0.004*SL
B to Y	t_R	0.103	0.086 + 0.008*SL	0.083 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.085	0.069 + 0.008*SL	0.070 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.414	0.401 + 0.006*SL	0.408 + 0.005*SL	0.419 + 0.004*SL
	t_{PHL}	0.380	0.366 + 0.007*SL	0.375 + 0.005*SL	0.393 + 0.004*SL
C to Y	t_R	0.104	0.088 + 0.008*SL	0.083 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.085	0.068 + 0.008*SL	0.070 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.433	0.420 + 0.006*SL	0.427 + 0.005*SL	0.438 + 0.004*SL
	t_{PHL}	0.374	0.360 + 0.007*SL	0.369 + 0.005*SL	0.386 + 0.004*SL
D to Y	t_R	0.104	0.088 + 0.008*SL	0.084 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.079	0.063 + 0.008*SL	0.063 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.509	0.496 + 0.006*SL	0.504 + 0.005*SL	0.515 + 0.004*SL
	t_{PHL}	0.363	0.349 + 0.007*SL	0.358 + 0.005*SL	0.375 + 0.004*SL
E to Y	t_R	0.104	0.089 + 0.008*SL	0.083 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.080	0.064 + 0.008*SL	0.064 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.521	0.508 + 0.006*SL	0.516 + 0.005*SL	0.527 + 0.004*SL
	t_{PHL}	0.383	0.370 + 0.007*SL	0.378 + 0.005*SL	0.395 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	x	x	0
x	x	x	x	1	x	0
x	x	x	x	x	1	0
Other States						1

Cell Data

Input Load (SL)												Gate Count	
AO3111						*AO3111D2*						*AO3111*	*AO3111*D2
A	B	C	D	E	F	A	B	C	D	E	F		
0.9	0.9	0.9	0.9	0.9	0.9	1.9	2.0	2.0	1.9	1.9	1.9	2.33	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO3111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.726	0.437 + 0.144*SL	0.429 + 0.146*SL	0.466 + 0.145*SL
	t_F	0.375	0.201 + 0.087*SL	0.189 + 0.090*SL	0.182 + 0.090*SL
	t_{PLH}	0.254	0.133 + 0.061*SL	0.120 + 0.064*SL	0.121 + 0.064*SL
	t_{PHL}	0.226	0.143 + 0.042*SL	0.143 + 0.042*SL	0.144 + 0.042*SL
B to Y	t_R	0.765	0.475 + 0.145*SL	0.465 + 0.147*SL	0.502 + 0.146*SL
	t_F	0.374	0.199 + 0.088*SL	0.189 + 0.090*SL	0.182 + 0.090*SL
	t_{PLH}	0.276	0.152 + 0.062*SL	0.143 + 0.064*SL	0.142 + 0.064*SL
	t_{PHL}	0.222	0.138 + 0.042*SL	0.139 + 0.042*SL	0.140 + 0.042*SL
C to Y	t_R	0.803	0.515 + 0.144*SL	0.501 + 0.147*SL	0.536 + 0.146*SL
	t_F	0.372	0.195 + 0.088*SL	0.188 + 0.090*SL	0.182 + 0.090*SL
	t_{PLH}	0.296	0.171 + 0.063*SL	0.164 + 0.064*SL	0.163 + 0.064*SL
	t_{PHL}	0.216	0.132 + 0.042*SL	0.133 + 0.042*SL	0.136 + 0.042*SL
D to Y	t_R	0.843	0.557 + 0.143*SL	0.545 + 0.146*SL	0.537 + 0.146*SL
	t_F	0.267	0.192 + 0.038*SL	0.181 + 0.040*SL	0.163 + 0.041*SL
	t_{PLH}	0.422	0.291 + 0.066*SL	0.295 + 0.064*SL	0.302 + 0.064*SL
	t_{PHL}	0.210	0.165 + 0.022*SL	0.167 + 0.022*SL	0.171 + 0.022*SL
E to Y	t_R	0.846	0.560 + 0.143*SL	0.547 + 0.146*SL	0.537 + 0.146*SL
	t_F	0.304	0.227 + 0.039*SL	0.219 + 0.040*SL	0.199 + 0.041*SL
	t_{PLH}	0.467	0.335 + 0.066*SL	0.340 + 0.065*SL	0.348 + 0.064*SL
	t_{PHL}	0.228	0.182 + 0.023*SL	0.186 + 0.022*SL	0.195 + 0.022*SL
F to Y	t_R	0.844	0.558 + 0.143*SL	0.546 + 0.146*SL	0.537 + 0.146*SL
	t_F	0.335	0.256 + 0.040*SL	0.253 + 0.040*SL	0.238 + 0.041*SL
	t_{PLH}	0.486	0.355 + 0.066*SL	0.360 + 0.065*SL	0.368 + 0.064*SL
	t_{PHL}	0.237	0.189 + 0.024*SL	0.197 + 0.022*SL	0.214 + 0.022*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO3111D2

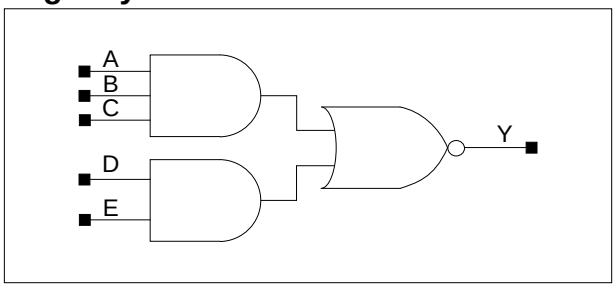
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.593	0.451 + 0.071*SL	0.445 + 0.073*SL	0.480 + 0.072*SL
	t_F	0.299	0.213 + 0.043*SL	0.205 + 0.045*SL	0.193 + 0.045*SL
	t_{PLH}	0.200	0.144 + 0.028*SL	0.128 + 0.032*SL	0.125 + 0.032*SL
	t_{PHL}	0.189	0.148 + 0.021*SL	0.148 + 0.021*SL	0.149 + 0.021*SL
B to Y	t_R	0.633	0.491 + 0.071*SL	0.483 + 0.073*SL	0.516 + 0.073*SL
	t_F	0.297	0.211 + 0.043*SL	0.203 + 0.045*SL	0.193 + 0.045*SL
	t_{PLH}	0.222	0.164 + 0.029*SL	0.153 + 0.032*SL	0.150 + 0.032*SL
	t_{PHL}	0.186	0.144 + 0.021*SL	0.144 + 0.021*SL	0.147 + 0.021*SL
C to Y	t_R	0.670	0.529 + 0.070*SL	0.519 + 0.073*SL	0.550 + 0.073*SL
	t_F	0.295	0.208 + 0.044*SL	0.202 + 0.045*SL	0.193 + 0.045*SL
	t_{PLH}	0.241	0.182 + 0.030*SL	0.173 + 0.032*SL	0.172 + 0.032*SL
	t_{PHL}	0.181	0.139 + 0.021*SL	0.140 + 0.021*SL	0.143 + 0.021*SL
D to Y	t_R	0.712	0.572 + 0.070*SL	0.563 + 0.072*SL	0.550 + 0.073*SL
	t_F	0.229	0.191 + 0.019*SL	0.188 + 0.020*SL	0.165 + 0.020*SL
	t_{PLH}	0.363	0.298 + 0.033*SL	0.301 + 0.032*SL	0.309 + 0.032*SL
	t_{PHL}	0.188	0.166 + 0.011*SL	0.167 + 0.011*SL	0.172 + 0.011*SL
E to Y	t_R	0.715	0.576 + 0.070*SL	0.566 + 0.072*SL	0.550 + 0.073*SL
	t_F	0.266	0.228 + 0.019*SL	0.225 + 0.020*SL	0.200 + 0.020*SL
	t_{PLH}	0.407	0.341 + 0.033*SL	0.345 + 0.032*SL	0.354 + 0.032*SL
	t_{PHL}	0.203	0.180 + 0.011*SL	0.183 + 0.011*SL	0.193 + 0.011*SL
F to Y	t_R	0.714	0.573 + 0.070*SL	0.564 + 0.072*SL	0.550 + 0.073*SL
	t_F	0.295	0.256 + 0.020*SL	0.256 + 0.020*SL	0.239 + 0.020*SL
	t_{PLH}	0.427	0.361 + 0.033*SL	0.365 + 0.032*SL	0.374 + 0.032*SL
	t_{PHL}	0.211	0.187 + 0.012*SL	0.192 + 0.011*SL	0.212 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO32/AO32D2/AO32D4

3-AND and 2-AND into 2-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	1	x	x	0
x	x	x	1	1	0
Other States					1

Cell Data

Input Load (SL)														
AO32					*AO32D2*					*AO32D4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
1.0	1.0	1.0	1.1	1.1	1.0	1.0	1.1	1.1	1.1	1.0	1.1	1.1	1.1	1.1

Gate Count		
AO32	*AO32D2*	*AO32D4*
2.00	3.00	3.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO32

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.379	0.236 + 0.071*SL	0.222 + 0.075*SL	0.216 + 0.075*SL
	t_F	0.307	0.195 + 0.056*SL	0.179 + 0.060*SL	0.160 + 0.061*SL
	t_{PLH}	0.207	0.142 + 0.032*SL	0.140 + 0.033*SL	0.139 + 0.033*SL
	t_{PHL}	0.166	0.110 + 0.028*SL	0.112 + 0.028*SL	0.112 + 0.028*SL
B to Y	t_R	0.407	0.265 + 0.071*SL	0.249 + 0.075*SL	0.243 + 0.075*SL
	t_F	0.303	0.190 + 0.057*SL	0.176 + 0.060*SL	0.160 + 0.061*SL
	t_{PLH}	0.225	0.160 + 0.032*SL	0.158 + 0.033*SL	0.156 + 0.033*SL
	t_{PHL}	0.162	0.106 + 0.028*SL	0.108 + 0.028*SL	0.109 + 0.028*SL
C to Y	t_R	0.439	0.298 + 0.071*SL	0.281 + 0.075*SL	0.273 + 0.075*SL
	t_F	0.297	0.181 + 0.058*SL	0.172 + 0.060*SL	0.160 + 0.061*SL
	t_{PLH}	0.242	0.177 + 0.033*SL	0.175 + 0.033*SL	0.174 + 0.033*SL
	t_{PHL}	0.157	0.100 + 0.028*SL	0.103 + 0.028*SL	0.104 + 0.028*SL
D to Y	t_R	0.407	0.262 + 0.072*SL	0.252 + 0.075*SL	0.242 + 0.075*SL
	t_F	0.283	0.211 + 0.036*SL	0.198 + 0.039*SL	0.172 + 0.040*SL
	t_{PLH}	0.269	0.202 + 0.034*SL	0.204 + 0.033*SL	0.210 + 0.033*SL
	t_{PHL}	0.192	0.152 + 0.020*SL	0.155 + 0.019*SL	0.159 + 0.019*SL
E to Y	t_R	0.436	0.291 + 0.073*SL	0.282 + 0.075*SL	0.273 + 0.075*SL
	t_F	0.277	0.202 + 0.037*SL	0.193 + 0.039*SL	0.172 + 0.040*SL
	t_{PLH}	0.290	0.223 + 0.034*SL	0.225 + 0.033*SL	0.227 + 0.033*SL
	t_{PHL}	0.179	0.139 + 0.020*SL	0.142 + 0.019*SL	0.146 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO32D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.097	0.062 + 0.017*SL	0.054 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.082	0.050 + 0.016*SL	0.048 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.330	0.309 + 0.010*SL	0.315 + 0.009*SL	0.317 + 0.009*SL
	t_{PHL}	0.301	0.278 + 0.011*SL	0.287 + 0.009*SL	0.294 + 0.009*SL
B to Y	t_R	0.098	0.064 + 0.017*SL	0.054 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.083	0.052 + 0.016*SL	0.048 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.351	0.330 + 0.010*SL	0.337 + 0.009*SL	0.339 + 0.009*SL
	t_{PHL}	0.297	0.275 + 0.011*SL	0.284 + 0.009*SL	0.290 + 0.009*SL
C to Y	t_R	0.099	0.065 + 0.017*SL	0.056 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.083	0.051 + 0.016*SL	0.048 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.372	0.351 + 0.010*SL	0.357 + 0.009*SL	0.359 + 0.009*SL
	t_{PHL}	0.292	0.269 + 0.011*SL	0.278 + 0.009*SL	0.285 + 0.009*SL
D to Y	t_R	0.098	0.063 + 0.017*SL	0.055 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.081	0.049 + 0.016*SL	0.046 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.395	0.374 + 0.010*SL	0.381 + 0.009*SL	0.383 + 0.009*SL
	t_{PHL}	0.328	0.305 + 0.011*SL	0.314 + 0.009*SL	0.320 + 0.009*SL
E to Y	t_R	0.098	0.063 + 0.017*SL	0.056 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.081	0.048 + 0.016*SL	0.046 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.419	0.398 + 0.010*SL	0.404 + 0.009*SL	0.406 + 0.009*SL
	t_{PHL}	0.313	0.291 + 0.011*SL	0.300 + 0.009*SL	0.306 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO32D4

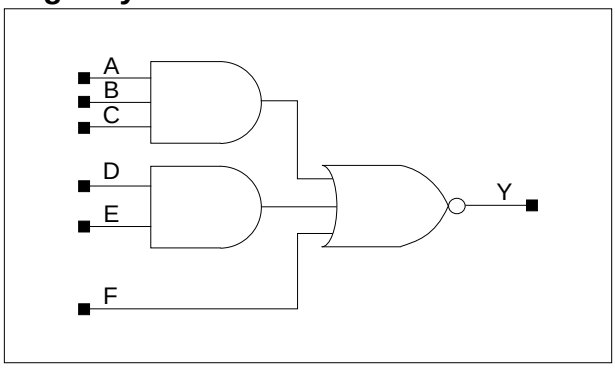
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.096	0.080 + 0.008*SL	0.076 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.083	0.066 + 0.008*SL	0.068 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.369	0.356 + 0.006*SL	0.363 + 0.005*SL	0.373 + 0.004*SL
	t_{PHL}	0.338	0.324 + 0.007*SL	0.333 + 0.005*SL	0.350 + 0.004*SL
B to Y	t_R	0.096	0.079 + 0.009*SL	0.077 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.084	0.067 + 0.008*SL	0.068 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.391	0.378 + 0.006*SL	0.385 + 0.005*SL	0.395 + 0.004*SL
	t_{PHL}	0.334	0.320 + 0.007*SL	0.329 + 0.005*SL	0.346 + 0.004*SL
C to Y	t_R	0.098	0.081 + 0.008*SL	0.078 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.084	0.067 + 0.008*SL	0.068 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.412	0.400 + 0.006*SL	0.407 + 0.005*SL	0.417 + 0.004*SL
	t_{PHL}	0.329	0.315 + 0.007*SL	0.324 + 0.005*SL	0.341 + 0.004*SL
D to Y	t_R	0.097	0.080 + 0.008*SL	0.076 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.080	0.064 + 0.008*SL	0.064 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.435	0.423 + 0.006*SL	0.430 + 0.005*SL	0.440 + 0.004*SL
	t_{PHL}	0.361	0.348 + 0.007*SL	0.356 + 0.005*SL	0.373 + 0.004*SL
E to Y	t_R	0.098	0.082 + 0.008*SL	0.078 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.080	0.064 + 0.008*SL	0.064 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.460	0.447 + 0.006*SL	0.454 + 0.005*SL	0.464 + 0.004*SL
	t_{PHL}	0.347	0.334 + 0.007*SL	0.342 + 0.005*SL	0.359 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO321/AO321D2/AO321D4

3-AND and 2-AND into 3-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	x	0
x	x	x	x	x	1	0
Other States						1

Cell Data

Input Load (SL)																	
AO321						*AO321D2*						*AO321D4*					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
0.9	1.0	1.0	0.9	0.9	0.9	1.0	1.0	1.0	0.9	0.9	0.9	1.0	1.0	1.0	0.9	0.9	0.9

Gate Count		
AO321	*AO321D2*	*AO321D4*
2.67	3.33	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO321

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.582	0.362 + 0.110*SL	0.352 + 0.112*SL	0.371 + 0.112*SL
	t_F	0.348	0.208 + 0.070*SL	0.193 + 0.074*SL	0.182 + 0.074*SL
	t_{PLH}	0.239	0.145 + 0.047*SL	0.138 + 0.049*SL	0.138 + 0.049*SL
	t_{PHL}	0.196	0.129 + 0.034*SL	0.129 + 0.034*SL	0.129 + 0.034*SL
B to Y	t_R	0.620	0.401 + 0.110*SL	0.389 + 0.112*SL	0.408 + 0.112*SL
	t_F	0.345	0.203 + 0.071*SL	0.192 + 0.074*SL	0.181 + 0.074*SL
	t_{PLH}	0.263	0.168 + 0.048*SL	0.163 + 0.049*SL	0.161 + 0.049*SL
	t_{PHL}	0.195	0.126 + 0.034*SL	0.127 + 0.034*SL	0.129 + 0.034*SL
C to Y	t_R	0.659	0.441 + 0.109*SL	0.427 + 0.112*SL	0.445 + 0.112*SL
	t_F	0.341	0.198 + 0.072*SL	0.189 + 0.074*SL	0.181 + 0.074*SL
	t_{PLH}	0.284	0.188 + 0.048*SL	0.185 + 0.049*SL	0.184 + 0.049*SL
	t_{PHL}	0.189	0.120 + 0.034*SL	0.122 + 0.034*SL	0.124 + 0.034*SL
D to Y	t_R	0.649	0.435 + 0.107*SL	0.422 + 0.110*SL	0.412 + 0.111*SL
	t_F	0.419	0.295 + 0.062*SL	0.285 + 0.064*SL	0.275 + 0.064*SL
	t_{PLH}	0.372	0.272 + 0.050*SL	0.277 + 0.049*SL	0.284 + 0.049*SL
	t_{PHL}	0.300	0.236 + 0.032*SL	0.239 + 0.031*SL	0.245 + 0.031*SL
E to Y	t_R	0.683	0.465 + 0.109*SL	0.455 + 0.112*SL	0.445 + 0.112*SL
	t_F	0.417	0.293 + 0.062*SL	0.286 + 0.064*SL	0.275 + 0.064*SL
	t_{PLH}	0.394	0.293 + 0.050*SL	0.297 + 0.049*SL	0.301 + 0.049*SL
	t_{PHL}	0.287	0.223 + 0.032*SL	0.227 + 0.031*SL	0.233 + 0.031*SL
F to Y	t_R	0.683	0.465 + 0.109*SL	0.454 + 0.112*SL	0.445 + 0.112*SL
	t_F	0.350	0.276 + 0.037*SL	0.267 + 0.039*SL	0.247 + 0.040*SL
	t_{PLH}	0.426	0.325 + 0.050*SL	0.329 + 0.049*SL	0.335 + 0.049*SL
	t_{PHL}	0.228	0.182 + 0.023*SL	0.188 + 0.022*SL	0.203 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO321D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.102	0.068 + 0.017*SL	0.059 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.084	0.052 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.372	0.351 + 0.011*SL	0.359 + 0.009*SL	0.360 + 0.009*SL
	t_{PHL}	0.337	0.315 + 0.011*SL	0.324 + 0.009*SL	0.331 + 0.009*SL
B to Y	t_R	0.103	0.070 + 0.017*SL	0.060 + 0.019*SL	0.034 + 0.019*SL
	t_F	0.083	0.050 + 0.016*SL	0.049 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.399	0.378 + 0.011*SL	0.385 + 0.009*SL	0.387 + 0.009*SL
	t_{PHL}	0.335	0.312 + 0.011*SL	0.322 + 0.009*SL	0.328 + 0.009*SL
C to Y	t_R	0.105	0.071 + 0.017*SL	0.062 + 0.019*SL	0.034 + 0.019*SL
	t_F	0.083	0.051 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.422	0.400 + 0.011*SL	0.408 + 0.009*SL	0.410 + 0.009*SL
	t_{PHL}	0.328	0.306 + 0.011*SL	0.315 + 0.009*SL	0.321 + 0.009*SL
D to Y	t_R	0.104	0.070 + 0.017*SL	0.061 + 0.019*SL	0.034 + 0.019*SL
	t_F	0.083	0.050 + 0.016*SL	0.049 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.504	0.482 + 0.011*SL	0.490 + 0.009*SL	0.492 + 0.009*SL
	t_{PHL}	0.454	0.431 + 0.011*SL	0.440 + 0.009*SL	0.446 + 0.009*SL
E to Y	t_R	0.105	0.071 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.084	0.052 + 0.016*SL	0.050 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.528	0.507 + 0.011*SL	0.514 + 0.009*SL	0.516 + 0.009*SL
	t_{PHL}	0.441	0.418 + 0.011*SL	0.428 + 0.009*SL	0.434 + 0.009*SL
F to Y	t_R	0.105	0.072 + 0.017*SL	0.063 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.082	0.051 + 0.016*SL	0.047 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.559	0.538 + 0.011*SL	0.546 + 0.009*SL	0.547 + 0.009*SL
	t_{PHL}	0.377	0.355 + 0.011*SL	0.364 + 0.009*SL	0.370 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO321D4

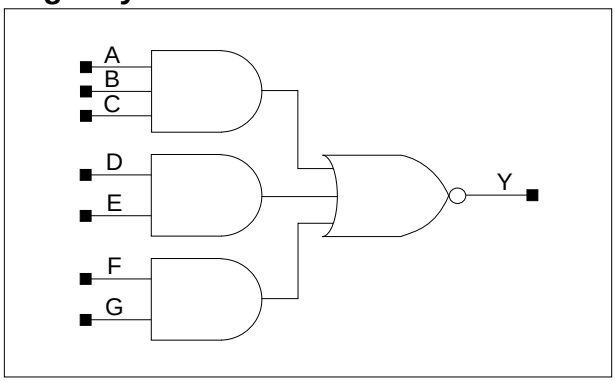
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.086 + 0.008*SL	0.082 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.085	0.069 + 0.008*SL	0.070 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.414	0.401 + 0.006*SL	0.409 + 0.005*SL	0.420 + 0.004*SL
	t_{PHL}	0.377	0.363 + 0.007*SL	0.372 + 0.005*SL	0.389 + 0.004*SL
B to Y	t_R	0.104	0.088 + 0.008*SL	0.084 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.085	0.068 + 0.008*SL	0.070 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.443	0.430 + 0.006*SL	0.438 + 0.005*SL	0.448 + 0.004*SL
	t_{PHL}	0.375	0.361 + 0.007*SL	0.370 + 0.005*SL	0.388 + 0.004*SL
C to Y	t_R	0.106	0.090 + 0.008*SL	0.086 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.085	0.069 + 0.008*SL	0.070 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.468	0.455 + 0.007*SL	0.463 + 0.005*SL	0.474 + 0.004*SL
	t_{PHL}	0.369	0.355 + 0.007*SL	0.364 + 0.005*SL	0.382 + 0.004*SL
D to Y	t_R	0.106	0.090 + 0.008*SL	0.085 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.085	0.068 + 0.008*SL	0.069 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.551	0.538 + 0.007*SL	0.546 + 0.005*SL	0.557 + 0.004*SL
	t_{PHL}	0.493	0.480 + 0.007*SL	0.488 + 0.005*SL	0.505 + 0.004*SL
E to Y	t_R	0.106	0.089 + 0.008*SL	0.086 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.084	0.067 + 0.009*SL	0.069 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.576	0.563 + 0.007*SL	0.571 + 0.005*SL	0.582 + 0.004*SL
	t_{PHL}	0.480	0.467 + 0.007*SL	0.475 + 0.005*SL	0.492 + 0.004*SL
F to Y	t_R	0.106	0.090 + 0.008*SL	0.086 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.083	0.066 + 0.008*SL	0.067 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.607	0.594 + 0.007*SL	0.602 + 0.005*SL	0.613 + 0.004*SL
	t_{PHL}	0.414	0.401 + 0.007*SL	0.409 + 0.005*SL	0.427 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO322/AO322D2/AO322D4

3-AND and Two 2-ANDs into 3-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
1	1	1	x	x	x	x	0
x	x	x	1	1	x	x	0
x	x	x	x	x	1	1	0
Other States							1

Cell Data

Input Load (SL)							Gate Count
AO322							*AO322*
A	B	C	D	E	F	G	
1.0	1.0	1.0	0.9	0.9	0.9	0.9	3.00
AO322D2							*AO322D2*
A	B	C	D	E	F	G	
1.0	1.0	1.0	0.9	0.9	0.9	0.9	3.67
AO322D4							*AO322D4*
A	B	C	D	E	F	G	
1.0	1.0	1.0	0.9	0.9	0.9	0.9	4.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO322

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.613	0.392 + 0.111*SL	0.384 + 0.113*SL	0.406 + 0.112*SL
	t_F	0.352	0.224 + 0.064*SL	0.209 + 0.068*SL	0.195 + 0.068*SL
	t_{PLH}	0.259	0.164 + 0.048*SL	0.158 + 0.049*SL	0.158 + 0.049*SL
	t_{PHL}	0.190	0.128 + 0.031*SL	0.128 + 0.031*SL	0.128 + 0.031*SL
B to Y	t_R	0.654	0.433 + 0.110*SL	0.425 + 0.113*SL	0.448 + 0.112*SL
	t_F	0.349	0.220 + 0.065*SL	0.207 + 0.068*SL	0.195 + 0.068*SL
	t_{PLH}	0.285	0.189 + 0.048*SL	0.185 + 0.049*SL	0.185 + 0.049*SL
	t_{PHL}	0.188	0.125 + 0.031*SL	0.126 + 0.031*SL	0.128 + 0.031*SL
C to Y	t_R	0.697	0.478 + 0.110*SL	0.467 + 0.113*SL	0.488 + 0.112*SL
	t_F	0.344	0.213 + 0.066*SL	0.204 + 0.068*SL	0.195 + 0.068*SL
	t_{PLH}	0.309	0.212 + 0.048*SL	0.210 + 0.049*SL	0.209 + 0.049*SL
	t_{PHL}	0.183	0.119 + 0.032*SL	0.121 + 0.031*SL	0.123 + 0.031*SL
D to Y	t_R	0.698	0.480 + 0.109*SL	0.470 + 0.112*SL	0.461 + 0.112*SL
	t_F	0.460	0.338 + 0.061*SL	0.326 + 0.064*SL	0.313 + 0.064*SL
	t_{PLH}	0.401	0.300 + 0.050*SL	0.304 + 0.049*SL	0.311 + 0.049*SL
	t_{PHL}	0.294	0.230 + 0.032*SL	0.233 + 0.031*SL	0.239 + 0.031*SL
E to Y	t_R	0.724	0.505 + 0.110*SL	0.497 + 0.112*SL	0.488 + 0.112*SL
	t_F	0.459	0.336 + 0.062*SL	0.326 + 0.064*SL	0.313 + 0.064*SL
	t_{PLH}	0.419	0.319 + 0.050*SL	0.322 + 0.049*SL	0.327 + 0.049*SL
	t_{PHL}	0.281	0.217 + 0.032*SL	0.221 + 0.031*SL	0.227 + 0.031*SL
F to Y	t_R	0.698	0.480 + 0.109*SL	0.470 + 0.112*SL	0.460 + 0.112*SL
	t_F	0.568	0.445 + 0.061*SL	0.436 + 0.064*SL	0.418 + 0.064*SL
	t_{PLH}	0.451	0.350 + 0.050*SL	0.355 + 0.049*SL	0.362 + 0.049*SL
	t_{PHL}	0.342	0.274 + 0.034*SL	0.283 + 0.032*SL	0.303 + 0.031*SL
G to Y	t_R	0.725	0.506 + 0.109*SL	0.497 + 0.112*SL	0.488 + 0.112*SL
	t_F	0.567	0.442 + 0.062*SL	0.437 + 0.064*SL	0.418 + 0.064*SL
	t_{PLH}	0.470	0.369 + 0.050*SL	0.373 + 0.049*SL	0.378 + 0.049*SL
	t_{PHL}	0.329	0.261 + 0.034*SL	0.270 + 0.032*SL	0.290 + 0.031*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO322D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.069 + 0.017*SL	0.060 + 0.019*SL	0.034 + 0.019*SL
	t_F	0.084	0.053 + 0.015*SL	0.048 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.399	0.378 + 0.011*SL	0.386 + 0.009*SL	0.387 + 0.009*SL
	t_{PHL}	0.337	0.315 + 0.011*SL	0.324 + 0.009*SL	0.331 + 0.009*SL
B to Y	t_R	0.105	0.071 + 0.017*SL	0.062 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.083	0.050 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.426	0.405 + 0.011*SL	0.412 + 0.009*SL	0.414 + 0.009*SL
	t_{PHL}	0.333	0.311 + 0.011*SL	0.320 + 0.009*SL	0.327 + 0.009*SL
C to Y	t_R	0.106	0.072 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.084	0.052 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.450	0.428 + 0.011*SL	0.436 + 0.009*SL	0.438 + 0.009*SL
	t_{PHL}	0.327	0.305 + 0.011*SL	0.314 + 0.009*SL	0.321 + 0.009*SL
D to Y	t_R	0.106	0.072 + 0.017*SL	0.063 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.086	0.055 + 0.016*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.538	0.517 + 0.011*SL	0.524 + 0.009*SL	0.526 + 0.009*SL
	t_{PHL}	0.456	0.433 + 0.011*SL	0.442 + 0.009*SL	0.449 + 0.009*SL
E to Y	t_R	0.107	0.073 + 0.017*SL	0.065 + 0.019*SL	0.034 + 0.019*SL
	t_F	0.085	0.053 + 0.016*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.556	0.535 + 0.011*SL	0.542 + 0.009*SL	0.544 + 0.009*SL
	t_{PHL}	0.443	0.420 + 0.011*SL	0.430 + 0.009*SL	0.436 + 0.009*SL
F to Y	t_R	0.106	0.072 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.088	0.056 + 0.016*SL	0.053 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.571	0.550 + 0.011*SL	0.557 + 0.009*SL	0.559 + 0.009*SL
	t_{PHL}	0.506	0.483 + 0.011*SL	0.493 + 0.009*SL	0.500 + 0.009*SL
G to Y	t_R	0.107	0.073 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.087	0.054 + 0.016*SL	0.054 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.592	0.571 + 0.011*SL	0.579 + 0.009*SL	0.580 + 0.009*SL
	t_{PHL}	0.494	0.471 + 0.011*SL	0.481 + 0.009*SL	0.487 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO322D4

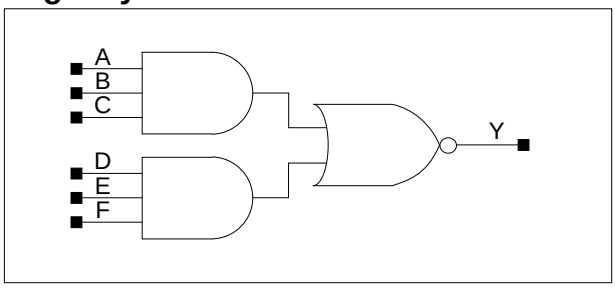
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.105	0.088 + 0.008*SL	0.085 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.086	0.070 + 0.008*SL	0.071 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.445	0.432 + 0.006*SL	0.440 + 0.005*SL	0.451 + 0.004*SL
	t_{PHL}	0.380	0.366 + 0.007*SL	0.375 + 0.005*SL	0.392 + 0.004*SL
B to Y	t_R	0.106	0.090 + 0.008*SL	0.085 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.086	0.069 + 0.008*SL	0.071 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.473	0.460 + 0.006*SL	0.468 + 0.005*SL	0.478 + 0.004*SL
	t_{PHL}	0.376	0.362 + 0.007*SL	0.371 + 0.005*SL	0.389 + 0.004*SL
C to Y	t_R	0.107	0.090 + 0.008*SL	0.087 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.086	0.070 + 0.008*SL	0.070 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.497	0.484 + 0.007*SL	0.492 + 0.005*SL	0.503 + 0.004*SL
	t_{PHL}	0.370	0.356 + 0.007*SL	0.364 + 0.005*SL	0.382 + 0.004*SL
D to Y	t_R	0.107	0.091 + 0.008*SL	0.087 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.087	0.070 + 0.008*SL	0.072 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.586	0.573 + 0.007*SL	0.581 + 0.005*SL	0.591 + 0.004*SL
	t_{PHL}	0.499	0.485 + 0.007*SL	0.494 + 0.005*SL	0.512 + 0.004*SL
E to Y	t_R	0.108	0.091 + 0.008*SL	0.088 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.088	0.071 + 0.008*SL	0.073 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.605	0.592 + 0.007*SL	0.600 + 0.005*SL	0.611 + 0.004*SL
	t_{PHL}	0.486	0.472 + 0.007*SL	0.481 + 0.005*SL	0.499 + 0.004*SL
F to Y	t_R	0.107	0.090 + 0.008*SL	0.086 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.090	0.074 + 0.008*SL	0.074 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.619	0.606 + 0.007*SL	0.614 + 0.005*SL	0.624 + 0.004*SL
	t_{PHL}	0.552	0.538 + 0.007*SL	0.547 + 0.005*SL	0.565 + 0.004*SL
G to Y	t_R	0.107	0.090 + 0.008*SL	0.087 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.090	0.074 + 0.008*SL	0.075 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.641	0.628 + 0.007*SL	0.636 + 0.005*SL	0.646 + 0.004*SL
	t_{PHL}	0.539	0.525 + 0.007*SL	0.534 + 0.005*SL	0.552 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO33/AO33D2/AO33D4

Two 3-ANDs into 2-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	1	0
Other States						1

Cell Data

Input Load (SL)																	
AO33						*AO33D2*						*AO33D4*					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
1.0	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1

Gate Count		
AO33	*AO33D2*	*AO33D4*
2.33	3.33	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO33

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.411	0.268 + 0.072*SL	0.255 + 0.075*SL	0.249 + 0.075*SL
	t_F	0.328	0.224 + 0.052*SL	0.208 + 0.056*SL	0.185 + 0.057*SL
	t_{PLH}	0.228	0.162 + 0.033*SL	0.162 + 0.033*SL	0.162 + 0.033*SL
	t_{PHL}	0.160	0.106 + 0.027*SL	0.111 + 0.026*SL	0.115 + 0.026*SL
B to Y	t_R	0.440	0.296 + 0.072*SL	0.284 + 0.075*SL	0.279 + 0.075*SL
	t_F	0.323	0.219 + 0.052*SL	0.203 + 0.056*SL	0.185 + 0.057*SL
	t_{PLH}	0.248	0.182 + 0.033*SL	0.181 + 0.033*SL	0.181 + 0.033*SL
	t_{PHL}	0.157	0.102 + 0.027*SL	0.108 + 0.026*SL	0.112 + 0.026*SL
C to Y	t_R	0.475	0.332 + 0.071*SL	0.318 + 0.075*SL	0.311 + 0.075*SL
	t_F	0.316	0.209 + 0.054*SL	0.199 + 0.056*SL	0.185 + 0.057*SL
	t_{PLH}	0.267	0.201 + 0.033*SL	0.201 + 0.033*SL	0.200 + 0.033*SL
	t_{PHL}	0.151	0.096 + 0.027*SL	0.103 + 0.026*SL	0.107 + 0.026*SL
D to Y	t_R	0.413	0.269 + 0.072*SL	0.259 + 0.075*SL	0.249 + 0.075*SL
	t_F	0.384	0.279 + 0.052*SL	0.266 + 0.056*SL	0.249 + 0.056*SL
	t_{PLH}	0.277	0.209 + 0.034*SL	0.213 + 0.033*SL	0.218 + 0.033*SL
	t_{PHL}	0.248	0.195 + 0.026*SL	0.198 + 0.026*SL	0.202 + 0.026*SL
E to Y	t_R	0.442	0.297 + 0.073*SL	0.288 + 0.075*SL	0.278 + 0.075*SL
	t_F	0.381	0.275 + 0.053*SL	0.265 + 0.056*SL	0.249 + 0.056*SL
	t_{PLH}	0.298	0.230 + 0.034*SL	0.232 + 0.033*SL	0.236 + 0.033*SL
	t_{PHL}	0.244	0.191 + 0.027*SL	0.194 + 0.026*SL	0.199 + 0.026*SL
F to Y	t_R	0.475	0.330 + 0.073*SL	0.321 + 0.075*SL	0.311 + 0.075*SL
	t_F	0.379	0.271 + 0.054*SL	0.263 + 0.056*SL	0.249 + 0.056*SL
	t_{PLH}	0.318	0.250 + 0.034*SL	0.253 + 0.033*SL	0.256 + 0.033*SL
	t_{PHL}	0.238	0.184 + 0.027*SL	0.188 + 0.026*SL	0.194 + 0.026*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO33D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.098	0.063 + 0.017*SL	0.055 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.084	0.051 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.354	0.333 + 0.010*SL	0.340 + 0.009*SL	0.342 + 0.009*SL
	t_{PHL}	0.307	0.285 + 0.011*SL	0.294 + 0.009*SL	0.301 + 0.009*SL
B to Y	t_R	0.099	0.065 + 0.017*SL	0.056 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.084	0.053 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.377	0.356 + 0.010*SL	0.363 + 0.009*SL	0.365 + 0.009*SL
	t_{PHL}	0.304	0.281 + 0.011*SL	0.291 + 0.009*SL	0.297 + 0.009*SL
C to Y	t_R	0.100	0.065 + 0.017*SL	0.057 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.084	0.053 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.400	0.379 + 0.010*SL	0.385 + 0.009*SL	0.387 + 0.009*SL
	t_{PHL}	0.298	0.276 + 0.011*SL	0.285 + 0.009*SL	0.292 + 0.009*SL
D to Y	t_R	0.098	0.063 + 0.017*SL	0.055 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.084	0.053 + 0.015*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.403	0.382 + 0.010*SL	0.389 + 0.009*SL	0.390 + 0.009*SL
	t_{PHL}	0.400	0.377 + 0.011*SL	0.387 + 0.009*SL	0.393 + 0.009*SL
E to Y	t_R	0.099	0.065 + 0.017*SL	0.056 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.083	0.050 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.426	0.406 + 0.010*SL	0.412 + 0.009*SL	0.414 + 0.009*SL
	t_{PHL}	0.395	0.373 + 0.011*SL	0.382 + 0.009*SL	0.389 + 0.009*SL
F to Y	t_R	0.100	0.066 + 0.017*SL	0.057 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.084	0.053 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.450	0.429 + 0.010*SL	0.435 + 0.009*SL	0.437 + 0.009*SL
	t_{PHL}	0.389	0.367 + 0.011*SL	0.376 + 0.009*SL	0.383 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO33D4

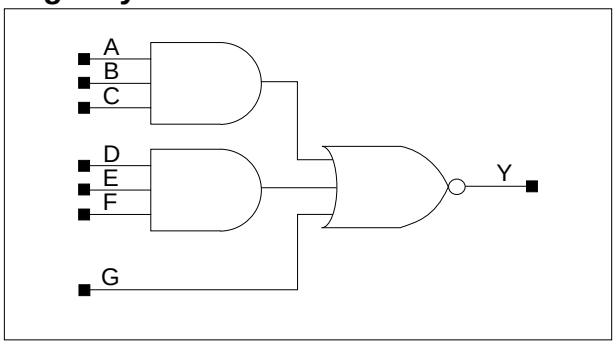
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.097	0.080 + 0.009*SL	0.077 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.085	0.069 + 0.008*SL	0.069 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.394	0.381 + 0.006*SL	0.388 + 0.004*SL	0.397 + 0.004*SL
	t_{PHL}	0.345	0.332 + 0.007*SL	0.340 + 0.005*SL	0.358 + 0.004*SL
B to Y	t_R	0.098	0.081 + 0.008*SL	0.077 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.085	0.068 + 0.008*SL	0.070 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.417	0.405 + 0.006*SL	0.412 + 0.005*SL	0.421 + 0.004*SL
	t_{PHL}	0.342	0.328 + 0.007*SL	0.337 + 0.005*SL	0.355 + 0.004*SL
C to Y	t_R	0.099	0.083 + 0.008*SL	0.079 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.085	0.068 + 0.008*SL	0.070 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.440	0.428 + 0.006*SL	0.435 + 0.005*SL	0.445 + 0.004*SL
	t_{PHL}	0.337	0.323 + 0.007*SL	0.332 + 0.005*SL	0.349 + 0.004*SL
D to Y	t_R	0.097	0.080 + 0.009*SL	0.077 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.084	0.068 + 0.008*SL	0.069 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.442	0.430 + 0.006*SL	0.437 + 0.005*SL	0.446 + 0.004*SL
	t_{PHL}	0.436	0.423 + 0.007*SL	0.432 + 0.005*SL	0.449 + 0.004*SL
E to Y	t_R	0.098	0.081 + 0.008*SL	0.078 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.084	0.067 + 0.008*SL	0.069 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.466	0.454 + 0.006*SL	0.461 + 0.005*SL	0.471 + 0.004*SL
	t_{PHL}	0.432	0.419 + 0.007*SL	0.427 + 0.005*SL	0.445 + 0.004*SL
F to Y	t_R	0.099	0.082 + 0.008*SL	0.079 + 0.009*SL	0.049 + 0.010*SL
	t_F	0.084	0.068 + 0.008*SL	0.068 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.491	0.478 + 0.006*SL	0.485 + 0.005*SL	0.495 + 0.004*SL
	t_{PHL}	0.426	0.412 + 0.007*SL	0.421 + 0.005*SL	0.438 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO331/AO331D2/AO331D4

Two 3-ANDs into 3-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
1	1	1	x	x	x	x	0
x	x	x	1	1	1	x	0
x	x	x	x	x	x	1	0
Other States							1

Cell Data

Input Load (SL)							Gate Count
AO331							*AO331*
A	B	C	D	E	F	G	
1.0	1.0	1.0	1.0	1.0	1.0	0.9	2.67
AO331D2							*AO331D2*
A	B	C	D	E	F	G	
1.0	1.0	1.0	1.0	1.0	1.0	0.9	3.67
AO331D4							*AO331D4*
A	B	C	D	E	F	G	
1.0	1.0	1.0	1.0	1.0	1.0	0.9	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO331

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.649	0.428 + 0.110*SL	0.420 + 0.113*SL	0.443 + 0.112*SL
	t_F	0.379	0.249 + 0.065*SL	0.234 + 0.069*SL	0.220 + 0.069*SL
	t_{PLH}	0.273	0.176 + 0.048*SL	0.173 + 0.049*SL	0.174 + 0.049*SL
	t_{PHL}	0.197	0.132 + 0.033*SL	0.135 + 0.032*SL	0.138 + 0.032*SL
B to Y	t_R	0.683	0.462 + 0.110*SL	0.454 + 0.113*SL	0.477 + 0.112*SL
	t_F	0.376	0.245 + 0.066*SL	0.232 + 0.069*SL	0.220 + 0.069*SL
	t_{PLH}	0.294	0.197 + 0.048*SL	0.195 + 0.049*SL	0.195 + 0.049*SL
	t_{PHL}	0.192	0.127 + 0.033*SL	0.130 + 0.032*SL	0.134 + 0.032*SL
C to Y	t_R	0.713	0.495 + 0.109*SL	0.485 + 0.112*SL	0.508 + 0.111*SL
	t_F	0.373	0.240 + 0.066*SL	0.230 + 0.069*SL	0.220 + 0.069*SL
	t_{PLH}	0.312	0.215 + 0.048*SL	0.213 + 0.049*SL	0.213 + 0.049*SL
	t_{PHL}	0.184	0.118 + 0.033*SL	0.122 + 0.032*SL	0.126 + 0.032*SL
D to Y	t_R	0.669	0.454 + 0.108*SL	0.443 + 0.110*SL	0.433 + 0.111*SL
	t_F	0.476	0.343 + 0.066*SL	0.333 + 0.069*SL	0.323 + 0.069*SL
	t_{PLH}	0.387	0.287 + 0.050*SL	0.292 + 0.049*SL	0.300 + 0.049*SL
	t_{PHL}	0.315	0.250 + 0.033*SL	0.253 + 0.032*SL	0.260 + 0.032*SL
E to Y	t_R	0.713	0.495 + 0.109*SL	0.485 + 0.112*SL	0.476 + 0.112*SL
	t_F	0.476	0.342 + 0.067*SL	0.335 + 0.069*SL	0.324 + 0.069*SL
	t_{PLH}	0.417	0.316 + 0.050*SL	0.320 + 0.049*SL	0.326 + 0.049*SL
	t_{PHL}	0.313	0.247 + 0.033*SL	0.251 + 0.032*SL	0.258 + 0.032*SL
F to Y	t_R	0.744	0.528 + 0.108*SL	0.518 + 0.111*SL	0.508 + 0.111*SL
	t_F	0.475	0.340 + 0.067*SL	0.333 + 0.069*SL	0.324 + 0.069*SL
	t_{PLH}	0.437	0.338 + 0.050*SL	0.341 + 0.049*SL	0.347 + 0.049*SL
	t_{PHL}	0.306	0.241 + 0.033*SL	0.244 + 0.032*SL	0.251 + 0.032*SL
G to Y	t_R	0.745	0.528 + 0.108*SL	0.519 + 0.111*SL	0.508 + 0.111*SL
	t_F	0.369	0.295 + 0.037*SL	0.287 + 0.039*SL	0.268 + 0.040*SL
	t_{PLH}	0.473	0.374 + 0.050*SL	0.377 + 0.049*SL	0.384 + 0.049*SL
	t_{PHL}	0.237	0.189 + 0.024*SL	0.197 + 0.022*SL	0.214 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO331D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.104	0.070 + 0.017*SL	0.062 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.086	0.055 + 0.015*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.402	0.381 + 0.011*SL	0.388 + 0.009*SL	0.390 + 0.009*SL
	t_{PHL}	0.344	0.321 + 0.011*SL	0.331 + 0.009*SL	0.338 + 0.009*SL
B to Y	t_R	0.106	0.072 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.084	0.051 + 0.017*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.426	0.405 + 0.011*SL	0.412 + 0.009*SL	0.414 + 0.009*SL
	t_{PHL}	0.339	0.316 + 0.011*SL	0.326 + 0.009*SL	0.333 + 0.009*SL
C to Y	t_R	0.107	0.074 + 0.017*SL	0.065 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.086	0.054 + 0.016*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.446	0.425 + 0.011*SL	0.432 + 0.009*SL	0.434 + 0.009*SL
	t_{PHL}	0.331	0.308 + 0.011*SL	0.318 + 0.009*SL	0.325 + 0.009*SL
D to Y	t_R	0.105	0.071 + 0.017*SL	0.062 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.087	0.055 + 0.016*SL	0.052 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.514	0.492 + 0.011*SL	0.500 + 0.009*SL	0.502 + 0.009*SL
	t_{PHL}	0.476	0.453 + 0.011*SL	0.463 + 0.009*SL	0.469 + 0.009*SL
E to Y	t_R	0.107	0.073 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.086	0.056 + 0.015*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.547	0.525 + 0.011*SL	0.533 + 0.009*SL	0.534 + 0.009*SL
	t_{PHL}	0.473	0.451 + 0.011*SL	0.460 + 0.009*SL	0.467 + 0.009*SL
F to Y	t_R	0.108	0.074 + 0.017*SL	0.066 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.085	0.053 + 0.016*SL	0.052 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.570	0.548 + 0.011*SL	0.556 + 0.009*SL	0.558 + 0.009*SL
	t_{PHL}	0.467	0.444 + 0.011*SL	0.453 + 0.009*SL	0.460 + 0.009*SL
G to Y	t_R	0.108	0.074 + 0.017*SL	0.065 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.081	0.048 + 0.017*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.606	0.584 + 0.011*SL	0.592 + 0.009*SL	0.594 + 0.009*SL
	t_{PHL}	0.388	0.366 + 0.011*SL	0.375 + 0.009*SL	0.381 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO331D4

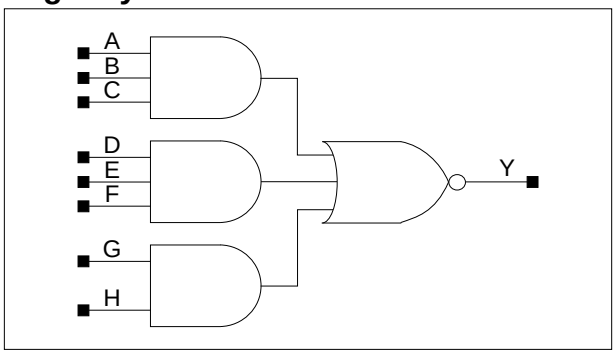
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.106	0.089 + 0.008*SL	0.085 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.088	0.071 + 0.008*SL	0.072 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.462	0.449 + 0.007*SL	0.457 + 0.005*SL	0.467 + 0.004*SL
	t_{PHL}	0.395	0.382 + 0.007*SL	0.390 + 0.005*SL	0.408 + 0.004*SL
B to Y	t_R	0.108	0.092 + 0.008*SL	0.088 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.088	0.072 + 0.008*SL	0.072 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.489	0.476 + 0.007*SL	0.484 + 0.005*SL	0.495 + 0.004*SL
	t_{PHL}	0.391	0.378 + 0.007*SL	0.387 + 0.005*SL	0.404 + 0.004*SL
C to Y	t_R	0.110	0.094 + 0.008*SL	0.089 + 0.009*SL	0.054 + 0.010*SL
	t_F	0.088	0.071 + 0.008*SL	0.073 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.512	0.498 + 0.007*SL	0.507 + 0.005*SL	0.518 + 0.004*SL
	t_{PHL}	0.385	0.371 + 0.007*SL	0.380 + 0.005*SL	0.398 + 0.004*SL
D to Y	t_R	0.106	0.090 + 0.008*SL	0.086 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.088	0.072 + 0.008*SL	0.073 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.575	0.562 + 0.007*SL	0.570 + 0.005*SL	0.581 + 0.004*SL
	t_{PHL}	0.524	0.511 + 0.007*SL	0.520 + 0.005*SL	0.537 + 0.004*SL
E to Y	t_R	0.109	0.092 + 0.008*SL	0.089 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.088	0.071 + 0.008*SL	0.072 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.608	0.595 + 0.007*SL	0.603 + 0.005*SL	0.614 + 0.004*SL
	t_{PHL}	0.522	0.508 + 0.007*SL	0.517 + 0.005*SL	0.534 + 0.004*SL
F to Y	t_R	0.110	0.094 + 0.008*SL	0.089 + 0.009*SL	0.054 + 0.010*SL
	t_F	0.088	0.071 + 0.008*SL	0.072 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.633	0.619 + 0.007*SL	0.628 + 0.005*SL	0.639 + 0.004*SL
	t_{PHL}	0.515	0.501 + 0.007*SL	0.510 + 0.005*SL	0.528 + 0.004*SL
G to Y	t_R	0.110	0.093 + 0.008*SL	0.090 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.083	0.066 + 0.008*SL	0.068 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.669	0.655 + 0.007*SL	0.664 + 0.005*SL	0.675 + 0.004*SL
	t_{PHL}	0.431	0.418 + 0.007*SL	0.426 + 0.005*SL	0.443 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO332/AO332D2/AO332D4

Two 3-ANDs and 2-AND into 3-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	1	x	x	x	x	x	0
x	x	x	1	1	1	x	x	0
x	x	x	x	x	x	1	1	0
Other States								1

Cell Data

Input Load (SL)								Gate Count
AO332								*AO332*
A	B	C	D	E	F	G	H	
1.0	1.0	1.0	1.0	1.0	1.0	0.9	0.9	3.00
AO332D2								*AO332D2*
A	B	C	D	E	F	G	H	
1.0	1.0	1.0	1.0	1.0	1.0	0.9	0.9	4.00
AO332D4								*AO332D4*
A	B	C	D	E	F	G	H	
1.0	1.0	1.0	1.0	1.0	1.0	0.9	0.9	4.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO332

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.673	0.451 + 0.111*SL	0.444 + 0.113*SL	0.469 + 0.112*SL
	t_F	0.392	0.272 + 0.060*SL	0.257 + 0.063*SL	0.241 + 0.064*SL
	t_{PLH}	0.283	0.186 + 0.048*SL	0.183 + 0.049*SL	0.185 + 0.049*SL
	t_{PHL}	0.195	0.135 + 0.030*SL	0.138 + 0.029*SL	0.141 + 0.029*SL
B to Y	t_R	0.710	0.489 + 0.111*SL	0.481 + 0.113*SL	0.508 + 0.112*SL
	t_F	0.389	0.268 + 0.060*SL	0.255 + 0.064*SL	0.241 + 0.064*SL
	t_{PLH}	0.306	0.210 + 0.048*SL	0.207 + 0.049*SL	0.207 + 0.049*SL
	t_{PHL}	0.191	0.131 + 0.030*SL	0.134 + 0.029*SL	0.137 + 0.029*SL
C to Y	t_R	0.743	0.525 + 0.109*SL	0.515 + 0.112*SL	0.541 + 0.111*SL
	t_F	0.384	0.261 + 0.061*SL	0.252 + 0.064*SL	0.241 + 0.064*SL
	t_{PLH}	0.326	0.230 + 0.048*SL	0.228 + 0.049*SL	0.227 + 0.049*SL
	t_{PHL}	0.183	0.122 + 0.030*SL	0.126 + 0.029*SL	0.130 + 0.029*SL
D to Y	t_R	0.729	0.510 + 0.109*SL	0.501 + 0.112*SL	0.492 + 0.112*SL
	t_F	0.490	0.369 + 0.060*SL	0.357 + 0.064*SL	0.342 + 0.064*SL
	t_{PLH}	0.420	0.319 + 0.051*SL	0.324 + 0.049*SL	0.333 + 0.049*SL
	t_{PHL}	0.289	0.229 + 0.030*SL	0.232 + 0.029*SL	0.238 + 0.029*SL
E to Y	t_R	0.768	0.549 + 0.110*SL	0.541 + 0.112*SL	0.533 + 0.112*SL
	t_F	0.490	0.368 + 0.061*SL	0.358 + 0.063*SL	0.342 + 0.064*SL
	t_{PLH}	0.449	0.348 + 0.050*SL	0.352 + 0.049*SL	0.359 + 0.049*SL
	t_{PHL}	0.287	0.226 + 0.030*SL	0.230 + 0.029*SL	0.237 + 0.029*SL
F to Y	t_R	0.802	0.585 + 0.109*SL	0.577 + 0.111*SL	0.569 + 0.111*SL
	t_F	0.488	0.365 + 0.061*SL	0.356 + 0.064*SL	0.342 + 0.064*SL
	t_{PLH}	0.471	0.372 + 0.050*SL	0.375 + 0.049*SL	0.381 + 0.049*SL
	t_{PHL}	0.280	0.219 + 0.030*SL	0.223 + 0.029*SL	0.231 + 0.029*SL
G to Y	t_R	0.778	0.561 + 0.108*SL	0.552 + 0.111*SL	0.542 + 0.111*SL
	t_F	0.610	0.486 + 0.062*SL	0.478 + 0.064*SL	0.461 + 0.064*SL
	t_{PLH}	0.508	0.408 + 0.050*SL	0.412 + 0.049*SL	0.420 + 0.049*SL
	t_{PHL}	0.363	0.295 + 0.034*SL	0.304 + 0.032*SL	0.325 + 0.031*SL
H to Y	t_R	0.803	0.586 + 0.109*SL	0.578 + 0.111*SL	0.569 + 0.111*SL
	t_F	0.610	0.485 + 0.062*SL	0.479 + 0.064*SL	0.461 + 0.064*SL
	t_{PLH}	0.526	0.426 + 0.050*SL	0.429 + 0.049*SL	0.435 + 0.049*SL
	t_{PHL}	0.350	0.282 + 0.034*SL	0.291 + 0.032*SL	0.313 + 0.031*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO332D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.105	0.070 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.086	0.054 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.409	0.388 + 0.011*SL	0.396 + 0.009*SL	0.397 + 0.009*SL
	t_{PHL}	0.345	0.322 + 0.011*SL	0.332 + 0.009*SL	0.339 + 0.009*SL
B to Y	t_R	0.107	0.073 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.085	0.052 + 0.016*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.436	0.415 + 0.011*SL	0.422 + 0.009*SL	0.424 + 0.009*SL
	t_{PHL}	0.340	0.317 + 0.011*SL	0.327 + 0.009*SL	0.334 + 0.009*SL
C to Y	t_R	0.108	0.075 + 0.017*SL	0.066 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.086	0.055 + 0.015*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.458	0.437 + 0.011*SL	0.444 + 0.009*SL	0.446 + 0.009*SL
	t_{PHL}	0.332	0.309 + 0.011*SL	0.319 + 0.009*SL	0.326 + 0.009*SL
D to Y	t_R	0.107	0.073 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.087	0.057 + 0.015*SL	0.052 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.547	0.525 + 0.011*SL	0.533 + 0.009*SL	0.534 + 0.009*SL
	t_{PHL}	0.452	0.429 + 0.011*SL	0.439 + 0.009*SL	0.446 + 0.009*SL
E to Y	t_R	0.109	0.075 + 0.017*SL	0.066 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.086	0.054 + 0.016*SL	0.053 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.578	0.557 + 0.011*SL	0.564 + 0.009*SL	0.566 + 0.009*SL
	t_{PHL}	0.449	0.427 + 0.011*SL	0.436 + 0.009*SL	0.443 + 0.009*SL
F to Y	t_R	0.110	0.077 + 0.017*SL	0.068 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.087	0.056 + 0.016*SL	0.053 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.603	0.582 + 0.011*SL	0.590 + 0.009*SL	0.592 + 0.009*SL
	t_{PHL}	0.443	0.420 + 0.011*SL	0.430 + 0.009*SL	0.437 + 0.009*SL
G to Y	t_R	0.109	0.075 + 0.017*SL	0.066 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.090	0.059 + 0.016*SL	0.055 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.638	0.617 + 0.011*SL	0.625 + 0.009*SL	0.627 + 0.009*SL
	t_{PHL}	0.539	0.516 + 0.011*SL	0.526 + 0.009*SL	0.533 + 0.009*SL
H to Y	t_R	0.110	0.076 + 0.017*SL	0.068 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.090	0.060 + 0.015*SL	0.055 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.658	0.636 + 0.011*SL	0.644 + 0.009*SL	0.646 + 0.009*SL
	t_{PHL}	0.526	0.503 + 0.011*SL	0.513 + 0.009*SL	0.520 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO332D4

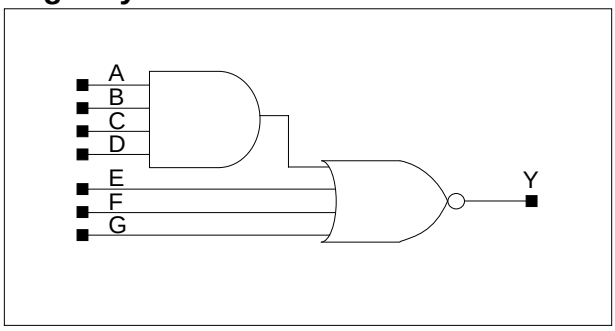
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.105	0.088 + 0.008*SL	0.085 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.088	0.072 + 0.008*SL	0.072 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.456	0.443 + 0.006*SL	0.451 + 0.005*SL	0.461 + 0.004*SL
	t_{PHL}	0.385	0.371 + 0.007*SL	0.380 + 0.005*SL	0.398 + 0.004*SL
B to Y	t_R	0.107	0.091 + 0.008*SL	0.087 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.087	0.071 + 0.008*SL	0.072 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.484	0.470 + 0.007*SL	0.479 + 0.005*SL	0.489 + 0.004*SL
	t_{PHL}	0.381	0.367 + 0.007*SL	0.376 + 0.005*SL	0.394 + 0.004*SL
C to Y	t_R	0.109	0.093 + 0.008*SL	0.090 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.087	0.071 + 0.008*SL	0.072 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.507	0.494 + 0.007*SL	0.502 + 0.005*SL	0.513 + 0.004*SL
	t_{PHL}	0.373	0.359 + 0.007*SL	0.367 + 0.005*SL	0.385 + 0.004*SL
D to Y	t_R	0.108	0.092 + 0.008*SL	0.087 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.089	0.073 + 0.008*SL	0.073 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.594	0.581 + 0.007*SL	0.589 + 0.005*SL	0.599 + 0.004*SL
	t_{PHL}	0.493	0.479 + 0.007*SL	0.488 + 0.005*SL	0.506 + 0.004*SL
E to Y	t_R	0.109	0.093 + 0.008*SL	0.090 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.089	0.073 + 0.008*SL	0.074 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.626	0.613 + 0.007*SL	0.621 + 0.005*SL	0.632 + 0.004*SL
	t_{PHL}	0.490	0.476 + 0.007*SL	0.485 + 0.005*SL	0.503 + 0.004*SL
F to Y	t_R	0.111	0.096 + 0.008*SL	0.091 + 0.009*SL	0.054 + 0.010*SL
	t_F	0.089	0.072 + 0.008*SL	0.074 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.653	0.639 + 0.007*SL	0.648 + 0.005*SL	0.659 + 0.004*SL
	t_{PHL}	0.484	0.470 + 0.007*SL	0.479 + 0.005*SL	0.497 + 0.004*SL
G to Y	t_R	0.110	0.093 + 0.008*SL	0.090 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.092	0.076 + 0.008*SL	0.077 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.687	0.674 + 0.007*SL	0.682 + 0.005*SL	0.693 + 0.004*SL
	t_{PHL}	0.581	0.567 + 0.007*SL	0.576 + 0.005*SL	0.595 + 0.004*SL
H to Y	t_R	0.111	0.095 + 0.008*SL	0.091 + 0.009*SL	0.054 + 0.010*SL
	t_F	0.092	0.076 + 0.008*SL	0.078 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.707	0.694 + 0.007*SL	0.702 + 0.005*SL	0.713 + 0.004*SL
	t_{PHL}	0.568	0.554 + 0.007*SL	0.563 + 0.005*SL	0.581 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

AO4111/AO4111D2

4-AND into 4-NOR with 1X/2X Drive

Logic SymbolCell Data



Truth Table

A	B	C	D	E	F	G	Y
1	1	1	1	x	x	x	0
x	x	x	x	1	x	x	0
x	x	x	x	x	1	x	0
x	x	x	x	x	x	1	0
Other States							1

Cell Data

Input Load (SL)							Gate Count
AO4111							*AO4111*
A	B	C	D	E	F	G	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	2.67
AO4111D2							*AO4111D2*
A	B	C	D	E	F	G	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	3.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO4111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.762	0.470 + 0.146*SL	0.466 + 0.147*SL	0.520 + 0.145*SL
	t_F	0.458	0.254 + 0.102*SL	0.242 + 0.105*SL	0.239 + 0.105*SL
	t_{PLH}	0.248	0.130 + 0.059*SL	0.110 + 0.064*SL	0.112 + 0.064*SL
	t_{PHL}	0.250	0.156 + 0.047*SL	0.156 + 0.047*SL	0.158 + 0.047*SL
B to Y	t_R	0.810	0.518 + 0.146*SL	0.511 + 0.148*SL	0.564 + 0.146*SL
	t_F	0.459	0.253 + 0.103*SL	0.245 + 0.105*SL	0.239 + 0.105*SL
	t_{PLH}	0.274	0.152 + 0.061*SL	0.139 + 0.064*SL	0.140 + 0.064*SL
	t_{PHL}	0.255	0.160 + 0.047*SL	0.162 + 0.047*SL	0.165 + 0.047*SL
C to Y	t_R	0.850	0.559 + 0.145*SL	0.549 + 0.148*SL	0.601 + 0.146*SL
	t_F	0.458	0.252 + 0.103*SL	0.245 + 0.105*SL	0.239 + 0.105*SL
	t_{PLH}	0.295	0.171 + 0.062*SL	0.162 + 0.064*SL	0.163 + 0.064*SL
	t_{PHL}	0.255	0.160 + 0.048*SL	0.162 + 0.047*SL	0.166 + 0.047*SL
D to Y	t_R	0.893	0.604 + 0.144*SL	0.590 + 0.148*SL	0.639 + 0.146*SL
	t_F	0.456	0.248 + 0.104*SL	0.243 + 0.105*SL	0.239 + 0.105*SL
	t_{PLH}	0.314	0.188 + 0.063*SL	0.183 + 0.064*SL	0.185 + 0.064*SL
	t_{PHL}	0.254	0.158 + 0.048*SL	0.160 + 0.047*SL	0.165 + 0.047*SL
E to Y	t_R	0.951	0.666 + 0.143*SL	0.653 + 0.146*SL	0.640 + 0.146*SL
	t_F	0.287	0.211 + 0.038*SL	0.202 + 0.041*SL	0.185 + 0.041*SL
	t_{PLH}	0.489	0.357 + 0.066*SL	0.363 + 0.065*SL	0.373 + 0.064*SL
	t_{PHL}	0.224	0.179 + 0.023*SL	0.182 + 0.022*SL	0.187 + 0.022*SL
F to Y	t_R	0.954	0.669 + 0.142*SL	0.654 + 0.146*SL	0.640 + 0.146*SL
	t_F	0.324	0.246 + 0.039*SL	0.240 + 0.040*SL	0.222 + 0.041*SL
	t_{PLH}	0.534	0.402 + 0.066*SL	0.408 + 0.065*SL	0.419 + 0.064*SL
	t_{PHL}	0.242	0.195 + 0.023*SL	0.201 + 0.022*SL	0.211 + 0.022*SL
G to Y	t_R	0.953	0.667 + 0.143*SL	0.654 + 0.146*SL	0.640 + 0.146*SL
	t_F	0.356	0.275 + 0.040*SL	0.274 + 0.041*SL	0.261 + 0.041*SL
	t_{PLH}	0.554	0.421 + 0.066*SL	0.428 + 0.065*SL	0.439 + 0.064*SL
	t_{PHL}	0.252	0.203 + 0.024*SL	0.211 + 0.022*SL	0.230 + 0.022*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

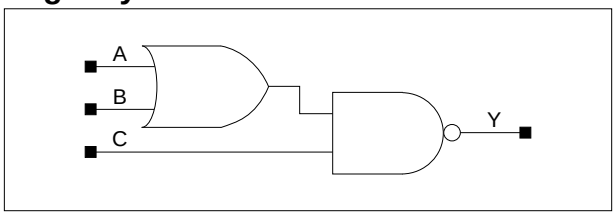
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

AO4111D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.105	0.071 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.087	0.056 + 0.015*SL	0.051 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.369	0.348 + 0.011*SL	0.355 + 0.009*SL	0.358 + 0.009*SL
	t_{PHL}	0.388	0.365 + 0.011*SL	0.375 + 0.009*SL	0.382 + 0.009*SL
B to Y	t_R	0.108	0.074 + 0.017*SL	0.065 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.087	0.056 + 0.016*SL	0.052 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.399	0.377 + 0.011*SL	0.385 + 0.009*SL	0.388 + 0.009*SL
	t_{PHL}	0.393	0.370 + 0.011*SL	0.380 + 0.009*SL	0.387 + 0.009*SL
C to Y	t_R	0.110	0.076 + 0.017*SL	0.067 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.087	0.056 + 0.015*SL	0.051 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.423	0.401 + 0.011*SL	0.409 + 0.009*SL	0.412 + 0.009*SL
	t_{PHL}	0.392	0.370 + 0.011*SL	0.379 + 0.009*SL	0.386 + 0.009*SL
D to Y	t_R	0.112	0.078 + 0.017*SL	0.069 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.087	0.056 + 0.015*SL	0.051 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.444	0.422 + 0.011*SL	0.431 + 0.009*SL	0.433 + 0.009*SL
	t_{PHL}	0.390	0.368 + 0.011*SL	0.377 + 0.009*SL	0.384 + 0.009*SL
E to Y	t_R	0.113	0.080 + 0.017*SL	0.071 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.079	0.045 + 0.017*SL	0.046 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.617	0.595 + 0.011*SL	0.603 + 0.009*SL	0.606 + 0.009*SL
	t_{PHL}	0.359	0.337 + 0.011*SL	0.346 + 0.009*SL	0.352 + 0.009*SL
F to Y	t_R	0.113	0.079 + 0.017*SL	0.071 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.080	0.047 + 0.017*SL	0.046 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.661	0.640 + 0.011*SL	0.648 + 0.009*SL	0.651 + 0.009*SL
	t_{PHL}	0.383	0.360 + 0.011*SL	0.369 + 0.009*SL	0.376 + 0.009*SL
G to Y	t_R	0.113	0.080 + 0.017*SL	0.070 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.082	0.051 + 0.016*SL	0.047 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.681	0.659 + 0.011*SL	0.668 + 0.009*SL	0.670 + 0.009*SL
	t_{PHL}	0.397	0.375 + 0.011*SL	0.384 + 0.009*SL	0.390 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	0	x	1
x	x	0	1
Others States			0

Cell Data

Input Load (SL)											
OA21			*OA21D2*			*OA21D2B*			*OA21D4*		
A	B	C	A	B	C	A	B	C	A	B	C
0.9	1.0	1.0	1.8	2.0	1.9	0.9	1.0	1.0	0.9	1.0	1.0

Gate Count			
OA21	*OA21D2*	*OA21D2B*	*OA21D4*
1.33	2.33	2.33	2.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.322	0.187 + 0.068*SL	0.166 + 0.073*SL	0.149 + 0.073*SL
	t_F	0.250	0.138 + 0.056*SL	0.120 + 0.060*SL	0.102 + 0.061*SL
	t_{PLH}	0.178	0.114 + 0.032*SL	0.113 + 0.032*SL	0.110 + 0.032*SL
	t_{PHL}	0.161	0.102 + 0.030*SL	0.104 + 0.029*SL	0.103 + 0.029*SL
B to Y	t_R	0.315	0.176 + 0.069*SL	0.163 + 0.073*SL	0.149 + 0.073*SL
	t_F	0.301	0.192 + 0.054*SL	0.171 + 0.059*SL	0.150 + 0.060*SL
	t_{PLH}	0.185	0.120 + 0.033*SL	0.121 + 0.032*SL	0.121 + 0.032*SL
	t_{PHL}	0.191	0.133 + 0.029*SL	0.134 + 0.029*SL	0.135 + 0.029*SL
C to Y	t_R	0.212	0.146 + 0.033*SL	0.126 + 0.038*SL	0.092 + 0.039*SL
	t_F	0.288	0.173 + 0.057*SL	0.163 + 0.060*SL	0.150 + 0.060*SL
	t_{PLH}	0.140	0.103 + 0.018*SL	0.107 + 0.017*SL	0.104 + 0.017*SL
	t_{PHL}	0.190	0.131 + 0.029*SL	0.133 + 0.029*SL	0.137 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

OA21D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.221	0.157 + 0.032*SL	0.138 + 0.037*SL	0.108 + 0.037*SL
	t_F	0.169	0.114 + 0.027*SL	0.101 + 0.031*SL	0.071 + 0.031*SL
	t_{PLH}	0.128	0.092 + 0.018*SL	0.099 + 0.016*SL	0.095 + 0.016*SL
	t_{PHL}	0.111	0.077 + 0.017*SL	0.087 + 0.015*SL	0.087 + 0.015*SL
B to Y	t_R	0.211	0.144 + 0.033*SL	0.130 + 0.037*SL	0.108 + 0.037*SL
	t_F	0.220	0.168 + 0.026*SL	0.153 + 0.030*SL	0.116 + 0.030*SL
	t_{PLH}	0.133	0.098 + 0.018*SL	0.104 + 0.016*SL	0.104 + 0.016*SL
	t_{PHL}	0.144	0.112 + 0.016*SL	0.116 + 0.015*SL	0.117 + 0.015*SL
C to Y	t_R	0.162	0.132 + 0.015*SL	0.117 + 0.019*SL	0.070 + 0.020*SL
	t_F	0.200	0.143 + 0.029*SL	0.136 + 0.030*SL	0.116 + 0.030*SL
	t_{PLH}	0.110	0.088 + 0.011*SL	0.096 + 0.009*SL	0.095 + 0.009*SL
	t_{PHL}	0.139	0.108 + 0.016*SL	0.112 + 0.015*SL	0.116 + 0.015*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA21D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.094	0.058 + 0.018*SL	0.052 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.079	0.048 + 0.016*SL	0.045 + 0.016*SL	0.025 + 0.017*SL
	t_{PLH}	0.285	0.264 + 0.010*SL	0.270 + 0.009*SL	0.272 + 0.009*SL
	t_{PHL}	0.263	0.241 + 0.011*SL	0.250 + 0.009*SL	0.256 + 0.009*SL
B to Y	t_R	0.094	0.060 + 0.017*SL	0.052 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.081	0.050 + 0.015*SL	0.046 + 0.016*SL	0.025 + 0.017*SL
	t_{PLH}	0.288	0.267 + 0.010*SL	0.273 + 0.009*SL	0.275 + 0.009*SL
	t_{PHL}	0.304	0.281 + 0.011*SL	0.291 + 0.009*SL	0.297 + 0.009*SL
C to Y	t_R	0.093	0.058 + 0.017*SL	0.051 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.079	0.046 + 0.016*SL	0.046 + 0.016*SL	0.025 + 0.017*SL
	t_{PLH}	0.257	0.237 + 0.010*SL	0.242 + 0.009*SL	0.244 + 0.009*SL
	t_{PHL}	0.299	0.277 + 0.011*SL	0.286 + 0.009*SL	0.292 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OA21D4

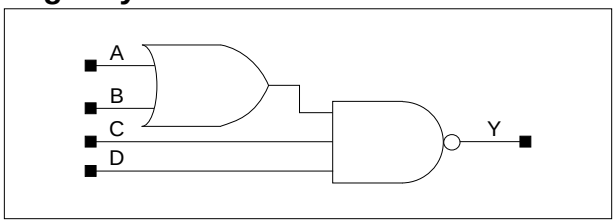
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.093	0.076 + 0.009*SL	0.073 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.080	0.063 + 0.008*SL	0.065 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.320	0.308 + 0.006*SL	0.314 + 0.005*SL	0.324 + 0.004*SL
	t_{PHL}	0.296	0.283 + 0.007*SL	0.291 + 0.005*SL	0.308 + 0.004*SL
B to Y	t_R	0.093	0.075 + 0.009*SL	0.074 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.081	0.065 + 0.008*SL	0.065 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.323	0.311 + 0.006*SL	0.317 + 0.005*SL	0.327 + 0.004*SL
	t_{PHL}	0.338	0.324 + 0.007*SL	0.332 + 0.005*SL	0.350 + 0.004*SL
C to Y	t_R	0.092	0.075 + 0.008*SL	0.071 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.081	0.064 + 0.009*SL	0.066 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.291	0.279 + 0.006*SL	0.286 + 0.005*SL	0.295 + 0.004*SL
	t_{PHL}	0.333	0.320 + 0.007*SL	0.328 + 0.005*SL	0.345 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OA211/OA211D2/OA211D2B/OA211D4

2-OR into 3-NAND with 1X/2X/2X(Buffered)/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1
Other States				0

Cell Data

Input Load (SL)															
OA211				*OA211D2*				*OA211D2B*				*OA211D4*			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
1.0	1.0	1.0	1.0	2.0	2.0	2.0	1.9	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

Input Load (SL)			
OA211	*OA211D2*	*OA211D2B*	*OA211D4*
1.67	2.67	2.67	3.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.332	0.194 + 0.069*SL	0.176 + 0.074*SL	0.162 + 0.074*SL
	t_F	0.327	0.183 + 0.072*SL	0.169 + 0.076*SL	0.158 + 0.076*SL
	t_{PLH}	0.188	0.124 + 0.032*SL	0.122 + 0.033*SL	0.120 + 0.033*SL
	t_{PHL}	0.183	0.114 + 0.035*SL	0.114 + 0.035*SL	0.114 + 0.035*SL
B to Y	t_R	0.328	0.187 + 0.070*SL	0.174 + 0.074*SL	0.162 + 0.074*SL
	t_F	0.391	0.248 + 0.072*SL	0.229 + 0.076*SL	0.215 + 0.077*SL
	t_{PLH}	0.192	0.126 + 0.033*SL	0.128 + 0.033*SL	0.128 + 0.033*SL
	t_{PHL}	0.220	0.150 + 0.035*SL	0.151 + 0.035*SL	0.151 + 0.035*SL
C to Y	t_R	0.221	0.154 + 0.033*SL	0.136 + 0.038*SL	0.104 + 0.039*SL
	t_F	0.384	0.236 + 0.074*SL	0.226 + 0.076*SL	0.215 + 0.077*SL
	t_{PLH}	0.147	0.111 + 0.018*SL	0.114 + 0.017*SL	0.112 + 0.017*SL
	t_{PHL}	0.237	0.166 + 0.036*SL	0.169 + 0.035*SL	0.173 + 0.035*SL
D to Y	t_R	0.233	0.167 + 0.033*SL	0.148 + 0.038*SL	0.114 + 0.039*SL
	t_F	0.381	0.233 + 0.074*SL	0.224 + 0.076*SL	0.215 + 0.077*SL
	t_{PLH}	0.153	0.118 + 0.018*SL	0.120 + 0.017*SL	0.118 + 0.017*SL
	t_{PHL}	0.228	0.157 + 0.036*SL	0.160 + 0.035*SL	0.164 + 0.035*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

OA211D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.261	0.194 + 0.033*SL	0.181 + 0.037*SL	0.157 + 0.037*SL
	t_F	0.251	0.182 + 0.035*SL	0.171 + 0.038*SL	0.152 + 0.038*SL
	t_{PLH}	0.153	0.119 + 0.017*SL	0.121 + 0.016*SL	0.119 + 0.016*SL
	t_{PHL}	0.146	0.110 + 0.018*SL	0.112 + 0.017*SL	0.112 + 0.017*SL
B to Y	t_R	0.254	0.186 + 0.034*SL	0.175 + 0.037*SL	0.157 + 0.037*SL
	t_F	0.315	0.246 + 0.034*SL	0.231 + 0.038*SL	0.208 + 0.038*SL
	t_{PLH}	0.156	0.122 + 0.017*SL	0.125 + 0.016*SL	0.126 + 0.016*SL
	t_{PHL}	0.183	0.147 + 0.018*SL	0.148 + 0.017*SL	0.149 + 0.017*SL
C to Y	t_R	0.186	0.155 + 0.016*SL	0.143 + 0.019*SL	0.101 + 0.019*SL
	t_F	0.305	0.232 + 0.036*SL	0.224 + 0.038*SL	0.208 + 0.038*SL
	t_{PLH}	0.127	0.107 + 0.010*SL	0.112 + 0.009*SL	0.111 + 0.009*SL
	t_{PHL}	0.198	0.163 + 0.018*SL	0.164 + 0.017*SL	0.169 + 0.017*SL
D to Y	t_R	0.200	0.169 + 0.016*SL	0.156 + 0.019*SL	0.113 + 0.020*SL
	t_F	0.301	0.228 + 0.037*SL	0.221 + 0.038*SL	0.208 + 0.038*SL
	t_{PLH}	0.134	0.114 + 0.010*SL	0.119 + 0.009*SL	0.117 + 0.009*SL
	t_{PHL}	0.190	0.154 + 0.018*SL	0.155 + 0.017*SL	0.161 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA211D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.095	0.061 + 0.017*SL	0.053 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.083	0.050 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.311	0.290 + 0.010*SL	0.297 + 0.009*SL	0.299 + 0.009*SL
	t_{PHL}	0.321	0.299 + 0.011*SL	0.308 + 0.009*SL	0.315 + 0.009*SL
B to Y	t_R	0.096	0.061 + 0.017*SL	0.053 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.085	0.053 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.316	0.295 + 0.010*SL	0.302 + 0.009*SL	0.303 + 0.009*SL
	t_{PHL}	0.368	0.345 + 0.011*SL	0.354 + 0.009*SL	0.361 + 0.009*SL
C to Y	t_R	0.093	0.057 + 0.018*SL	0.052 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.085	0.054 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.276	0.255 + 0.010*SL	0.261 + 0.009*SL	0.263 + 0.009*SL
	t_{PHL}	0.386	0.363 + 0.011*SL	0.373 + 0.009*SL	0.379 + 0.009*SL
D to Y	t_R	0.094	0.060 + 0.017*SL	0.051 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.083	0.050 + 0.017*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.283	0.263 + 0.010*SL	0.269 + 0.009*SL	0.270 + 0.009*SL
	t_{PHL}	0.377	0.354 + 0.011*SL	0.364 + 0.009*SL	0.370 + 0.009*SL

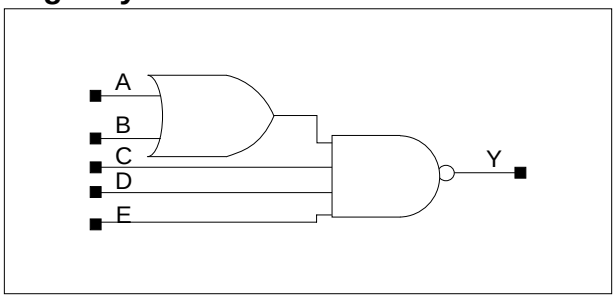
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OA211D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.094	0.076 + 0.009*SL	0.075 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.085	0.068 + 0.008*SL	0.069 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.348	0.336 + 0.006*SL	0.343 + 0.005*SL	0.353 + 0.004*SL
	t_{PHL}	0.356	0.343 + 0.007*SL	0.351 + 0.005*SL	0.369 + 0.004*SL
B to Y	t_R	0.095	0.078 + 0.008*SL	0.075 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.086	0.069 + 0.008*SL	0.070 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.353	0.340 + 0.006*SL	0.347 + 0.005*SL	0.357 + 0.004*SL
	t_{PHL}	0.401	0.387 + 0.007*SL	0.396 + 0.005*SL	0.414 + 0.004*SL
C to Y	t_R	0.093	0.076 + 0.009*SL	0.072 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.086	0.069 + 0.008*SL	0.071 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.311	0.299 + 0.006*SL	0.306 + 0.005*SL	0.315 + 0.004*SL
	t_{PHL}	0.418	0.404 + 0.007*SL	0.413 + 0.005*SL	0.431 + 0.004*SL
D to Y	t_R	0.093	0.076 + 0.009*SL	0.073 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.086	0.070 + 0.008*SL	0.070 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.319	0.307 + 0.006*SL	0.313 + 0.005*SL	0.323 + 0.004*SL
	t_{PHL}	0.409	0.395 + 0.007*SL	0.404 + 0.005*SL	0.422 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)										Gate Count	
OA2111					*OA2111D2*					*OA2111*	*OA2111D2*
A	B	C	D	E	A	B	C	D	E		
1.0	1.0	1.1	1.1	1.1	2.0	2.0	2.2	2.1	2.1	2.33	3.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA2111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.372	0.233 + 0.069*SL	0.216 + 0.074*SL	0.204 + 0.074*SL
	t_F	0.398	0.242 + 0.078*SL	0.229 + 0.081*SL	0.223 + 0.081*SL
	t_{PLH}	0.204	0.139 + 0.032*SL	0.138 + 0.033*SL	0.136 + 0.033*SL
	t_{PHL}	0.209	0.137 + 0.036*SL	0.136 + 0.036*SL	0.136 + 0.036*SL
B to Y	t_R	0.367	0.225 + 0.071*SL	0.214 + 0.074*SL	0.204 + 0.074*SL
	t_F	0.455	0.303 + 0.076*SL	0.287 + 0.080*SL	0.278 + 0.081*SL
	t_{PLH}	0.209	0.144 + 0.033*SL	0.144 + 0.033*SL	0.144 + 0.033*SL
	t_{PHL}	0.244	0.172 + 0.036*SL	0.173 + 0.036*SL	0.173 + 0.036*SL
C to Y	t_R	0.239	0.171 + 0.034*SL	0.155 + 0.038*SL	0.127 + 0.039*SL
	t_F	0.453	0.296 + 0.078*SL	0.288 + 0.080*SL	0.278 + 0.081*SL
	t_{PLH}	0.160	0.124 + 0.018*SL	0.126 + 0.017*SL	0.124 + 0.017*SL
	t_{PHL}	0.262	0.189 + 0.037*SL	0.191 + 0.036*SL	0.195 + 0.036*SL
D to Y	t_R	0.257	0.190 + 0.034*SL	0.173 + 0.038*SL	0.143 + 0.039*SL
	t_F	0.451	0.294 + 0.078*SL	0.287 + 0.080*SL	0.278 + 0.081*SL
	t_{PLH}	0.169	0.134 + 0.018*SL	0.134 + 0.017*SL	0.134 + 0.017*SL
	t_{PHL}	0.266	0.192 + 0.037*SL	0.195 + 0.036*SL	0.200 + 0.036*SL
E to Y	t_R	0.276	0.209 + 0.033*SL	0.192 + 0.038*SL	0.159 + 0.039*SL
	t_F	0.449	0.291 + 0.079*SL	0.285 + 0.080*SL	0.278 + 0.081*SL
	t_{PLH}	0.175	0.140 + 0.018*SL	0.141 + 0.017*SL	0.142 + 0.017*SL
	t_{PHL}	0.265	0.190 + 0.037*SL	0.194 + 0.036*SL	0.199 + 0.036*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA2111D2

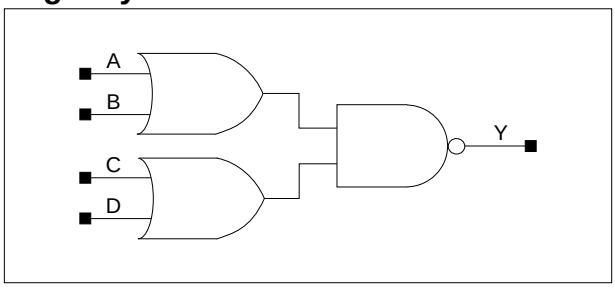
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.285	0.218 + 0.034*SL	0.206 + 0.037*SL	0.186 + 0.037*SL
	t_F	0.301	0.225 + 0.038*SL	0.216 + 0.040*SL	0.203 + 0.040*SL
	t_{PLH}	0.165	0.132 + 0.016*SL	0.133 + 0.016*SL	0.130 + 0.016*SL
	t_{PHL}	0.163	0.127 + 0.018*SL	0.126 + 0.018*SL	0.127 + 0.018*SL
B to Y	t_R	0.280	0.211 + 0.034*SL	0.201 + 0.037*SL	0.186 + 0.037*SL
	t_F	0.367	0.292 + 0.038*SL	0.280 + 0.041*SL	0.262 + 0.041*SL
	t_{PLH}	0.168	0.135 + 0.017*SL	0.137 + 0.016*SL	0.137 + 0.016*SL
	t_{PHL}	0.200	0.164 + 0.018*SL	0.164 + 0.018*SL	0.165 + 0.018*SL
C to Y	t_R	0.198	0.167 + 0.016*SL	0.154 + 0.019*SL	0.118 + 0.019*SL
	t_F	0.361	0.283 + 0.039*SL	0.277 + 0.041*SL	0.262 + 0.041*SL
	t_{PLH}	0.138	0.119 + 0.010*SL	0.122 + 0.009*SL	0.121 + 0.009*SL
	t_{PHL}	0.218	0.180 + 0.019*SL	0.182 + 0.018*SL	0.187 + 0.018*SL
D to Y	t_R	0.216	0.185 + 0.016*SL	0.173 + 0.019*SL	0.134 + 0.019*SL
	t_F	0.359	0.280 + 0.039*SL	0.275 + 0.041*SL	0.262 + 0.041*SL
	t_{PLH}	0.147	0.128 + 0.009*SL	0.131 + 0.009*SL	0.130 + 0.009*SL
	t_{PHL}	0.220	0.183 + 0.019*SL	0.185 + 0.018*SL	0.191 + 0.018*SL
E to Y	t_R	0.234	0.202 + 0.016*SL	0.191 + 0.019*SL	0.149 + 0.019*SL
	t_F	0.356	0.277 + 0.039*SL	0.272 + 0.041*SL	0.262 + 0.041*SL
	t_{PLH}	0.153	0.135 + 0.009*SL	0.137 + 0.009*SL	0.138 + 0.009*SL
	t_{PHL}	0.219	0.181 + 0.019*SL	0.183 + 0.018*SL	0.190 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OA22/OA22D2/OA22D2B/OA22D4

Two 2-ORs into 2-NAND with 1X/2X/2X(Buffered)/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	0	0	1
Other States				0

Cell Data

Input Load (SL)															
OA22				*OA22D2*				*OA22D2B*				*OA22D4*			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.9	1.0	0.9	1.0	1.9	1.9	1.9	1.9	0.9	1.0	1.0	1.0	0.9	1.0	1.0	1.0

Gate Count			
OA22	*OA22D2*	*OA22D2B*	*OA22D4*
1.67	2.67	2.67	3.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.371	0.238 + 0.067*SL	0.211 + 0.073*SL	0.190 + 0.074*SL
	t_F	0.281	0.157 + 0.062*SL	0.141 + 0.066*SL	0.126 + 0.066*SL
	t_{PLH}	0.171	0.104 + 0.033*SL	0.107 + 0.033*SL	0.111 + 0.033*SL
	t_{PHL}	0.192	0.127 + 0.032*SL	0.130 + 0.032*SL	0.133 + 0.032*SL
B to Y	t_R	0.363	0.225 + 0.069*SL	0.207 + 0.073*SL	0.190 + 0.074*SL
	t_F	0.332	0.209 + 0.061*SL	0.192 + 0.066*SL	0.175 + 0.066*SL
	t_{PLH}	0.174	0.106 + 0.034*SL	0.111 + 0.033*SL	0.118 + 0.033*SL
	t_{PHL}	0.224	0.159 + 0.033*SL	0.162 + 0.032*SL	0.164 + 0.032*SL
C to Y	t_R	0.410	0.277 + 0.067*SL	0.249 + 0.073*SL	0.229 + 0.074*SL
	t_F	0.275	0.149 + 0.063*SL	0.137 + 0.066*SL	0.126 + 0.066*SL
	t_{PLH}	0.197	0.131 + 0.033*SL	0.132 + 0.033*SL	0.136 + 0.033*SL
	t_{PHL}	0.190	0.124 + 0.033*SL	0.129 + 0.032*SL	0.134 + 0.032*SL
D to Y	t_R	0.401	0.263 + 0.069*SL	0.245 + 0.073*SL	0.229 + 0.074*SL
	t_F	0.326	0.200 + 0.063*SL	0.188 + 0.066*SL	0.175 + 0.066*SL
	t_{PLH}	0.201	0.134 + 0.033*SL	0.136 + 0.033*SL	0.143 + 0.033*SL
	t_{PHL}	0.223	0.157 + 0.033*SL	0.161 + 0.032*SL	0.166 + 0.032*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

OA22D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.321	0.257 + 0.032*SL	0.239 + 0.036*SL	0.207 + 0.037*SL
	t_F	0.234	0.172 + 0.031*SL	0.163 + 0.033*SL	0.142 + 0.034*SL
	t_{PLH}	0.143	0.108 + 0.018*SL	0.113 + 0.016*SL	0.118 + 0.016*SL
	t_{PHL}	0.170	0.137 + 0.017*SL	0.139 + 0.016*SL	0.143 + 0.016*SL
B to Y	t_R	0.311	0.245 + 0.033*SL	0.232 + 0.037*SL	0.207 + 0.037*SL
	t_F	0.289	0.227 + 0.031*SL	0.216 + 0.034*SL	0.193 + 0.034*SL
	t_{PLH}	0.147	0.112 + 0.018*SL	0.117 + 0.016*SL	0.124 + 0.016*SL
	t_{PHL}	0.204	0.170 + 0.017*SL	0.172 + 0.016*SL	0.176 + 0.016*SL
C to Y	t_R	0.355	0.291 + 0.032*SL	0.273 + 0.037*SL	0.241 + 0.037*SL
	t_F	0.227	0.164 + 0.032*SL	0.157 + 0.033*SL	0.141 + 0.034*SL
	t_{PLH}	0.167	0.134 + 0.017*SL	0.135 + 0.016*SL	0.139 + 0.016*SL
	t_{PHL}	0.165	0.131 + 0.017*SL	0.134 + 0.016*SL	0.140 + 0.016*SL
D to Y	t_R	0.344	0.277 + 0.034*SL	0.265 + 0.037*SL	0.241 + 0.037*SL
	t_F	0.282	0.219 + 0.032*SL	0.210 + 0.034*SL	0.193 + 0.034*SL
	t_{PLH}	0.171	0.137 + 0.017*SL	0.139 + 0.016*SL	0.146 + 0.016*SL
	t_{PHL}	0.201	0.167 + 0.017*SL	0.169 + 0.016*SL	0.175 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA22D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.099	0.064 + 0.017*SL	0.057 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.082	0.050 + 0.016*SL	0.047 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.306	0.285 + 0.010*SL	0.291 + 0.009*SL	0.293 + 0.009*SL
	t_{PHL}	0.321	0.299 + 0.011*SL	0.308 + 0.009*SL	0.314 + 0.009*SL
B to Y	t_R	0.099	0.065 + 0.017*SL	0.056 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.082	0.048 + 0.017*SL	0.049 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.310	0.289 + 0.010*SL	0.295 + 0.009*SL	0.297 + 0.009*SL
	t_{PHL}	0.365	0.343 + 0.011*SL	0.352 + 0.009*SL	0.358 + 0.009*SL
C to Y	t_R	0.099	0.065 + 0.017*SL	0.057 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.082	0.049 + 0.016*SL	0.048 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.329	0.309 + 0.010*SL	0.315 + 0.009*SL	0.317 + 0.009*SL
	t_{PHL}	0.318	0.296 + 0.011*SL	0.305 + 0.009*SL	0.311 + 0.009*SL
D to Y	t_R	0.100	0.066 + 0.017*SL	0.057 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.084	0.052 + 0.016*SL	0.049 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.332	0.312 + 0.010*SL	0.318 + 0.009*SL	0.320 + 0.009*SL
	t_{PHL}	0.357	0.335 + 0.011*SL	0.344 + 0.009*SL	0.350 + 0.009*SL

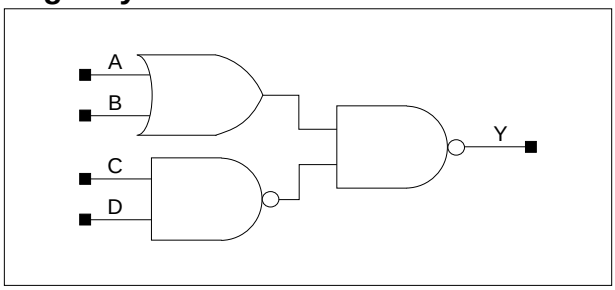
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OA22D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.099	0.082 + 0.009*SL	0.079 + 0.009*SL	0.049 + 0.010*SL
	t_F	0.082	0.064 + 0.009*SL	0.067 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.346	0.334 + 0.006*SL	0.341 + 0.004*SL	0.351 + 0.004*SL
	t_{PHL}	0.356	0.342 + 0.007*SL	0.351 + 0.005*SL	0.368 + 0.004*SL
B to Y	t_R	0.098	0.081 + 0.008*SL	0.078 + 0.009*SL	0.049 + 0.010*SL
	t_F	0.083	0.067 + 0.008*SL	0.067 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.350	0.338 + 0.006*SL	0.345 + 0.004*SL	0.355 + 0.004*SL
	t_{PHL}	0.400	0.387 + 0.007*SL	0.395 + 0.005*SL	0.412 + 0.004*SL
C to Y	t_R	0.099	0.083 + 0.008*SL	0.079 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.082	0.065 + 0.009*SL	0.067 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.372	0.359 + 0.006*SL	0.366 + 0.004*SL	0.376 + 0.004*SL
	t_{PHL}	0.353	0.340 + 0.007*SL	0.348 + 0.005*SL	0.366 + 0.004*SL
D to Y	t_R	0.099	0.082 + 0.008*SL	0.078 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.083	0.067 + 0.008*SL	0.068 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.375	0.362 + 0.006*SL	0.369 + 0.004*SL	0.379 + 0.004*SL
	t_{PHL}	0.393	0.380 + 0.007*SL	0.388 + 0.005*SL	0.405 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	1	1	1
	Other States			0

Cell Data

Input Load (SL)												Gate Count		
OA22A				*OA22D2A*				*OA22D4A*				*OA22A*	*OA22D2A*	*OA22D4A*
A	B	C	D	A	B	C	D	A	B	C	D			
0.9	1.0	1.0	1.0	1.8	2.0	1.0	1.0	0.9	1.0	1.0	1.0	2.00	2.67	3.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.287	0.153 + 0.067*SL	0.128 + 0.073*SL	0.109 + 0.074*SL
	t_F	0.220	0.110 + 0.055*SL	0.091 + 0.060*SL	0.070 + 0.060*SL
	t_{PLH}	0.163	0.097 + 0.033*SL	0.099 + 0.033*SL	0.096 + 0.033*SL
	t_{PHL}	0.141	0.081 + 0.030*SL	0.087 + 0.029*SL	0.086 + 0.029*SL
B to Y	t_R	0.279	0.140 + 0.070*SL	0.124 + 0.074*SL	0.109 + 0.074*SL
	t_F	0.274	0.165 + 0.054*SL	0.140 + 0.060*SL	0.116 + 0.061*SL
	t_{PLH}	0.167	0.100 + 0.033*SL	0.103 + 0.033*SL	0.102 + 0.033*SL
	t_{PHL}	0.174	0.114 + 0.030*SL	0.116 + 0.029*SL	0.116 + 0.029*SL
C to Y	t_R	0.173	0.102 + 0.036*SL	0.091 + 0.038*SL	0.075 + 0.039*SL
	t_F	0.247	0.128 + 0.059*SL	0.122 + 0.061*SL	0.116 + 0.061*SL
	t_{PLH}	0.211	0.173 + 0.019*SL	0.179 + 0.017*SL	0.180 + 0.017*SL
	t_{PHL}	0.252	0.191 + 0.031*SL	0.196 + 0.029*SL	0.202 + 0.029*SL
D to Y	t_R	0.173	0.102 + 0.036*SL	0.091 + 0.038*SL	0.075 + 0.039*SL
	t_F	0.247	0.128 + 0.060*SL	0.122 + 0.061*SL	0.116 + 0.061*SL
	t_{PLH}	0.199	0.161 + 0.019*SL	0.167 + 0.017*SL	0.168 + 0.017*SL
	t_{PHL}	0.263	0.201 + 0.031*SL	0.206 + 0.029*SL	0.212 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA22D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.224	0.159 + 0.032*SL	0.141 + 0.037*SL	0.111 + 0.037*SL
	t_F	0.170	0.116 + 0.027*SL	0.102 + 0.030*SL	0.073 + 0.031*SL
	t_{PLH}	0.129	0.093 + 0.018*SL	0.100 + 0.016*SL	0.095 + 0.016*SL
	t_{PHL}	0.113	0.078 + 0.017*SL	0.088 + 0.015*SL	0.089 + 0.015*SL
B to Y	t_R	0.214	0.147 + 0.033*SL	0.133 + 0.037*SL	0.111 + 0.037*SL
	t_F	0.220	0.169 + 0.026*SL	0.154 + 0.030*SL	0.118 + 0.030*SL
	t_{PLH}	0.135	0.099 + 0.018*SL	0.105 + 0.016*SL	0.105 + 0.016*SL
	t_{PHL}	0.144	0.113 + 0.015*SL	0.117 + 0.014*SL	0.118 + 0.014*SL
C to Y	t_R	0.151	0.115 + 0.018*SL	0.110 + 0.019*SL	0.082 + 0.019*SL
	t_F	0.191	0.133 + 0.029*SL	0.129 + 0.030*SL	0.118 + 0.030*SL
	t_{PLH}	0.234	0.213 + 0.011*SL	0.219 + 0.009*SL	0.228 + 0.009*SL
	t_{PHL}	0.249	0.218 + 0.016*SL	0.222 + 0.015*SL	0.230 + 0.014*SL
D to Y	t_R	0.152	0.117 + 0.017*SL	0.111 + 0.019*SL	0.082 + 0.019*SL
	t_F	0.192	0.134 + 0.029*SL	0.130 + 0.030*SL	0.118 + 0.030*SL
	t_{PLH}	0.220	0.199 + 0.011*SL	0.206 + 0.009*SL	0.214 + 0.009*SL
	t_{PHL}	0.258	0.227 + 0.016*SL	0.231 + 0.015*SL	0.238 + 0.014*SL

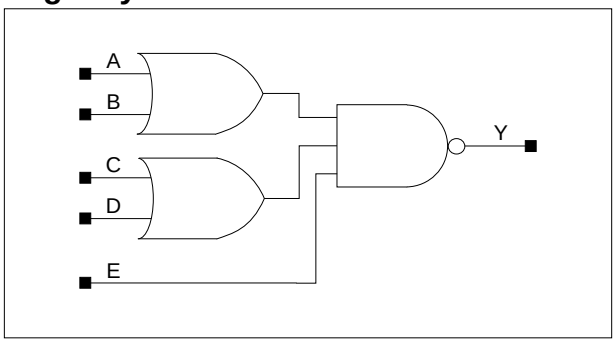
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OA22D4A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.094	0.077 + 0.008*SL	0.073 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.080	0.062 + 0.009*SL	0.065 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.321	0.309 + 0.006*SL	0.316 + 0.005*SL	0.325 + 0.004*SL
	t_{PHL}	0.297	0.283 + 0.007*SL	0.291 + 0.005*SL	0.309 + 0.004*SL
B to Y	t_R	0.093	0.075 + 0.009*SL	0.074 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.082	0.065 + 0.008*SL	0.066 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.325	0.313 + 0.006*SL	0.320 + 0.005*SL	0.330 + 0.004*SL
	t_{PHL}	0.339	0.325 + 0.007*SL	0.333 + 0.005*SL	0.351 + 0.004*SL
C to Y	t_R	0.093	0.075 + 0.009*SL	0.073 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.081	0.065 + 0.008*SL	0.065 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.375	0.362 + 0.006*SL	0.369 + 0.005*SL	0.378 + 0.004*SL
	t_{PHL}	0.415	0.401 + 0.007*SL	0.410 + 0.005*SL	0.427 + 0.004*SL
D to Y	t_R	0.093	0.076 + 0.009*SL	0.072 + 0.009*SL	0.046 + 0.010*SL
	t_F	0.081	0.065 + 0.008*SL	0.066 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.363	0.350 + 0.006*SL	0.357 + 0.005*SL	0.366 + 0.004*SL
	t_{PHL}	0.425	0.411 + 0.007*SL	0.420 + 0.005*SL	0.437 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	x	x	x	1
x	x	0	0	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)														
OA221					*OA221D2*					*OA221D4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.9	0.9	0.9	1.0	1.0	1.8	1.9	1.9	2.0	2.0	0.9	1.0	0.9	1.0	1.0

Gate Count		
OA221	*OA221D2*	*OA221D4*
2.33	3.33	3.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA221

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.434	0.297 + 0.068*SL	0.276 + 0.073*SL	0.259 + 0.074*SL
	t_F	0.415	0.256 + 0.079*SL	0.245 + 0.082*SL	0.238 + 0.082*SL
	t_{PLH}	0.197	0.131 + 0.033*SL	0.132 + 0.033*SL	0.137 + 0.033*SL
	t_{PHL}	0.253	0.176 + 0.039*SL	0.179 + 0.038*SL	0.182 + 0.038*SL
B to Y	t_R	0.428	0.288 + 0.070*SL	0.273 + 0.074*SL	0.259 + 0.074*SL
	t_F	0.481	0.323 + 0.079*SL	0.310 + 0.082*SL	0.302 + 0.082*SL
	t_{PLH}	0.204	0.137 + 0.033*SL	0.140 + 0.033*SL	0.147 + 0.033*SL
	t_{PHL}	0.296	0.219 + 0.038*SL	0.221 + 0.038*SL	0.224 + 0.038*SL
C to Y	t_R	0.479	0.344 + 0.068*SL	0.321 + 0.073*SL	0.305 + 0.074*SL
	t_F	0.424	0.262 + 0.081*SL	0.253 + 0.083*SL	0.245 + 0.084*SL
	t_{PLH}	0.224	0.158 + 0.033*SL	0.160 + 0.033*SL	0.166 + 0.033*SL
	t_{PHL}	0.272	0.193 + 0.039*SL	0.197 + 0.038*SL	0.203 + 0.038*SL
D to Y	t_R	0.473	0.333 + 0.070*SL	0.319 + 0.074*SL	0.305 + 0.074*SL
	t_F	0.480	0.320 + 0.080*SL	0.311 + 0.082*SL	0.302 + 0.082*SL
	t_{PLH}	0.231	0.164 + 0.033*SL	0.166 + 0.033*SL	0.174 + 0.033*SL
	t_{PHL}	0.311	0.233 + 0.039*SL	0.236 + 0.038*SL	0.241 + 0.038*SL
E to Y	t_R	0.339	0.275 + 0.032*SL	0.253 + 0.038*SL	0.213 + 0.039*SL
	t_F	0.477	0.316 + 0.081*SL	0.309 + 0.082*SL	0.302 + 0.082*SL
	t_{PLH}	0.162	0.125 + 0.018*SL	0.127 + 0.018*SL	0.136 + 0.017*SL
	t_{PHL}	0.311	0.232 + 0.039*SL	0.236 + 0.038*SL	0.244 + 0.038*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA221D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.339	0.274 + 0.032*SL	0.256 + 0.037*SL	0.227 + 0.037*SL
	t_F	0.304	0.227 + 0.039*SL	0.217 + 0.041*SL	0.202 + 0.041*SL
	t_{PLH}	0.149	0.115 + 0.017*SL	0.119 + 0.016*SL	0.125 + 0.016*SL
	t_{PHL}	0.198	0.159 + 0.020*SL	0.161 + 0.019*SL	0.165 + 0.019*SL
B to Y	t_R	0.329	0.261 + 0.034*SL	0.249 + 0.037*SL	0.227 + 0.037*SL
	t_F	0.366	0.290 + 0.038*SL	0.280 + 0.041*SL	0.263 + 0.041*SL
	t_{PLH}	0.157	0.122 + 0.018*SL	0.126 + 0.016*SL	0.135 + 0.016*SL
	t_{PHL}	0.239	0.200 + 0.019*SL	0.202 + 0.019*SL	0.206 + 0.019*SL
C to Y	t_R	0.376	0.312 + 0.032*SL	0.294 + 0.037*SL	0.265 + 0.037*SL
	t_F	0.308	0.228 + 0.040*SL	0.221 + 0.042*SL	0.207 + 0.042*SL
	t_{PLH}	0.175	0.142 + 0.017*SL	0.142 + 0.016*SL	0.149 + 0.016*SL
	t_{PHL}	0.209	0.169 + 0.020*SL	0.172 + 0.019*SL	0.181 + 0.019*SL
D to Y	t_R	0.366	0.298 + 0.034*SL	0.287 + 0.037*SL	0.265 + 0.037*SL
	t_F	0.363	0.286 + 0.039*SL	0.278 + 0.041*SL	0.263 + 0.041*SL
	t_{PLH}	0.181	0.148 + 0.017*SL	0.149 + 0.016*SL	0.159 + 0.016*SL
	t_{PHL}	0.249	0.209 + 0.020*SL	0.212 + 0.019*SL	0.219 + 0.019*SL
E to Y	t_R	0.241	0.210 + 0.015*SL	0.197 + 0.019*SL	0.149 + 0.019*SL
	t_F	0.359	0.279 + 0.040*SL	0.275 + 0.041*SL	0.263 + 0.041*SL
	t_{PLH}	0.134	0.114 + 0.010*SL	0.119 + 0.009*SL	0.122 + 0.009*SL
	t_{PHL}	0.245	0.205 + 0.020*SL	0.208 + 0.019*SL	0.218 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

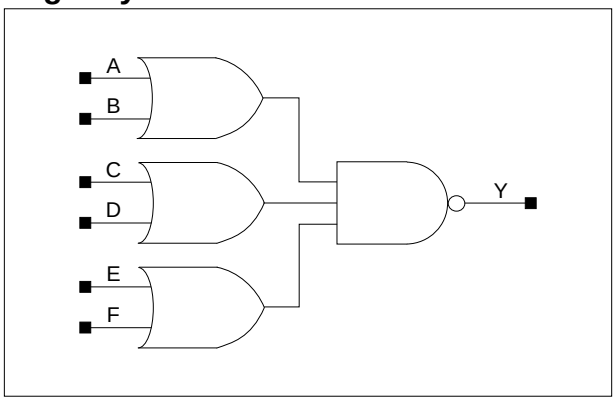
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA221D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.100	0.083 + 0.008*SL	0.079 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.087	0.070 + 0.008*SL	0.071 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.372	0.359 + 0.006*SL	0.367 + 0.005*SL	0.377 + 0.004*SL
	t_{PHL}	0.440	0.426 + 0.007*SL	0.435 + 0.005*SL	0.453 + 0.004*SL
B to Y	t_R	0.099	0.083 + 0.008*SL	0.079 + 0.009*SL	0.049 + 0.010*SL
	t_F	0.088	0.072 + 0.008*SL	0.072 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.378	0.365 + 0.006*SL	0.372 + 0.005*SL	0.382 + 0.004*SL
	t_{PHL}	0.493	0.479 + 0.007*SL	0.488 + 0.005*SL	0.505 + 0.004*SL
C to Y	t_R	0.100	0.084 + 0.008*SL	0.080 + 0.009*SL	0.049 + 0.010*SL
	t_F	0.086	0.069 + 0.008*SL	0.071 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.399	0.386 + 0.006*SL	0.394 + 0.005*SL	0.404 + 0.004*SL
	t_{PHL}	0.439	0.425 + 0.007*SL	0.434 + 0.005*SL	0.452 + 0.004*SL
D to Y	t_R	0.100	0.083 + 0.008*SL	0.080 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.088	0.072 + 0.008*SL	0.073 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.411	0.399 + 0.006*SL	0.406 + 0.005*SL	0.416 + 0.004*SL
	t_{PHL}	0.506	0.492 + 0.007*SL	0.501 + 0.005*SL	0.519 + 0.004*SL
E to Y	t_R	0.096	0.079 + 0.008*SL	0.076 + 0.009*SL	0.047 + 0.010*SL
	t_F	0.088	0.072 + 0.008*SL	0.073 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.337	0.324 + 0.006*SL	0.331 + 0.004*SL	0.341 + 0.004*SL
	t_{PHL}	0.505	0.491 + 0.007*SL	0.500 + 0.005*SL	0.518 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	x	x	x	x	1
x	x	0	0	x	x	1
x	x	x	x	0	0	1
Other States						0

Cell Data

Input Load (SL)												Gate Count	
OA222						*OA222D2*						*OA222*	*OA222D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.9	0.9	0.9	1.0	0.9	1.0	1.8	1.9	1.8	1.9	1.8	1.9	2.33	4.33
OA222D2B						*OA222D4*						*OA222D2B*	*OA222D4*
A	B	C	D	E	F	A	B	C	D	E	F		
0.9	1.0	0.9	1.0	0.9	1.0	0.9	1.0	0.9	1.0	0.9	1.0	3.33	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.507	0.372 + 0.068*SL	0.349 + 0.073*SL	0.330 + 0.074*SL
	t_F	0.516	0.334 + 0.091*SL	0.325 + 0.093*SL	0.321 + 0.093*SL
	t_{PLH}	0.200	0.132 + 0.034*SL	0.135 + 0.033*SL	0.147 + 0.033*SL
	t_{PHL}	0.327	0.239 + 0.044*SL	0.243 + 0.043*SL	0.249 + 0.043*SL
B to Y	t_R	0.500	0.361 + 0.070*SL	0.346 + 0.073*SL	0.330 + 0.074*SL
	t_F	0.596	0.413 + 0.091*SL	0.406 + 0.093*SL	0.401 + 0.093*SL
	t_{PLH}	0.211	0.143 + 0.034*SL	0.148 + 0.033*SL	0.161 + 0.033*SL
	t_{PHL}	0.382	0.295 + 0.044*SL	0.298 + 0.043*SL	0.304 + 0.043*SL
C to Y	t_R	0.563	0.428 + 0.068*SL	0.404 + 0.073*SL	0.386 + 0.074*SL
	t_F	0.517	0.340 + 0.088*SL	0.332 + 0.090*SL	0.325 + 0.091*SL
	t_{PLH}	0.230	0.162 + 0.034*SL	0.167 + 0.033*SL	0.179 + 0.033*SL
	t_{PHL}	0.347	0.260 + 0.043*SL	0.266 + 0.042*SL	0.275 + 0.042*SL
D to Y	t_R	0.557	0.418 + 0.069*SL	0.401 + 0.073*SL	0.386 + 0.074*SL
	t_F	0.598	0.414 + 0.092*SL	0.408 + 0.093*SL	0.401 + 0.093*SL
	t_{PLH}	0.236	0.167 + 0.034*SL	0.172 + 0.033*SL	0.186 + 0.033*SL
	t_{PHL}	0.403	0.314 + 0.044*SL	0.319 + 0.043*SL	0.326 + 0.043*SL
E to Y	t_R	0.592	0.458 + 0.067*SL	0.434 + 0.073*SL	0.412 + 0.074*SL
	t_F	0.523	0.341 + 0.091*SL	0.334 + 0.093*SL	0.328 + 0.093*SL
	t_{PLH}	0.248	0.180 + 0.034*SL	0.185 + 0.033*SL	0.197 + 0.033*SL
	t_{PHL}	0.356	0.267 + 0.044*SL	0.273 + 0.043*SL	0.283 + 0.043*SL
F to Y	t_R	0.585	0.447 + 0.069*SL	0.430 + 0.073*SL	0.412 + 0.074*SL
	t_F	0.597	0.413 + 0.092*SL	0.408 + 0.093*SL	0.401 + 0.093*SL
	t_{PLH}	0.257	0.188 + 0.035*SL	0.195 + 0.033*SL	0.208 + 0.033*SL
	t_{PHL}	0.407	0.318 + 0.044*SL	0.323 + 0.043*SL	0.331 + 0.043*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.431	0.367 + 0.032*SL	0.350 + 0.036*SL	0.320 + 0.037*SL
	t_F	0.419	0.328 + 0.045*SL	0.322 + 0.047*SL	0.313 + 0.047*SL
	t_{PLH}	0.166	0.132 + 0.017*SL	0.134 + 0.016*SL	0.146 + 0.016*SL
	t_{PHL}	0.283	0.239 + 0.022*SL	0.241 + 0.022*SL	0.248 + 0.021*SL
B to Y	t_R	0.421	0.353 + 0.034*SL	0.343 + 0.036*SL	0.320 + 0.037*SL
	t_F	0.484	0.394 + 0.045*SL	0.388 + 0.047*SL	0.379 + 0.047*SL
	t_{PLH}	0.171	0.136 + 0.017*SL	0.140 + 0.016*SL	0.154 + 0.016*SL
	t_{PHL}	0.329	0.285 + 0.022*SL	0.287 + 0.022*SL	0.293 + 0.021*SL
C to Y	t_R	0.460	0.396 + 0.032*SL	0.379 + 0.036*SL	0.350 + 0.037*SL
	t_F	0.423	0.331 + 0.046*SL	0.325 + 0.047*SL	0.316 + 0.047*SL
	t_{PLH}	0.187	0.154 + 0.017*SL	0.155 + 0.016*SL	0.165 + 0.016*SL
	t_{PHL}	0.293	0.248 + 0.023*SL	0.251 + 0.022*SL	0.261 + 0.022*SL
D to Y	t_R	0.450	0.382 + 0.034*SL	0.371 + 0.036*SL	0.350 + 0.037*SL
	t_F	0.485	0.394 + 0.045*SL	0.389 + 0.047*SL	0.379 + 0.047*SL
	t_{PLH}	0.192	0.158 + 0.017*SL	0.160 + 0.016*SL	0.173 + 0.016*SL
	t_{PHL}	0.338	0.293 + 0.022*SL	0.296 + 0.022*SL	0.303 + 0.021*SL
E to Y	t_R	0.499	0.435 + 0.032*SL	0.418 + 0.036*SL	0.385 + 0.037*SL
	t_F	0.421	0.329 + 0.046*SL	0.324 + 0.047*SL	0.316 + 0.047*SL
	t_{PLH}	0.207	0.173 + 0.017*SL	0.176 + 0.016*SL	0.187 + 0.016*SL
	t_{PHL}	0.300	0.255 + 0.023*SL	0.258 + 0.022*SL	0.269 + 0.022*SL
F to Y	t_R	0.489	0.422 + 0.034*SL	0.410 + 0.036*SL	0.385 + 0.037*SL
	t_F	0.483	0.391 + 0.046*SL	0.388 + 0.047*SL	0.379 + 0.047*SL
	t_{PLH}	0.213	0.179 + 0.017*SL	0.181 + 0.016*SL	0.194 + 0.016*SL
	t_{PHL}	0.346	0.301 + 0.022*SL	0.304 + 0.022*SL	0.312 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA222D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.102	0.068 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.087	0.054 + 0.016*SL	0.054 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.346	0.325 + 0.011*SL	0.332 + 0.009*SL	0.334 + 0.009*SL
	t_{PHL}	0.489	0.466 + 0.011*SL	0.476 + 0.009*SL	0.483 + 0.009*SL
B to Y	t_R	0.102	0.068 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.090	0.058 + 0.016*SL	0.055 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.351	0.330 + 0.011*SL	0.337 + 0.009*SL	0.339 + 0.009*SL
	t_{PHL}	0.545	0.522 + 0.011*SL	0.532 + 0.009*SL	0.538 + 0.009*SL
C to Y	t_R	0.103	0.069 + 0.017*SL	0.061 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.088	0.057 + 0.015*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.372	0.351 + 0.011*SL	0.358 + 0.009*SL	0.359 + 0.009*SL
	t_{PHL}	0.497	0.475 + 0.011*SL	0.484 + 0.009*SL	0.491 + 0.009*SL
D to Y	t_R	0.103	0.069 + 0.017*SL	0.061 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.090	0.059 + 0.015*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.381	0.360 + 0.011*SL	0.367 + 0.009*SL	0.369 + 0.009*SL
	t_{PHL}	0.562	0.539 + 0.011*SL	0.548 + 0.009*SL	0.555 + 0.009*SL
E to Y	t_R	0.105	0.071 + 0.017*SL	0.062 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.088	0.057 + 0.015*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.394	0.373 + 0.011*SL	0.380 + 0.009*SL	0.382 + 0.009*SL
	t_{PHL}	0.501	0.479 + 0.011*SL	0.488 + 0.009*SL	0.495 + 0.009*SL
F to Y	t_R	0.105	0.071 + 0.017*SL	0.062 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.090	0.059 + 0.015*SL	0.055 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.399	0.378 + 0.011*SL	0.385 + 0.009*SL	0.387 + 0.009*SL
	t_{PHL}	0.564	0.541 + 0.011*SL	0.551 + 0.009*SL	0.558 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA222D4

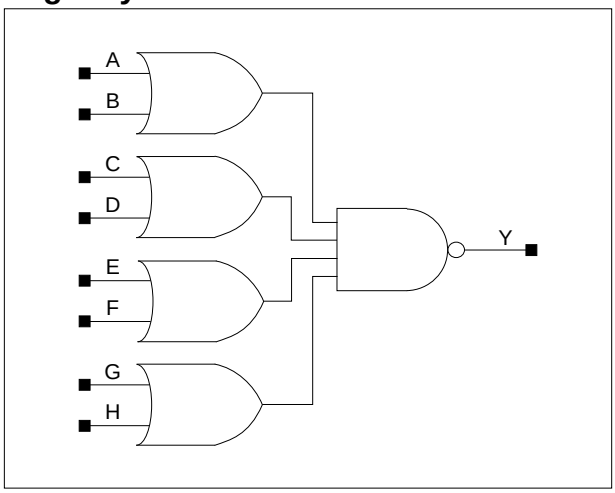
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.087 + 0.008*SL	0.083 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.089	0.073 + 0.008*SL	0.074 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.393	0.380 + 0.006*SL	0.388 + 0.005*SL	0.398 + 0.004*SL
	t_{PHL}	0.532	0.518 + 0.007*SL	0.527 + 0.005*SL	0.545 + 0.004*SL
B to Y	t_R	0.103	0.086 + 0.008*SL	0.082 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.091	0.075 + 0.008*SL	0.076 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.398	0.385 + 0.006*SL	0.393 + 0.005*SL	0.403 + 0.004*SL
	t_{PHL}	0.587	0.574 + 0.007*SL	0.583 + 0.005*SL	0.601 + 0.004*SL
C to Y	t_R	0.104	0.087 + 0.008*SL	0.083 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.089	0.072 + 0.008*SL	0.074 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.418	0.406 + 0.006*SL	0.413 + 0.005*SL	0.424 + 0.004*SL
	t_{PHL}	0.540	0.526 + 0.007*SL	0.535 + 0.005*SL	0.553 + 0.004*SL
D to Y	t_R	0.104	0.087 + 0.008*SL	0.083 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.091	0.074 + 0.008*SL	0.076 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.428	0.415 + 0.006*SL	0.423 + 0.005*SL	0.434 + 0.004*SL
	t_{PHL}	0.604	0.591 + 0.007*SL	0.600 + 0.005*SL	0.618 + 0.004*SL
E to Y	t_R	0.105	0.089 + 0.008*SL	0.085 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.089	0.072 + 0.008*SL	0.074 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.442	0.429 + 0.006*SL	0.437 + 0.005*SL	0.448 + 0.004*SL
	t_{PHL}	0.544	0.530 + 0.007*SL	0.539 + 0.005*SL	0.557 + 0.004*SL
F to Y	t_R	0.105	0.089 + 0.008*SL	0.085 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.091	0.075 + 0.008*SL	0.076 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.447	0.434 + 0.007*SL	0.442 + 0.005*SL	0.453 + 0.004*SL
	t_{PHL}	0.607	0.593 + 0.007*SL	0.602 + 0.005*SL	0.620 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OA2222/OA2222D2/OA2222D4

Four 2-ORs into 4-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	x	x	x	x	x	x	1
x	x	0	0	x	x	x	x	1
x	x	x	x	0	0	x	x	1
x	x	x	x	x	x	0	0	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
OA2222								*OA2222*
A	B	C	D	E	F	G	H	
0.9	1.0	0.9	1.0	0.9	1.0	1.0	1.0	3.33
OA2222D2								*OA2222D2*
A	B	C	D	E	F	G	H	
0.9	1.0	0.9	1.0	0.9	1.0	1.0	1.0	4.00
OA2222D4								*OA2222D4*
A	B	C	D	E	F	G	H	
0.9	1.0	0.9	1.0	0.9	1.0	1.0	1.0	4.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA2222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.595	0.459 + 0.068*SL	0.438 + 0.073*SL	0.419 + 0.074*SL
	t_F	0.561	0.371 + 0.095*SL	0.363 + 0.097*SL	0.361 + 0.097*SL
	t_{PLH}	0.221	0.152 + 0.035*SL	0.158 + 0.033*SL	0.170 + 0.033*SL
	t_{PHL}	0.334	0.244 + 0.045*SL	0.248 + 0.044*SL	0.254 + 0.044*SL
B to Y	t_R	0.589	0.450 + 0.070*SL	0.435 + 0.073*SL	0.419 + 0.074*SL
	t_F	0.629	0.439 + 0.095*SL	0.432 + 0.097*SL	0.430 + 0.097*SL
	t_{PLH}	0.227	0.157 + 0.035*SL	0.164 + 0.033*SL	0.178 + 0.033*SL
	t_{PHL}	0.380	0.291 + 0.045*SL	0.294 + 0.044*SL	0.298 + 0.044*SL
C to Y	t_R	0.636	0.500 + 0.068*SL	0.478 + 0.073*SL	0.461 + 0.074*SL
	t_F	0.568	0.377 + 0.096*SL	0.370 + 0.097*SL	0.364 + 0.098*SL
	t_{PLH}	0.250	0.182 + 0.034*SL	0.187 + 0.033*SL	0.198 + 0.033*SL
	t_{PHL}	0.357	0.267 + 0.045*SL	0.271 + 0.044*SL	0.280 + 0.044*SL
D to Y	t_R	0.630	0.490 + 0.070*SL	0.476 + 0.074*SL	0.461 + 0.074*SL
	t_F	0.633	0.443 + 0.095*SL	0.437 + 0.097*SL	0.430 + 0.097*SL
	t_{PLH}	0.256	0.187 + 0.035*SL	0.193 + 0.033*SL	0.206 + 0.033*SL
	t_{PHL}	0.403	0.313 + 0.045*SL	0.317 + 0.044*SL	0.323 + 0.044*SL
E to Y	t_R	0.722	0.587 + 0.067*SL	0.564 + 0.073*SL	0.541 + 0.074*SL
	t_F	0.562	0.369 + 0.096*SL	0.364 + 0.098*SL	0.358 + 0.098*SL
	t_{PLH}	0.297	0.228 + 0.034*SL	0.234 + 0.033*SL	0.247 + 0.033*SL
	t_{PHL}	0.395	0.303 + 0.046*SL	0.309 + 0.044*SL	0.319 + 0.044*SL
F to Y	t_R	0.716	0.577 + 0.069*SL	0.562 + 0.073*SL	0.541 + 0.074*SL
	t_F	0.632	0.441 + 0.096*SL	0.436 + 0.097*SL	0.430 + 0.097*SL
	t_{PLH}	0.307	0.238 + 0.035*SL	0.244 + 0.033*SL	0.258 + 0.033*SL
	t_{PHL}	0.444	0.354 + 0.045*SL	0.359 + 0.044*SL	0.367 + 0.044*SL
G to Y	t_R	0.684	0.549 + 0.068*SL	0.526 + 0.073*SL	0.506 + 0.074*SL
	t_F	0.711	0.496 + 0.108*SL	0.492 + 0.109*SL	0.487 + 0.109*SL
	t_{PLH}	0.279	0.211 + 0.034*SL	0.216 + 0.033*SL	0.227 + 0.033*SL
	t_{PHL}	0.484	0.383 + 0.050*SL	0.389 + 0.049*SL	0.400 + 0.049*SL
H to Y	t_R	0.678	0.539 + 0.070*SL	0.524 + 0.073*SL	0.506 + 0.074*SL
	t_F	0.808	0.587 + 0.110*SL	0.583 + 0.111*SL	0.578 + 0.112*SL
	t_{PLH}	0.285	0.216 + 0.034*SL	0.221 + 0.033*SL	0.234 + 0.033*SL
	t_{PHL}	0.550	0.448 + 0.051*SL	0.452 + 0.050*SL	0.460 + 0.050*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA2222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.105	0.071 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.089	0.059 + 0.015*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.374	0.353 + 0.011*SL	0.360 + 0.009*SL	0.362 + 0.009*SL
	t_{PHL}	0.499	0.476 + 0.011*SL	0.486 + 0.009*SL	0.493 + 0.009*SL
B to Y	t_R	0.106	0.072 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.090	0.058 + 0.016*SL	0.057 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.378	0.357 + 0.011*SL	0.364 + 0.009*SL	0.366 + 0.009*SL
	t_{PHL}	0.557	0.534 + 0.011*SL	0.544 + 0.009*SL	0.551 + 0.009*SL
C to Y	t_R	0.107	0.074 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.090	0.059 + 0.015*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.405	0.383 + 0.011*SL	0.391 + 0.009*SL	0.392 + 0.009*SL
	t_{PHL}	0.521	0.498 + 0.011*SL	0.508 + 0.009*SL	0.515 + 0.009*SL
D to Y	t_R	0.107	0.074 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.091	0.060 + 0.015*SL	0.056 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.410	0.388 + 0.011*SL	0.396 + 0.009*SL	0.398 + 0.009*SL
	t_{PHL}	0.581	0.558 + 0.011*SL	0.568 + 0.009*SL	0.575 + 0.009*SL
E to Y	t_R	0.109	0.075 + 0.017*SL	0.066 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.089	0.057 + 0.016*SL	0.055 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.428	0.406 + 0.011*SL	0.414 + 0.009*SL	0.416 + 0.009*SL
	t_{PHL}	0.534	0.511 + 0.011*SL	0.521 + 0.009*SL	0.528 + 0.009*SL
F to Y	t_R	0.109	0.075 + 0.017*SL	0.066 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.091	0.060 + 0.016*SL	0.056 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.434	0.412 + 0.011*SL	0.420 + 0.009*SL	0.421 + 0.009*SL
	t_{PHL}	0.591	0.568 + 0.011*SL	0.578 + 0.009*SL	0.585 + 0.009*SL
G to Y	t_R	0.110	0.077 + 0.017*SL	0.067 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.094	0.064 + 0.015*SL	0.058 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.446	0.424 + 0.011*SL	0.432 + 0.009*SL	0.434 + 0.009*SL
	t_{PHL}	0.669	0.646 + 0.012*SL	0.657 + 0.009*SL	0.663 + 0.009*SL
H to Y	t_R	0.110	0.076 + 0.017*SL	0.067 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.096	0.065 + 0.016*SL	0.062 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.455	0.433 + 0.011*SL	0.441 + 0.009*SL	0.443 + 0.009*SL
	t_{PHL}	0.748	0.725 + 0.012*SL	0.736 + 0.009*SL	0.742 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA2222D4

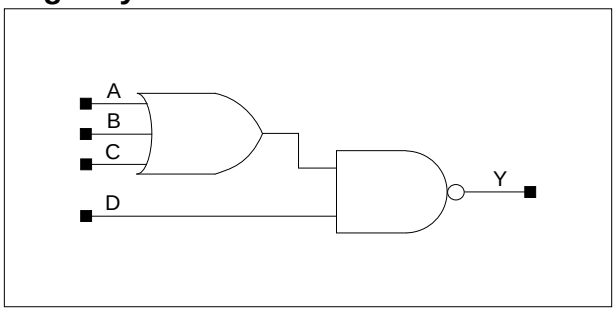
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.106	0.089 + 0.008*SL	0.086 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.091	0.074 + 0.008*SL	0.076 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.420	0.407 + 0.007*SL	0.415 + 0.005*SL	0.426 + 0.004*SL
	t_{PHL}	0.542	0.528 + 0.007*SL	0.537 + 0.005*SL	0.555 + 0.004*SL
B to Y	t_R	0.106	0.090 + 0.008*SL	0.086 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.093	0.076 + 0.008*SL	0.078 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.425	0.412 + 0.006*SL	0.420 + 0.005*SL	0.431 + 0.004*SL
	t_{PHL}	0.601	0.587 + 0.007*SL	0.596 + 0.005*SL	0.614 + 0.004*SL
C to Y	t_R	0.109	0.092 + 0.008*SL	0.088 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.091	0.075 + 0.008*SL	0.077 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.452	0.439 + 0.007*SL	0.447 + 0.005*SL	0.458 + 0.004*SL
	t_{PHL}	0.564	0.550 + 0.007*SL	0.559 + 0.005*SL	0.577 + 0.004*SL
D to Y	t_R	0.108	0.093 + 0.008*SL	0.087 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.093	0.076 + 0.008*SL	0.078 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.457	0.444 + 0.007*SL	0.453 + 0.005*SL	0.463 + 0.004*SL
	t_{PHL}	0.625	0.611 + 0.007*SL	0.620 + 0.005*SL	0.638 + 0.004*SL
E to Y	t_R	0.110	0.094 + 0.008*SL	0.089 + 0.009*SL	0.054 + 0.010*SL
	t_F	0.092	0.075 + 0.008*SL	0.076 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.474	0.461 + 0.007*SL	0.469 + 0.005*SL	0.480 + 0.004*SL
	t_{PHL}	0.572	0.558 + 0.007*SL	0.567 + 0.005*SL	0.585 + 0.004*SL
F to Y	t_R	0.109	0.094 + 0.008*SL	0.089 + 0.009*SL	0.054 + 0.010*SL
	t_F	0.093	0.077 + 0.008*SL	0.077 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.480	0.467 + 0.007*SL	0.475 + 0.005*SL	0.485 + 0.004*SL
	t_{PHL}	0.634	0.620 + 0.007*SL	0.629 + 0.005*SL	0.647 + 0.004*SL
G to Y	t_R	0.111	0.095 + 0.008*SL	0.091 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.096	0.079 + 0.008*SL	0.081 + 0.008*SL	0.051 + 0.008*SL
	t_{PLH}	0.493	0.479 + 0.007*SL	0.488 + 0.005*SL	0.499 + 0.004*SL
	t_{PHL}	0.712	0.698 + 0.007*SL	0.708 + 0.005*SL	0.726 + 0.004*SL
H to Y	t_R	0.111	0.095 + 0.008*SL	0.091 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.098	0.081 + 0.008*SL	0.083 + 0.008*SL	0.052 + 0.008*SL
	t_{PLH}	0.501	0.488 + 0.007*SL	0.497 + 0.005*SL	0.507 + 0.004*SL
	t_{PHL}	0.793	0.779 + 0.007*SL	0.788 + 0.005*SL	0.806 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OA31/OA31D2/OA31D4

3-OR into 2-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	x	1
x	x	x	0	1
Other States				0

Cell Data

Input Load (SL)												Gate Count		
OA31				*OA31D2*				*OA31D4*				*OA31*	*OA31D2*	*OA31D4*
A	B	C	D	A	B	C	D	A	B	C	D			
0.9	0.9	0.9	0.9	1.9	1.8	1.8	1.9	0.9	0.9	0.9	1.0	1.67	3.00	3.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA31

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.451	0.242 + 0.105*SL	0.222 + 0.110*SL	0.220 + 0.110*SL
	t_F	0.249	0.127 + 0.061*SL	0.108 + 0.066*SL	0.092 + 0.066*SL
	t_{PLH}	0.213	0.119 + 0.047*SL	0.114 + 0.048*SL	0.112 + 0.048*SL
	t_{PHL}	0.162	0.097 + 0.032*SL	0.100 + 0.032*SL	0.100 + 0.032*SL
B to Y	t_R	0.457	0.246 + 0.106*SL	0.231 + 0.109*SL	0.220 + 0.110*SL
	t_F	0.308	0.185 + 0.061*SL	0.165 + 0.067*SL	0.147 + 0.067*SL
	t_{PLH}	0.248	0.151 + 0.049*SL	0.152 + 0.048*SL	0.155 + 0.048*SL
	t_{PHL}	0.201	0.136 + 0.033*SL	0.138 + 0.032*SL	0.140 + 0.032*SL
C to Y	t_R	0.453	0.241 + 0.106*SL	0.227 + 0.109*SL	0.220 + 0.110*SL
	t_F	0.370	0.246 + 0.062*SL	0.229 + 0.066*SL	0.201 + 0.067*SL
	t_{PLH}	0.263	0.165 + 0.049*SL	0.168 + 0.048*SL	0.172 + 0.048*SL
	t_{PHL}	0.222	0.153 + 0.035*SL	0.161 + 0.032*SL	0.173 + 0.032*SL
D to Y	t_R	0.248	0.184 + 0.032*SL	0.161 + 0.038*SL	0.124 + 0.039*SL
	t_F	0.353	0.222 + 0.066*SL	0.218 + 0.067*SL	0.201 + 0.067*SL
	t_{PLH}	0.137	0.099 + 0.019*SL	0.105 + 0.017*SL	0.106 + 0.017*SL
	t_{PHL}	0.222	0.152 + 0.035*SL	0.161 + 0.033*SL	0.175 + 0.032*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA31D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.360	0.258 + 0.051*SL	0.244 + 0.055*SL	0.234 + 0.055*SL
	t_F	0.194	0.136 + 0.029*SL	0.123 + 0.033*SL	0.100 + 0.033*SL
	t_{PLH}	0.172	0.126 + 0.023*SL	0.122 + 0.024*SL	0.118 + 0.024*SL
	t_{PHL}	0.134	0.100 + 0.017*SL	0.105 + 0.016*SL	0.105 + 0.016*SL
B to Y	t_R	0.366	0.262 + 0.052*SL	0.251 + 0.055*SL	0.233 + 0.055*SL
	t_F	0.251	0.191 + 0.030*SL	0.178 + 0.033*SL	0.152 + 0.033*SL
	t_{PLH}	0.201	0.152 + 0.025*SL	0.154 + 0.024*SL	0.156 + 0.024*SL
	t_{PHL}	0.171	0.138 + 0.016*SL	0.140 + 0.016*SL	0.142 + 0.016*SL
C to Y	t_R	0.361	0.256 + 0.052*SL	0.246 + 0.055*SL	0.233 + 0.055*SL
	t_F	0.318	0.257 + 0.031*SL	0.247 + 0.033*SL	0.213 + 0.033*SL
	t_{PLH}	0.219	0.170 + 0.025*SL	0.173 + 0.024*SL	0.177 + 0.024*SL
	t_{PHL}	0.192	0.157 + 0.018*SL	0.162 + 0.016*SL	0.178 + 0.016*SL
D to Y	t_R	0.221	0.191 + 0.015*SL	0.177 + 0.019*SL	0.130 + 0.019*SL
	t_F	0.298	0.232 + 0.033*SL	0.231 + 0.033*SL	0.213 + 0.033*SL
	t_{PLH}	0.122	0.102 + 0.010*SL	0.108 + 0.009*SL	0.110 + 0.009*SL
	t_{PHL}	0.196	0.160 + 0.018*SL	0.166 + 0.016*SL	0.185 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OA31D4

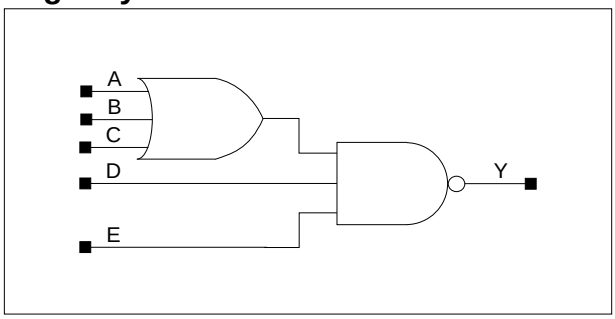
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.099	0.082 + 0.009*SL	0.079 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.080	0.063 + 0.009*SL	0.065 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.374	0.361 + 0.006*SL	0.368 + 0.005*SL	0.378 + 0.004*SL
	t_{PHL}	0.317	0.304 + 0.007*SL	0.312 + 0.005*SL	0.329 + 0.004*SL
B to Y	t_R	0.100	0.083 + 0.008*SL	0.079 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.083	0.066 + 0.008*SL	0.067 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.411	0.399 + 0.006*SL	0.406 + 0.005*SL	0.416 + 0.004*SL
	t_{PHL}	0.369	0.356 + 0.007*SL	0.364 + 0.005*SL	0.381 + 0.004*SL
C to Y	t_R	0.100	0.083 + 0.008*SL	0.080 + 0.009*SL	0.049 + 0.010*SL
	t_F	0.084	0.068 + 0.008*SL	0.069 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.426	0.413 + 0.006*SL	0.420 + 0.005*SL	0.431 + 0.004*SL
	t_{PHL}	0.400	0.387 + 0.007*SL	0.395 + 0.005*SL	0.412 + 0.004*SL
D to Y	t_R	0.096	0.079 + 0.008*SL	0.075 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.085	0.069 + 0.008*SL	0.069 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.302	0.289 + 0.006*SL	0.296 + 0.005*SL	0.306 + 0.004*SL
	t_{PHL}	0.400	0.387 + 0.007*SL	0.395 + 0.005*SL	0.413 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OA311/OA311D2/OA311D4

3-OR into 3-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)														
OA311					*OA311D2*					*OA311D4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.9	0.9	0.9	0.9	0.9	1.8	1.8	1.8	1.9	1.9	0.9	0.9	0.9	0.9	0.9

Gate Count		
OA311	*OA311D2*	*OA311D4*
2.00	3.33	3.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA311

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.510	0.299 + 0.106*SL	0.283 + 0.110*SL	0.281 + 0.110*SL
	t_F	0.382	0.206 + 0.088*SL	0.193 + 0.091*SL	0.188 + 0.091*SL
	t_{PLH}	0.237	0.142 + 0.048*SL	0.139 + 0.048*SL	0.138 + 0.048*SL
	t_{PHL}	0.224	0.140 + 0.042*SL	0.140 + 0.042*SL	0.141 + 0.042*SL
B to Y	t_R	0.516	0.304 + 0.106*SL	0.291 + 0.109*SL	0.281 + 0.110*SL
	t_F	0.456	0.280 + 0.088*SL	0.265 + 0.092*SL	0.258 + 0.092*SL
	t_{PLH}	0.272	0.175 + 0.049*SL	0.176 + 0.048*SL	0.178 + 0.048*SL
	t_{PHL}	0.274	0.188 + 0.043*SL	0.190 + 0.042*SL	0.192 + 0.042*SL
C to Y	t_R	0.512	0.298 + 0.107*SL	0.287 + 0.109*SL	0.281 + 0.110*SL
	t_F	0.545	0.371 + 0.087*SL	0.353 + 0.092*SL	0.333 + 0.092*SL
	t_{PLH}	0.289	0.191 + 0.049*SL	0.193 + 0.048*SL	0.196 + 0.048*SL
	t_{PHL}	0.308	0.219 + 0.045*SL	0.227 + 0.043*SL	0.238 + 0.042*SL
D to Y	t_R	0.265	0.199 + 0.033*SL	0.180 + 0.038*SL	0.145 + 0.039*SL
	t_F	0.538	0.359 + 0.089*SL	0.350 + 0.092*SL	0.333 + 0.092*SL
	t_{PLH}	0.147	0.110 + 0.019*SL	0.114 + 0.018*SL	0.117 + 0.017*SL
	t_{PHL}	0.324	0.233 + 0.045*SL	0.243 + 0.043*SL	0.258 + 0.042*SL
E to Y	t_R	0.276	0.211 + 0.033*SL	0.191 + 0.038*SL	0.155 + 0.039*SL
	t_F	0.537	0.357 + 0.090*SL	0.349 + 0.092*SL	0.333 + 0.092*SL
	t_{PLH}	0.152	0.116 + 0.018*SL	0.118 + 0.018*SL	0.121 + 0.017*SL
	t_{PHL}	0.317	0.227 + 0.045*SL	0.237 + 0.043*SL	0.252 + 0.042*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA311D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.399	0.295 + 0.052*SL	0.284 + 0.055*SL	0.275 + 0.055*SL
	t_F	0.288	0.202 + 0.043*SL	0.193 + 0.045*SL	0.182 + 0.045*SL
	t_{PLH}	0.187	0.140 + 0.023*SL	0.137 + 0.024*SL	0.135 + 0.024*SL
	t_{PHL}	0.177	0.136 + 0.021*SL	0.136 + 0.021*SL	0.137 + 0.021*SL
B to Y	t_R	0.404	0.300 + 0.052*SL	0.291 + 0.055*SL	0.275 + 0.055*SL
	t_F	0.363	0.277 + 0.043*SL	0.266 + 0.046*SL	0.252 + 0.046*SL
	t_{PLH}	0.220	0.171 + 0.025*SL	0.172 + 0.024*SL	0.175 + 0.024*SL
	t_{PHL}	0.226	0.183 + 0.022*SL	0.185 + 0.021*SL	0.188 + 0.021*SL
C to Y	t_R	0.400	0.295 + 0.053*SL	0.286 + 0.055*SL	0.275 + 0.055*SL
	t_F	0.452	0.367 + 0.043*SL	0.356 + 0.046*SL	0.327 + 0.046*SL
	t_{PLH}	0.236	0.187 + 0.025*SL	0.189 + 0.024*SL	0.193 + 0.024*SL
	t_{PHL}	0.258	0.213 + 0.023*SL	0.219 + 0.021*SL	0.234 + 0.021*SL
D to Y	t_R	0.235	0.204 + 0.016*SL	0.191 + 0.019*SL	0.146 + 0.019*SL
	t_F	0.442	0.353 + 0.044*SL	0.349 + 0.046*SL	0.327 + 0.046*SL
	t_{PLH}	0.128	0.108 + 0.010*SL	0.114 + 0.009*SL	0.117 + 0.009*SL
	t_{PHL}	0.278	0.232 + 0.023*SL	0.238 + 0.021*SL	0.258 + 0.021*SL
E to Y	t_R	0.247	0.216 + 0.015*SL	0.203 + 0.019*SL	0.156 + 0.020*SL
	t_F	0.441	0.351 + 0.045*SL	0.348 + 0.046*SL	0.327 + 0.046*SL
	t_{PLH}	0.134	0.114 + 0.010*SL	0.118 + 0.009*SL	0.122 + 0.009*SL
	t_{PHL}	0.269	0.223 + 0.023*SL	0.230 + 0.021*SL	0.250 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA311D4

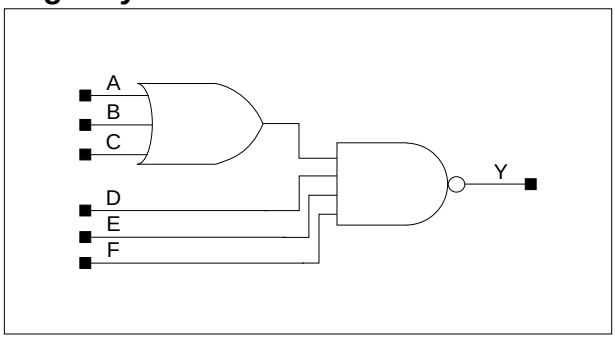
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.101	0.085 + 0.008*SL	0.081 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.087	0.071 + 0.008*SL	0.071 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.410	0.398 + 0.006*SL	0.405 + 0.005*SL	0.416 + 0.004*SL
	t_{PHL}	0.408	0.394 + 0.007*SL	0.403 + 0.005*SL	0.420 + 0.004*SL
B to Y	t_R	0.102	0.085 + 0.008*SL	0.081 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.089	0.072 + 0.008*SL	0.074 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.444	0.431 + 0.006*SL	0.439 + 0.005*SL	0.449 + 0.004*SL
	t_{PHL}	0.469	0.455 + 0.007*SL	0.464 + 0.005*SL	0.482 + 0.004*SL
C to Y	t_R	0.102	0.085 + 0.008*SL	0.081 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.091	0.075 + 0.008*SL	0.075 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.460	0.447 + 0.006*SL	0.454 + 0.005*SL	0.465 + 0.004*SL
	t_{PHL}	0.515	0.501 + 0.007*SL	0.510 + 0.005*SL	0.528 + 0.004*SL
D to Y	t_R	0.096	0.079 + 0.009*SL	0.077 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.091	0.075 + 0.008*SL	0.076 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.317	0.305 + 0.006*SL	0.312 + 0.005*SL	0.322 + 0.004*SL
	t_{PHL}	0.529	0.515 + 0.007*SL	0.524 + 0.005*SL	0.542 + 0.004*SL
E to Y	t_R	0.096	0.078 + 0.009*SL	0.076 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.091	0.075 + 0.008*SL	0.076 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.324	0.311 + 0.006*SL	0.318 + 0.005*SL	0.328 + 0.004*SL
	t_{PHL}	0.523	0.509 + 0.007*SL	0.518 + 0.005*SL	0.537 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

OA3111/OA3111D2

3-OR into 4-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	x	x	x	1
x	x	x	0	x	x	1
x	x	x	x	0	x	1
x	x	x	x	x	0	1
Other States						0

Cell Data

Input Load (SL)												Gate Count	
OA3111						*OA3111D2*						*OA3111*	*OA3111D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.9	0.9	0.9	0.9	0.9	0.9	1.9	1.9	1.9	2.0	2.0	1.9	2.33	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA3111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.580	0.369 + 0.105*SL	0.357 + 0.108*SL	0.356 + 0.108*SL
	t_F	0.572	0.340 + 0.116*SL	0.333 + 0.118*SL	0.335 + 0.118*SL
	t_{PLH}	0.264	0.169 + 0.047*SL	0.168 + 0.048*SL	0.167 + 0.048*SL
	t_{PHL}	0.304	0.197 + 0.053*SL	0.198 + 0.053*SL	0.201 + 0.053*SL
B to Y	t_R	0.586	0.375 + 0.106*SL	0.365 + 0.108*SL	0.356 + 0.108*SL
	t_F	0.664	0.432 + 0.116*SL	0.424 + 0.118*SL	0.423 + 0.118*SL
	t_{PLH}	0.302	0.206 + 0.048*SL	0.208 + 0.048*SL	0.209 + 0.048*SL
	t_{PHL}	0.369	0.262 + 0.053*SL	0.264 + 0.053*SL	0.267 + 0.053*SL
C to Y	t_R	0.583	0.370 + 0.106*SL	0.361 + 0.108*SL	0.356 + 0.108*SL
	t_F	0.755	0.531 + 0.112*SL	0.517 + 0.116*SL	0.504 + 0.116*SL
	t_{PLH}	0.316	0.220 + 0.048*SL	0.222 + 0.048*SL	0.224 + 0.048*SL
	t_{PHL}	0.408	0.300 + 0.054*SL	0.307 + 0.052*SL	0.317 + 0.052*SL
D to Y	t_R	0.289	0.223 + 0.033*SL	0.205 + 0.037*SL	0.173 + 0.038*SL
	t_F	0.755	0.529 + 0.113*SL	0.518 + 0.116*SL	0.504 + 0.116*SL
	t_{PLH}	0.158	0.122 + 0.018*SL	0.124 + 0.017*SL	0.128 + 0.017*SL
	t_{PHL}	0.440	0.331 + 0.055*SL	0.339 + 0.053*SL	0.354 + 0.052*SL
E to Y	t_R	0.302	0.236 + 0.033*SL	0.218 + 0.038*SL	0.185 + 0.039*SL
	t_F	0.755	0.529 + 0.113*SL	0.518 + 0.116*SL	0.504 + 0.116*SL
	t_{PLH}	0.165	0.129 + 0.018*SL	0.130 + 0.018*SL	0.134 + 0.017*SL
	t_{PHL}	0.441	0.332 + 0.055*SL	0.340 + 0.053*SL	0.355 + 0.052*SL
F to Y	t_R	0.314	0.247 + 0.033*SL	0.229 + 0.038*SL	0.194 + 0.039*SL
	t_F	0.754	0.529 + 0.113*SL	0.518 + 0.116*SL	0.504 + 0.116*SL
	t_{PLH}	0.169	0.133 + 0.018*SL	0.135 + 0.018*SL	0.139 + 0.017*SL
	t_{PHL}	0.440	0.330 + 0.055*SL	0.339 + 0.053*SL	0.354 + 0.052*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

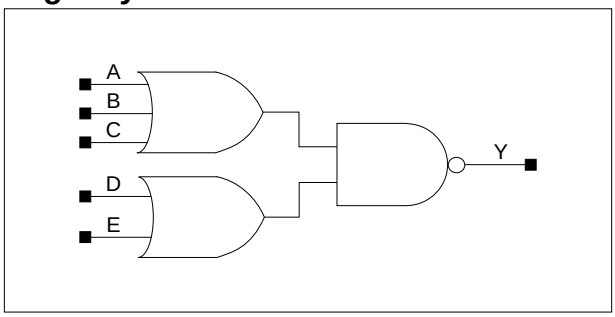
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA3111D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.450	0.346 + 0.052*SL	0.336 + 0.055*SL	0.330 + 0.055*SL
	t_F	0.383	0.285 + 0.049*SL	0.279 + 0.051*SL	0.274 + 0.051*SL
	t_{PLH}	0.210	0.163 + 0.024*SL	0.161 + 0.024*SL	0.160 + 0.024*SL
	t_{PHL}	0.206	0.160 + 0.023*SL	0.160 + 0.023*SL	0.162 + 0.023*SL
B to Y	t_R	0.456	0.351 + 0.053*SL	0.343 + 0.054*SL	0.330 + 0.055*SL
	t_F	0.465	0.367 + 0.049*SL	0.358 + 0.051*SL	0.351 + 0.051*SL
	t_{PLH}	0.244	0.196 + 0.024*SL	0.197 + 0.024*SL	0.200 + 0.024*SL
	t_{PHL}	0.260	0.213 + 0.023*SL	0.215 + 0.023*SL	0.218 + 0.023*SL
C to Y	t_R	0.452	0.346 + 0.053*SL	0.339 + 0.054*SL	0.330 + 0.055*SL
	t_F	0.563	0.467 + 0.048*SL	0.455 + 0.051*SL	0.432 + 0.051*SL
	t_{PLH}	0.260	0.211 + 0.024*SL	0.212 + 0.024*SL	0.217 + 0.024*SL
	t_{PHL}	0.298	0.249 + 0.024*SL	0.254 + 0.023*SL	0.267 + 0.023*SL
D to Y	t_R	0.208	0.175 + 0.016*SL	0.165 + 0.019*SL	0.129 + 0.019*SL
	t_F	0.559	0.460 + 0.049*SL	0.454 + 0.051*SL	0.432 + 0.051*SL
	t_{PLH}	0.143	0.124 + 0.009*SL	0.127 + 0.009*SL	0.125 + 0.009*SL
	t_{PHL}	0.333	0.284 + 0.025*SL	0.289 + 0.023*SL	0.308 + 0.023*SL
E to Y	t_R	0.221	0.189 + 0.016*SL	0.178 + 0.019*SL	0.141 + 0.019*SL
	t_F	0.559	0.460 + 0.050*SL	0.454 + 0.051*SL	0.432 + 0.051*SL
	t_{PLH}	0.149	0.131 + 0.009*SL	0.133 + 0.009*SL	0.132 + 0.009*SL
	t_{PHL}	0.334	0.284 + 0.025*SL	0.290 + 0.023*SL	0.310 + 0.023*SL
F to Y	t_R	0.234	0.202 + 0.016*SL	0.192 + 0.019*SL	0.152 + 0.019*SL
	t_F	0.558	0.458 + 0.050*SL	0.453 + 0.051*SL	0.432 + 0.051*SL
	t_{PLH}	0.155	0.136 + 0.009*SL	0.138 + 0.009*SL	0.138 + 0.009*SL
	t_{PHL}	0.331	0.281 + 0.025*SL	0.287 + 0.023*SL	0.307 + 0.023*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	x	x	1
x	x	x	0	0	1
Other States					0

Cell Data

Input Load (SL)														
OA32					*OA32D2*					*OA32D4*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.9	0.9	0.9	0.9	0.9	1.9	1.9	1.8	1.9	1.8	0.9	0.9	0.9	0.9	0.9

Gate Count		
OA32	*OA32D2*	*OA32D4*
2.33	4.00	4.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA32

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.592	0.386 + 0.103*SL	0.365 + 0.108*SL	0.363 + 0.108*SL
	t_F	0.307	0.181 + 0.063*SL	0.166 + 0.067*SL	0.153 + 0.067*SL
	t_{PLH}	0.227	0.130 + 0.048*SL	0.132 + 0.048*SL	0.137 + 0.048*SL
	t_{PHL}	0.209	0.143 + 0.033*SL	0.146 + 0.032*SL	0.149 + 0.032*SL
B to Y	t_R	0.600	0.392 + 0.104*SL	0.376 + 0.108*SL	0.363 + 0.108*SL
	t_F	0.370	0.244 + 0.063*SL	0.229 + 0.067*SL	0.215 + 0.067*SL
	t_{PLH}	0.271	0.171 + 0.050*SL	0.179 + 0.048*SL	0.189 + 0.048*SL
	t_{PHL}	0.252	0.186 + 0.033*SL	0.190 + 0.032*SL	0.195 + 0.032*SL
C to Y	t_R	0.596	0.387 + 0.105*SL	0.372 + 0.108*SL	0.363 + 0.108*SL
	t_F	0.436	0.309 + 0.064*SL	0.298 + 0.066*SL	0.277 + 0.067*SL
	t_{PLH}	0.290	0.190 + 0.050*SL	0.198 + 0.048*SL	0.209 + 0.048*SL
	t_{PHL}	0.278	0.208 + 0.035*SL	0.217 + 0.033*SL	0.231 + 0.032*SL
D to Y	t_R	0.459	0.324 + 0.068*SL	0.302 + 0.073*SL	0.285 + 0.074*SL
	t_F	0.377	0.245 + 0.066*SL	0.242 + 0.067*SL	0.226 + 0.067*SL
	t_{PLH}	0.216	0.151 + 0.033*SL	0.151 + 0.033*SL	0.159 + 0.032*SL
	t_{PHL}	0.245	0.174 + 0.036*SL	0.186 + 0.033*SL	0.204 + 0.032*SL
E to Y	t_R	0.454	0.315 + 0.069*SL	0.300 + 0.073*SL	0.285 + 0.074*SL
	t_F	0.427	0.295 + 0.066*SL	0.292 + 0.067*SL	0.277 + 0.067*SL
	t_{PLH}	0.221	0.155 + 0.033*SL	0.157 + 0.033*SL	0.167 + 0.032*SL
	t_{PHL}	0.283	0.213 + 0.035*SL	0.222 + 0.033*SL	0.238 + 0.032*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA32D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.501	0.401 + 0.050*SL	0.385 + 0.054*SL	0.375 + 0.054*SL
	t_F	0.248	0.185 + 0.031*SL	0.177 + 0.033*SL	0.159 + 0.034*SL
	t_{PLH}	0.182	0.135 + 0.024*SL	0.133 + 0.024*SL	0.140 + 0.024*SL
	t_{PHL}	0.181	0.148 + 0.017*SL	0.149 + 0.016*SL	0.154 + 0.016*SL
B to Y	t_R	0.508	0.405 + 0.051*SL	0.395 + 0.054*SL	0.375 + 0.054*SL
	t_F	0.311	0.250 + 0.031*SL	0.240 + 0.033*SL	0.220 + 0.034*SL
	t_{PLH}	0.226	0.175 + 0.025*SL	0.179 + 0.024*SL	0.193 + 0.024*SL
	t_{PHL}	0.223	0.190 + 0.017*SL	0.192 + 0.016*SL	0.199 + 0.016*SL
C to Y	t_R	0.505	0.402 + 0.051*SL	0.391 + 0.054*SL	0.375 + 0.054*SL
	t_F	0.379	0.316 + 0.032*SL	0.310 + 0.033*SL	0.285 + 0.034*SL
	t_{PLH}	0.245	0.193 + 0.026*SL	0.199 + 0.024*SL	0.215 + 0.024*SL
	t_{PHL}	0.247	0.212 + 0.018*SL	0.218 + 0.016*SL	0.236 + 0.016*SL
D to Y	t_R	0.398	0.333 + 0.033*SL	0.318 + 0.036*SL	0.292 + 0.037*SL
	t_F	0.318	0.253 + 0.033*SL	0.251 + 0.033*SL	0.234 + 0.034*SL
	t_{PLH}	0.186	0.153 + 0.016*SL	0.153 + 0.016*SL	0.161 + 0.016*SL
	t_{PHL}	0.215	0.178 + 0.018*SL	0.186 + 0.016*SL	0.209 + 0.016*SL
E to Y	t_R	0.391	0.322 + 0.034*SL	0.313 + 0.036*SL	0.292 + 0.037*SL
	t_F	0.368	0.302 + 0.033*SL	0.301 + 0.033*SL	0.284 + 0.034*SL
	t_{PLH}	0.190	0.157 + 0.017*SL	0.158 + 0.016*SL	0.169 + 0.016*SL
	t_{PHL}	0.252	0.217 + 0.018*SL	0.223 + 0.016*SL	0.242 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

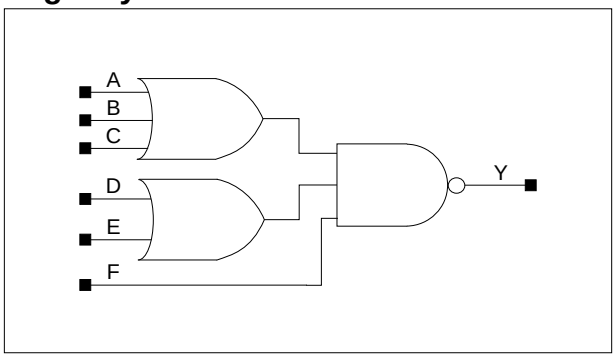
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA32D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.105	0.089 + 0.008*SL	0.085 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.082	0.065 + 0.008*SL	0.066 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.406	0.393 + 0.007*SL	0.401 + 0.005*SL	0.412 + 0.004*SL
	t_{PHL}	0.373	0.359 + 0.007*SL	0.367 + 0.005*SL	0.385 + 0.004*SL
B to Y	t_R	0.106	0.089 + 0.008*SL	0.085 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.083	0.066 + 0.008*SL	0.068 + 0.008*SL	0.044 + 0.008*SL
	t_{PLH}	0.450	0.437 + 0.007*SL	0.445 + 0.005*SL	0.455 + 0.004*SL
	t_{PHL}	0.428	0.414 + 0.007*SL	0.422 + 0.005*SL	0.440 + 0.004*SL
C to Y	t_R	0.106	0.089 + 0.008*SL	0.085 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.086	0.070 + 0.008*SL	0.070 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.471	0.458 + 0.007*SL	0.466 + 0.005*SL	0.476 + 0.004*SL
	t_{PHL}	0.466	0.452 + 0.007*SL	0.461 + 0.005*SL	0.478 + 0.004*SL
D to Y	t_R	0.105	0.088 + 0.008*SL	0.085 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.085	0.068 + 0.008*SL	0.070 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.398	0.385 + 0.006*SL	0.393 + 0.005*SL	0.404 + 0.004*SL
	t_{PHL}	0.423	0.410 + 0.007*SL	0.418 + 0.005*SL	0.436 + 0.004*SL
E to Y	t_R	0.105	0.089 + 0.008*SL	0.085 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.086	0.069 + 0.008*SL	0.070 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.403	0.390 + 0.007*SL	0.398 + 0.005*SL	0.409 + 0.004*SL
	t_{PHL}	0.470	0.456 + 0.007*SL	0.465 + 0.005*SL	0.482 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	x	x	x	1
x	x	x	0	0	x	1
x	x	x	x	x	0	1
Other States						0

Cell Data

Input Load (SL)																	
OA321						*OA321D2*						*OA321D4*					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9

Gate Count		
OA321	*OA321D2*	*OA321D4*
2.67	3.67	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA321

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.674	0.465 + 0.104*SL	0.449 + 0.108*SL	0.446 + 0.108*SL
	t_F	0.490	0.308 + 0.091*SL	0.299 + 0.093*SL	0.296 + 0.093*SL
	t_{PLH}	0.262	0.164 + 0.049*SL	0.169 + 0.048*SL	0.175 + 0.048*SL
	t_{PHL}	0.296	0.209 + 0.044*SL	0.212 + 0.043*SL	0.216 + 0.043*SL
B to Y	t_R	0.680	0.471 + 0.105*SL	0.457 + 0.108*SL	0.446 + 0.108*SL
	t_F	0.565	0.384 + 0.091*SL	0.375 + 0.093*SL	0.370 + 0.093*SL
	t_{PLH}	0.302	0.203 + 0.050*SL	0.210 + 0.048*SL	0.219 + 0.048*SL
	t_{PHL}	0.350	0.263 + 0.044*SL	0.266 + 0.043*SL	0.271 + 0.043*SL
C to Y	t_R	0.676	0.466 + 0.105*SL	0.454 + 0.108*SL	0.446 + 0.108*SL
	t_F	0.651	0.471 + 0.090*SL	0.460 + 0.093*SL	0.446 + 0.093*SL
	t_{PLH}	0.318	0.218 + 0.050*SL	0.226 + 0.048*SL	0.237 + 0.048*SL
	t_{PHL}	0.389	0.299 + 0.045*SL	0.306 + 0.043*SL	0.318 + 0.043*SL
D to Y	t_R	0.498	0.362 + 0.068*SL	0.343 + 0.073*SL	0.330 + 0.073*SL
	t_F	0.586	0.403 + 0.091*SL	0.394 + 0.094*SL	0.378 + 0.094*SL
	t_{PLH}	0.237	0.171 + 0.033*SL	0.173 + 0.032*SL	0.179 + 0.032*SL
	t_{PHL}	0.363	0.271 + 0.046*SL	0.281 + 0.044*SL	0.298 + 0.043*SL
E to Y	t_R	0.493	0.353 + 0.070*SL	0.342 + 0.073*SL	0.330 + 0.073*SL
	t_F	0.649	0.467 + 0.091*SL	0.460 + 0.093*SL	0.446 + 0.093*SL
	t_{PLH}	0.245	0.179 + 0.033*SL	0.182 + 0.033*SL	0.190 + 0.032*SL
	t_{PHL}	0.412	0.322 + 0.045*SL	0.330 + 0.043*SL	0.343 + 0.043*SL
F to Y	t_R	0.348	0.282 + 0.033*SL	0.264 + 0.038*SL	0.228 + 0.039*SL
	t_F	0.648	0.466 + 0.091*SL	0.460 + 0.093*SL	0.446 + 0.093*SL
	t_{PLH}	0.168	0.133 + 0.018*SL	0.133 + 0.018*SL	0.142 + 0.017*SL
	t_{PHL}	0.417	0.326 + 0.045*SL	0.334 + 0.043*SL	0.350 + 0.043*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA321D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.106	0.073 + 0.017*SL	0.063 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.087	0.055 + 0.016*SL	0.053 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.397	0.376 + 0.011*SL	0.383 + 0.009*SL	0.385 + 0.009*SL
	t_{PHL}	0.447	0.424 + 0.011*SL	0.434 + 0.009*SL	0.440 + 0.009*SL
B to Y	t_R	0.106	0.071 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.088	0.055 + 0.016*SL	0.055 + 0.016*SL	0.026 + 0.017*SL
	t_{PLH}	0.434	0.413 + 0.011*SL	0.420 + 0.009*SL	0.422 + 0.009*SL
	t_{PHL}	0.513	0.490 + 0.011*SL	0.500 + 0.009*SL	0.507 + 0.009*SL
C to Y	t_R	0.106	0.072 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.092	0.061 + 0.015*SL	0.056 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.452	0.431 + 0.011*SL	0.438 + 0.009*SL	0.440 + 0.009*SL
	t_{PHL}	0.567	0.544 + 0.011*SL	0.554 + 0.009*SL	0.561 + 0.009*SL
D to Y	t_R	0.101	0.067 + 0.017*SL	0.057 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.088	0.056 + 0.016*SL	0.055 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.371	0.350 + 0.010*SL	0.357 + 0.009*SL	0.359 + 0.009*SL
	t_{PHL}	0.511	0.488 + 0.011*SL	0.498 + 0.009*SL	0.505 + 0.009*SL
E to Y	t_R	0.100	0.065 + 0.018*SL	0.058 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.091	0.061 + 0.015*SL	0.056 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.383	0.363 + 0.010*SL	0.369 + 0.009*SL	0.371 + 0.009*SL
	t_{PHL}	0.590	0.567 + 0.011*SL	0.577 + 0.009*SL	0.584 + 0.009*SL
F to Y	t_R	0.097	0.062 + 0.017*SL	0.054 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.092	0.061 + 0.015*SL	0.057 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.307	0.286 + 0.010*SL	0.292 + 0.009*SL	0.294 + 0.009*SL
	t_{PHL}	0.593	0.570 + 0.011*SL	0.580 + 0.009*SL	0.587 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

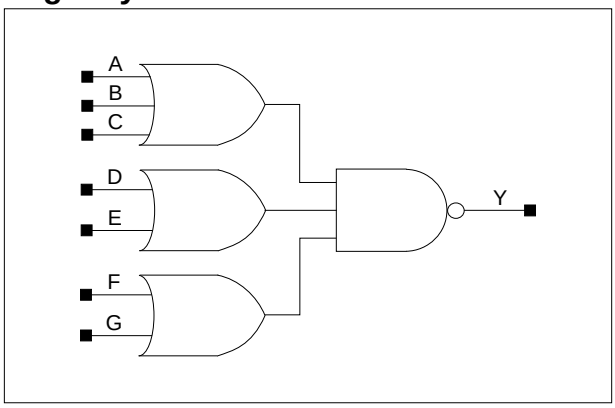
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA321D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.109	0.092 + 0.008*SL	0.088 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.090	0.074 + 0.008*SL	0.075 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.448	0.435 + 0.007*SL	0.444 + 0.005*SL	0.455 + 0.004*SL
	t_{PHL}	0.490	0.477 + 0.007*SL	0.486 + 0.005*SL	0.504 + 0.004*SL
B to Y	t_R	0.108	0.092 + 0.008*SL	0.088 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.091	0.075 + 0.008*SL	0.076 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.485	0.472 + 0.007*SL	0.480 + 0.005*SL	0.491 + 0.004*SL
	t_{PHL}	0.557	0.544 + 0.007*SL	0.552 + 0.005*SL	0.571 + 0.004*SL
C to Y	t_R	0.109	0.092 + 0.008*SL	0.089 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.094	0.078 + 0.008*SL	0.078 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.503	0.490 + 0.007*SL	0.498 + 0.005*SL	0.510 + 0.004*SL
	t_{PHL}	0.613	0.599 + 0.007*SL	0.608 + 0.005*SL	0.627 + 0.004*SL
D to Y	t_R	0.106	0.090 + 0.008*SL	0.086 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.092	0.077 + 0.008*SL	0.076 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.419	0.406 + 0.007*SL	0.414 + 0.005*SL	0.425 + 0.004*SL
	t_{PHL}	0.557	0.543 + 0.007*SL	0.552 + 0.005*SL	0.571 + 0.004*SL
E to Y	t_R	0.106	0.089 + 0.008*SL	0.086 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.094	0.079 + 0.008*SL	0.078 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.432	0.419 + 0.007*SL	0.427 + 0.005*SL	0.438 + 0.004*SL
	t_{PHL}	0.636	0.623 + 0.007*SL	0.631 + 0.005*SL	0.650 + 0.004*SL
F to Y	t_R	0.097	0.080 + 0.009*SL	0.077 + 0.009*SL	0.048 + 0.010*SL
	t_F	0.094	0.079 + 0.008*SL	0.078 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.348	0.336 + 0.006*SL	0.343 + 0.005*SL	0.353 + 0.004*SL
	t_{PHL}	0.639	0.626 + 0.007*SL	0.634 + 0.005*SL	0.653 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
0	0	0	x	x	x	x	1
x	x	x	0	0	x	x	1
x	x	x	x	x	0	0	1
Other States							0

Cell Data

Input Load (SL)							Gate Count
OA322							*OA322*
A	B	C	D	E	F	G	
0.9	0.9	0.9	1.0	0.9	0.9	1.0	2.67
OA322D2							*OA322D2*
A	B	C	D	E	F	G	
0.9	0.9	0.9	1.0	0.9	0.9	1.0	4.00
OA322D4							*OA322D4*
A	B	C	D	E	F	G	
0.9	0.9	1.0	0.9	0.9	0.9	1.0	4.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA322

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.785	0.576 + 0.104*SL	0.559 + 0.108*SL	0.556 + 0.108*SL
	t_F	0.550	0.367 + 0.091*SL	0.359 + 0.093*SL	0.356 + 0.093*SL
	t_{PLH}	0.278	0.178 + 0.050*SL	0.186 + 0.048*SL	0.194 + 0.048*SL
	t_{PHL}	0.347	0.259 + 0.044*SL	0.263 + 0.043*SL	0.268 + 0.043*SL
B to Y	t_R	0.791	0.582 + 0.105*SL	0.568 + 0.108*SL	0.556 + 0.108*SL
	t_F	0.626	0.443 + 0.092*SL	0.436 + 0.093*SL	0.433 + 0.093*SL
	t_{PLH}	0.320	0.219 + 0.050*SL	0.228 + 0.048*SL	0.240 + 0.048*SL
	t_{PHL}	0.404	0.316 + 0.044*SL	0.319 + 0.043*SL	0.325 + 0.043*SL
C to Y	t_R	0.788	0.577 + 0.105*SL	0.565 + 0.108*SL	0.556 + 0.108*SL
	t_F	0.711	0.529 + 0.091*SL	0.521 + 0.093*SL	0.510 + 0.093*SL
	t_{PLH}	0.337	0.236 + 0.051*SL	0.246 + 0.048*SL	0.259 + 0.048*SL
	t_{PHL}	0.444	0.355 + 0.045*SL	0.361 + 0.043*SL	0.373 + 0.043*SL
D to Y	t_R	0.589	0.451 + 0.069*SL	0.432 + 0.074*SL	0.418 + 0.074*SL
	t_F	0.628	0.451 + 0.088*SL	0.444 + 0.090*SL	0.431 + 0.091*SL
	t_{PLH}	0.251	0.183 + 0.034*SL	0.187 + 0.033*SL	0.198 + 0.033*SL
	t_{PHL}	0.410	0.321 + 0.044*SL	0.330 + 0.042*SL	0.347 + 0.042*SL
E to Y	t_R	0.584	0.443 + 0.071*SL	0.431 + 0.074*SL	0.418 + 0.074*SL
	t_F	0.711	0.527 + 0.092*SL	0.522 + 0.093*SL	0.509 + 0.093*SL
	t_{PLH}	0.255	0.186 + 0.034*SL	0.192 + 0.033*SL	0.204 + 0.033*SL
	t_{PHL}	0.468	0.379 + 0.045*SL	0.385 + 0.043*SL	0.399 + 0.043*SL
F to Y	t_R	0.617	0.479 + 0.069*SL	0.460 + 0.074*SL	0.444 + 0.074*SL
	t_F	0.639	0.457 + 0.091*SL	0.450 + 0.093*SL	0.436 + 0.093*SL
	t_{PLH}	0.270	0.202 + 0.034*SL	0.206 + 0.033*SL	0.216 + 0.033*SL
	t_{PHL}	0.421	0.330 + 0.046*SL	0.339 + 0.043*SL	0.356 + 0.043*SL
G to Y	t_R	0.611	0.470 + 0.070*SL	0.458 + 0.074*SL	0.444 + 0.074*SL
	t_F	0.711	0.527 + 0.092*SL	0.522 + 0.093*SL	0.510 + 0.093*SL
	t_{PLH}	0.279	0.210 + 0.034*SL	0.216 + 0.033*SL	0.226 + 0.033*SL
	t_{PHL}	0.473	0.383 + 0.045*SL	0.390 + 0.043*SL	0.404 + 0.043*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA322D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.111	0.077 + 0.017*SL	0.068 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.089	0.058 + 0.015*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.419	0.397 + 0.011*SL	0.405 + 0.009*SL	0.407 + 0.009*SL
	t_{PHL}	0.502	0.480 + 0.011*SL	0.489 + 0.009*SL	0.496 + 0.009*SL
B to Y	t_R	0.110	0.077 + 0.017*SL	0.068 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.090	0.058 + 0.016*SL	0.056 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.459	0.438 + 0.011*SL	0.446 + 0.009*SL	0.447 + 0.009*SL
	t_{PHL}	0.572	0.550 + 0.011*SL	0.560 + 0.009*SL	0.566 + 0.009*SL
C to Y	t_R	0.110	0.077 + 0.017*SL	0.068 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.092	0.061 + 0.016*SL	0.058 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.473	0.452 + 0.011*SL	0.460 + 0.009*SL	0.462 + 0.009*SL
	t_{PHL}	0.622	0.599 + 0.011*SL	0.609 + 0.009*SL	0.616 + 0.009*SL
D to Y	t_R	0.105	0.072 + 0.017*SL	0.062 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.090	0.057 + 0.016*SL	0.057 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.396	0.375 + 0.011*SL	0.382 + 0.009*SL	0.383 + 0.009*SL
	t_{PHL}	0.574	0.551 + 0.011*SL	0.561 + 0.009*SL	0.568 + 0.009*SL
E to Y	t_R	0.105	0.070 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.093	0.063 + 0.015*SL	0.057 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.400	0.379 + 0.011*SL	0.387 + 0.009*SL	0.388 + 0.009*SL
	t_{PHL}	0.646	0.623 + 0.011*SL	0.633 + 0.009*SL	0.640 + 0.009*SL
F to Y	t_R	0.106	0.072 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.091	0.061 + 0.015*SL	0.056 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.413	0.392 + 0.011*SL	0.399 + 0.009*SL	0.401 + 0.009*SL
	t_{PHL}	0.585	0.562 + 0.011*SL	0.573 + 0.009*SL	0.579 + 0.009*SL
G to Y	t_R	0.105	0.071 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.093	0.062 + 0.015*SL	0.058 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.421	0.400 + 0.011*SL	0.407 + 0.009*SL	0.409 + 0.009*SL
	t_{PHL}	0.650	0.627 + 0.011*SL	0.638 + 0.009*SL	0.645 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

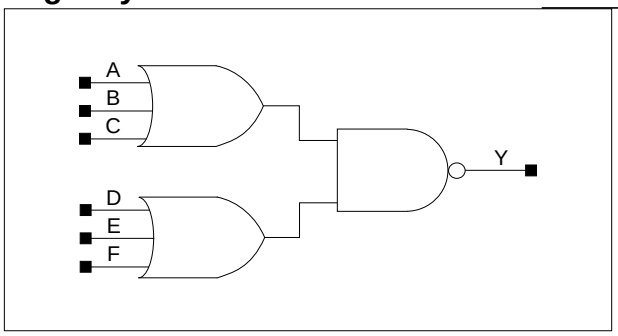
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA322D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.113	0.097 + 0.008*SL	0.092 + 0.009*SL	0.056 + 0.010*SL
	t_F	0.090	0.074 + 0.008*SL	0.076 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.474	0.460 + 0.007*SL	0.469 + 0.005*SL	0.480 + 0.004*SL
	t_{PHL}	0.544	0.531 + 0.007*SL	0.540 + 0.005*SL	0.557 + 0.004*SL
B to Y	t_R	0.113	0.096 + 0.008*SL	0.093 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.092	0.076 + 0.008*SL	0.077 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.510	0.496 + 0.007*SL	0.505 + 0.005*SL	0.516 + 0.004*SL
	t_{PHL}	0.610	0.597 + 0.007*SL	0.605 + 0.005*SL	0.623 + 0.004*SL
C to Y	t_R	0.113	0.096 + 0.008*SL	0.092 + 0.009*SL	0.056 + 0.010*SL
	t_F	0.095	0.079 + 0.008*SL	0.079 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.524	0.511 + 0.007*SL	0.520 + 0.005*SL	0.531 + 0.004*SL
	t_{PHL}	0.657	0.643 + 0.007*SL	0.652 + 0.005*SL	0.670 + 0.004*SL
D to Y	t_R	0.110	0.094 + 0.008*SL	0.089 + 0.009*SL	0.054 + 0.010*SL
	t_F	0.093	0.077 + 0.008*SL	0.077 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.446	0.433 + 0.007*SL	0.441 + 0.005*SL	0.452 + 0.004*SL
	t_{PHL}	0.614	0.601 + 0.007*SL	0.609 + 0.005*SL	0.627 + 0.004*SL
E to Y	t_R	0.110	0.094 + 0.008*SL	0.090 + 0.009*SL	0.054 + 0.010*SL
	t_F	0.095	0.078 + 0.008*SL	0.080 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.451	0.438 + 0.007*SL	0.446 + 0.005*SL	0.457 + 0.004*SL
	t_{PHL}	0.682	0.668 + 0.007*SL	0.677 + 0.005*SL	0.695 + 0.004*SL
F to Y	t_R	0.111	0.095 + 0.008*SL	0.090 + 0.009*SL	0.054 + 0.010*SL
	t_F	0.093	0.077 + 0.008*SL	0.078 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.462	0.449 + 0.007*SL	0.457 + 0.005*SL	0.468 + 0.004*SL
	t_{PHL}	0.620	0.606 + 0.007*SL	0.615 + 0.005*SL	0.633 + 0.004*SL
G to Y	t_R	0.111	0.094 + 0.008*SL	0.091 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.094	0.077 + 0.009*SL	0.080 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.470	0.457 + 0.007*SL	0.465 + 0.005*SL	0.476 + 0.004*SL
	t_{PHL}	0.685	0.671 + 0.007*SL	0.680 + 0.005*SL	0.698 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	x	x	x	1
x	x	x	0	0	0	1
Other States						0

Cell Data

Input Load (SL)																	
OA33						*OA33D2*						*OA33D4*					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
0.9	0.9	0.9	0.9	0.9	0.9	1.9	1.9	1.9	1.9	1.9	1.9	0.9	1.0	1.0	0.9	1.0	0.9

Gate Count		
OA33	*OA33D2*	*OA33D4*
2.33	4.00	3.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA33

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.737	0.532 + 0.102*SL	0.507 + 0.109*SL	0.495 + 0.109*SL
	t_F	0.363	0.235 + 0.064*SL	0.227 + 0.066*SL	0.211 + 0.066*SL
	t_{PLH}	0.233	0.135 + 0.049*SL	0.136 + 0.049*SL	0.159 + 0.048*SL
	t_{PHL}	0.236	0.167 + 0.034*SL	0.176 + 0.032*SL	0.189 + 0.032*SL
B to Y	t_R	0.743	0.536 + 0.104*SL	0.516 + 0.109*SL	0.495 + 0.109*SL
	t_F	0.421	0.291 + 0.065*SL	0.283 + 0.067*SL	0.268 + 0.067*SL
	t_{PLH}	0.271	0.170 + 0.050*SL	0.176 + 0.049*SL	0.203 + 0.048*SL
	t_{PHL}	0.281	0.212 + 0.034*SL	0.220 + 0.033*SL	0.232 + 0.032*SL
C to Y	t_R	0.739	0.531 + 0.104*SL	0.512 + 0.109*SL	0.495 + 0.109*SL
	t_F	0.482	0.353 + 0.064*SL	0.344 + 0.066*SL	0.323 + 0.067*SL
	t_{PLH}	0.286	0.185 + 0.051*SL	0.191 + 0.049*SL	0.219 + 0.048*SL
	t_{PHL}	0.308	0.237 + 0.035*SL	0.247 + 0.033*SL	0.265 + 0.032*SL
D to Y	t_R	0.675	0.464 + 0.105*SL	0.449 + 0.109*SL	0.447 + 0.109*SL
	t_F	0.362	0.232 + 0.065*SL	0.229 + 0.066*SL	0.213 + 0.066*SL
	t_{PLH}	0.287	0.189 + 0.049*SL	0.192 + 0.048*SL	0.196 + 0.048*SL
	t_{PHL}	0.241	0.171 + 0.035*SL	0.181 + 0.032*SL	0.196 + 0.032*SL
E to Y	t_R	0.681	0.470 + 0.106*SL	0.457 + 0.109*SL	0.447 + 0.109*SL
	t_F	0.420	0.289 + 0.066*SL	0.285 + 0.067*SL	0.270 + 0.067*SL
	t_{PLH}	0.324	0.225 + 0.050*SL	0.231 + 0.048*SL	0.239 + 0.048*SL
	t_{PHL}	0.287	0.217 + 0.035*SL	0.226 + 0.033*SL	0.240 + 0.032*SL
F to Y	t_R	0.678	0.465 + 0.106*SL	0.454 + 0.109*SL	0.447 + 0.109*SL
	t_F	0.479	0.348 + 0.065*SL	0.344 + 0.066*SL	0.323 + 0.067*SL
	t_{PLH}	0.338	0.237 + 0.050*SL	0.244 + 0.048*SL	0.254 + 0.048*SL
	t_{PHL}	0.313	0.242 + 0.035*SL	0.252 + 0.033*SL	0.271 + 0.032*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA33D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.510	0.408 + 0.051*SL	0.393 + 0.055*SL	0.379 + 0.055*SL
	t_F	0.304	0.241 + 0.032*SL	0.237 + 0.033*SL	0.217 + 0.033*SL
	t_{PLH}	0.188	0.140 + 0.024*SL	0.139 + 0.024*SL	0.148 + 0.024*SL
	t_{PHL}	0.204	0.168 + 0.018*SL	0.175 + 0.016*SL	0.193 + 0.016*SL
B to Y	t_R	0.514	0.411 + 0.052*SL	0.400 + 0.055*SL	0.379 + 0.055*SL
	t_F	0.355	0.291 + 0.032*SL	0.287 + 0.033*SL	0.268 + 0.033*SL
	t_{PLH}	0.218	0.168 + 0.025*SL	0.171 + 0.024*SL	0.187 + 0.024*SL
	t_{PHL}	0.244	0.209 + 0.017*SL	0.215 + 0.016*SL	0.231 + 0.016*SL
C to Y	t_R	0.510	0.406 + 0.052*SL	0.395 + 0.055*SL	0.379 + 0.055*SL
	t_F	0.422	0.358 + 0.032*SL	0.355 + 0.033*SL	0.329 + 0.033*SL
	t_{PLH}	0.237	0.185 + 0.026*SL	0.191 + 0.024*SL	0.208 + 0.024*SL
	t_{PHL}	0.273	0.237 + 0.018*SL	0.244 + 0.016*SL	0.268 + 0.016*SL
D to Y	t_R	0.572	0.468 + 0.052*SL	0.456 + 0.055*SL	0.449 + 0.055*SL
	t_F	0.303	0.237 + 0.033*SL	0.236 + 0.033*SL	0.218 + 0.034*SL
	t_{PLH}	0.243	0.194 + 0.024*SL	0.195 + 0.024*SL	0.199 + 0.024*SL
	t_{PHL}	0.211	0.175 + 0.018*SL	0.182 + 0.016*SL	0.202 + 0.016*SL
E to Y	t_R	0.578	0.473 + 0.052*SL	0.464 + 0.055*SL	0.449 + 0.055*SL
	t_F	0.356	0.291 + 0.033*SL	0.289 + 0.033*SL	0.273 + 0.033*SL
	t_{PLH}	0.282	0.231 + 0.025*SL	0.235 + 0.024*SL	0.245 + 0.024*SL
	t_{PHL}	0.253	0.218 + 0.018*SL	0.224 + 0.016*SL	0.242 + 0.016*SL
F to Y	t_R	0.574	0.468 + 0.053*SL	0.461 + 0.055*SL	0.449 + 0.055*SL
	t_F	0.418	0.352 + 0.033*SL	0.351 + 0.033*SL	0.328 + 0.033*SL
	t_{PLH}	0.297	0.247 + 0.025*SL	0.251 + 0.024*SL	0.262 + 0.024*SL
	t_{PHL}	0.280	0.244 + 0.018*SL	0.251 + 0.016*SL	0.276 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

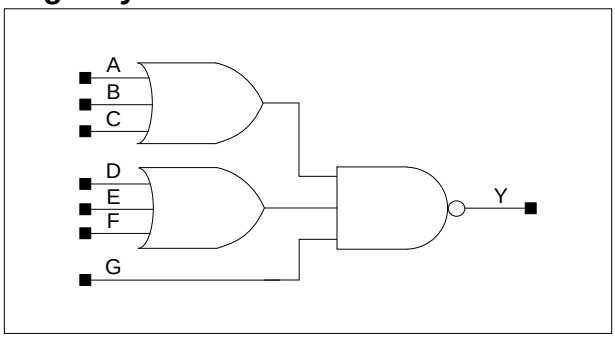
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA33D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.112	0.095 + 0.008*SL	0.092 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.085	0.068 + 0.008*SL	0.069 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.429	0.415 + 0.007*SL	0.424 + 0.005*SL	0.436 + 0.004*SL
	t_{PHL}	0.409	0.396 + 0.007*SL	0.404 + 0.005*SL	0.422 + 0.004*SL
B to Y	t_R	0.112	0.096 + 0.008*SL	0.091 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.086	0.070 + 0.008*SL	0.070 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.463	0.449 + 0.007*SL	0.458 + 0.005*SL	0.469 + 0.004*SL
	t_{PHL}	0.463	0.450 + 0.007*SL	0.458 + 0.005*SL	0.476 + 0.004*SL
C to Y	t_R	0.113	0.097 + 0.008*SL	0.092 + 0.009*SL	0.056 + 0.010*SL
	t_F	0.087	0.071 + 0.008*SL	0.073 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.477	0.464 + 0.007*SL	0.473 + 0.005*SL	0.484 + 0.004*SL
	t_{PHL}	0.501	0.487 + 0.007*SL	0.496 + 0.005*SL	0.513 + 0.004*SL
D to Y	t_R	0.114	0.099 + 0.008*SL	0.094 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.084	0.068 + 0.008*SL	0.069 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.479	0.465 + 0.007*SL	0.474 + 0.005*SL	0.486 + 0.004*SL
	t_{PHL}	0.414	0.401 + 0.007*SL	0.409 + 0.005*SL	0.427 + 0.004*SL
E to Y	t_R	0.115	0.099 + 0.008*SL	0.094 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.088	0.071 + 0.008*SL	0.072 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.528	0.514 + 0.007*SL	0.523 + 0.005*SL	0.535 + 0.004*SL
	t_{PHL}	0.505	0.491 + 0.007*SL	0.500 + 0.005*SL	0.517 + 0.004*SL
F to Y	t_R	0.115	0.098 + 0.008*SL	0.095 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.086	0.069 + 0.008*SL	0.070 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.512	0.499 + 0.007*SL	0.508 + 0.005*SL	0.519 + 0.004*SL
	t_{PHL}	0.468	0.454 + 0.007*SL	0.462 + 0.005*SL	0.480 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
0	0	0	x	x	x	x	1
x	x	x	0	0	0	x	1
x	x	x	x	x	x	0	1
Other States							0

Cell Data

Input Load (SL)							Gate Count
OA331							*OA331*
A	B	C	D	E	F	G	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	2.67
OA331D2							*OA331D2*
A	B	C	D	E	F	G	
0.9	0.9	0.9	0.9	0.9	0.9	1.0	3.67
OA331D4							*OA331D4*
A	B	C	D	E	F	G	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	4.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA331

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.817	0.611 + 0.103*SL	0.589 + 0.109*SL	0.579 + 0.109*SL
	t_F	0.569	0.390 + 0.089*SL	0.380 + 0.092*SL	0.368 + 0.092*SL
	t_{PLH}	0.260	0.161 + 0.050*SL	0.164 + 0.049*SL	0.189 + 0.048*SL
	t_{PHL}	0.336	0.246 + 0.045*SL	0.255 + 0.043*SL	0.270 + 0.042*SL
B to Y	t_R	0.824	0.616 + 0.104*SL	0.599 + 0.108*SL	0.579 + 0.109*SL
	t_F	0.642	0.461 + 0.091*SL	0.453 + 0.093*SL	0.442 + 0.093*SL
	t_{PLH}	0.296	0.196 + 0.050*SL	0.202 + 0.049*SL	0.230 + 0.048*SL
	t_{PHL}	0.394	0.304 + 0.045*SL	0.311 + 0.043*SL	0.324 + 0.043*SL
C to Y	t_R	0.681	0.470 + 0.106*SL	0.458 + 0.109*SL	0.449 + 0.109*SL
	t_F	0.728	0.548 + 0.090*SL	0.538 + 0.092*SL	0.519 + 0.093*SL
	t_{PLH}	0.315	0.215 + 0.050*SL	0.223 + 0.048*SL	0.237 + 0.048*SL
	t_{PHL}	0.438	0.347 + 0.046*SL	0.356 + 0.043*SL	0.374 + 0.043*SL
D to Y	t_R	0.736	0.525 + 0.105*SL	0.512 + 0.109*SL	0.513 + 0.109*SL
	t_F	0.577	0.395 + 0.091*SL	0.385 + 0.094*SL	0.369 + 0.094*SL
	t_{PLH}	0.310	0.212 + 0.049*SL	0.216 + 0.048*SL	0.221 + 0.048*SL
	t_{PHL}	0.362	0.269 + 0.046*SL	0.280 + 0.044*SL	0.297 + 0.043*SL
E to Y	t_R	0.744	0.532 + 0.106*SL	0.521 + 0.109*SL	0.513 + 0.109*SL
	t_F	0.656	0.473 + 0.092*SL	0.465 + 0.094*SL	0.451 + 0.094*SL
	t_{PLH}	0.356	0.257 + 0.050*SL	0.263 + 0.048*SL	0.272 + 0.048*SL
	t_{PHL}	0.425	0.334 + 0.046*SL	0.342 + 0.044*SL	0.357 + 0.043*SL
F to Y	t_R	0.741	0.528 + 0.106*SL	0.519 + 0.109*SL	0.513 + 0.109*SL
	t_F	0.730	0.550 + 0.090*SL	0.541 + 0.092*SL	0.519 + 0.093*SL
	t_{PLH}	0.373	0.273 + 0.050*SL	0.280 + 0.048*SL	0.289 + 0.048*SL
	t_{PHL}	0.462	0.370 + 0.046*SL	0.380 + 0.043*SL	0.400 + 0.043*SL
G to Y	t_R	0.353	0.287 + 0.033*SL	0.269 + 0.038*SL	0.233 + 0.039*SL
	t_F	0.728	0.547 + 0.090*SL	0.539 + 0.092*SL	0.519 + 0.093*SL
	t_{PLH}	0.171	0.135 + 0.018*SL	0.136 + 0.018*SL	0.145 + 0.017*SL
	t_{PHL}	0.470	0.378 + 0.046*SL	0.388 + 0.043*SL	0.411 + 0.043*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA331D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.111	0.078 + 0.017*SL	0.068 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.090	0.060 + 0.015*SL	0.055 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.407	0.385 + 0.011*SL	0.394 + 0.009*SL	0.397 + 0.009*SL
	t_{PHL}	0.506	0.483 + 0.011*SL	0.493 + 0.009*SL	0.500 + 0.009*SL
B to Y	t_R	0.111	0.077 + 0.017*SL	0.069 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.091	0.060 + 0.016*SL	0.057 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.443	0.422 + 0.011*SL	0.430 + 0.009*SL	0.433 + 0.009*SL
	t_{PHL}	0.574	0.551 + 0.011*SL	0.561 + 0.009*SL	0.568 + 0.009*SL
C to Y	t_R	0.111	0.077 + 0.017*SL	0.069 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.094	0.062 + 0.016*SL	0.060 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.460	0.438 + 0.011*SL	0.446 + 0.009*SL	0.449 + 0.009*SL
	t_{PHL}	0.619	0.596 + 0.012*SL	0.606 + 0.009*SL	0.613 + 0.009*SL
D to Y	t_R	0.108	0.074 + 0.017*SL	0.067 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.089	0.058 + 0.016*SL	0.055 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.455	0.433 + 0.011*SL	0.441 + 0.009*SL	0.443 + 0.009*SL
	t_{PHL}	0.517	0.494 + 0.011*SL	0.504 + 0.009*SL	0.511 + 0.009*SL
E to Y	t_R	0.109	0.075 + 0.017*SL	0.066 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.092	0.060 + 0.016*SL	0.057 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.494	0.472 + 0.011*SL	0.480 + 0.009*SL	0.482 + 0.009*SL
	t_{PHL}	0.591	0.568 + 0.011*SL	0.578 + 0.009*SL	0.585 + 0.009*SL
F to Y	t_R	0.109	0.075 + 0.017*SL	0.066 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.094	0.063 + 0.015*SL	0.059 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.513	0.491 + 0.011*SL	0.499 + 0.009*SL	0.501 + 0.009*SL
	t_{PHL}	0.645	0.622 + 0.012*SL	0.632 + 0.009*SL	0.639 + 0.009*SL
G to Y	t_R	0.097	0.063 + 0.017*SL	0.054 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.094	0.063 + 0.015*SL	0.059 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.314	0.293 + 0.010*SL	0.299 + 0.009*SL	0.301 + 0.009*SL
	t_{PHL}	0.652	0.629 + 0.012*SL	0.639 + 0.009*SL	0.646 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

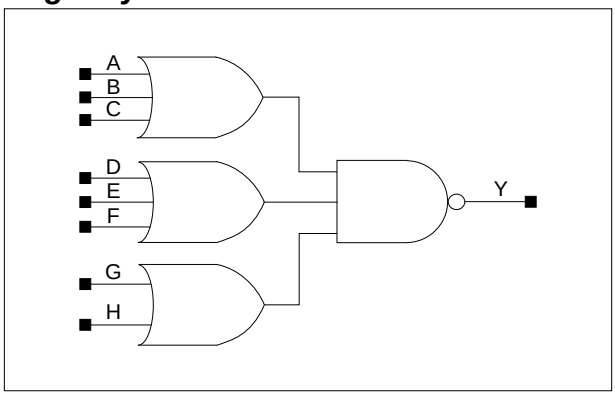
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA331D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.114	0.098 + 0.008*SL	0.094 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.092	0.075 + 0.008*SL	0.078 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.461	0.448 + 0.007*SL	0.456 + 0.005*SL	0.469 + 0.004*SL
	t_{PHL}	0.546	0.532 + 0.007*SL	0.542 + 0.005*SL	0.560 + 0.004*SL
B to Y	t_R	0.115	0.099 + 0.008*SL	0.095 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.094	0.078 + 0.008*SL	0.078 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.497	0.484 + 0.007*SL	0.493 + 0.005*SL	0.505 + 0.004*SL
	t_{PHL}	0.615	0.601 + 0.007*SL	0.610 + 0.005*SL	0.628 + 0.004*SL
C to Y	t_R	0.115	0.099 + 0.008*SL	0.095 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.096	0.080 + 0.008*SL	0.081 + 0.008*SL	0.051 + 0.008*SL
	t_{PLH}	0.514	0.500 + 0.007*SL	0.509 + 0.005*SL	0.521 + 0.004*SL
	t_{PHL}	0.661	0.647 + 0.007*SL	0.656 + 0.005*SL	0.675 + 0.004*SL
D to Y	t_R	0.117	0.100 + 0.008*SL	0.097 + 0.009*SL	0.058 + 0.010*SL
	t_F	0.092	0.076 + 0.008*SL	0.076 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.509	0.495 + 0.007*SL	0.504 + 0.005*SL	0.517 + 0.004*SL
	t_{PHL}	0.558	0.544 + 0.007*SL	0.553 + 0.005*SL	0.571 + 0.004*SL
E to Y	t_R	0.117	0.101 + 0.008*SL	0.096 + 0.009*SL	0.058 + 0.010*SL
	t_F	0.094	0.077 + 0.008*SL	0.078 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.548	0.534 + 0.007*SL	0.543 + 0.005*SL	0.556 + 0.004*SL
	t_{PHL}	0.632	0.618 + 0.007*SL	0.627 + 0.005*SL	0.645 + 0.004*SL
F to Y	t_R	0.117	0.101 + 0.008*SL	0.097 + 0.009*SL	0.058 + 0.010*SL
	t_F	0.096	0.079 + 0.008*SL	0.082 + 0.008*SL	0.051 + 0.008*SL
	t_{PLH}	0.567	0.553 + 0.007*SL	0.563 + 0.005*SL	0.575 + 0.004*SL
	t_{PHL}	0.687	0.673 + 0.007*SL	0.682 + 0.005*SL	0.700 + 0.004*SL
G to Y	t_R	0.102	0.085 + 0.008*SL	0.081 + 0.009*SL	0.050 + 0.010*SL
	t_F	0.096	0.080 + 0.008*SL	0.081 + 0.008*SL	0.051 + 0.008*SL
	t_{PLH}	0.355	0.342 + 0.006*SL	0.349 + 0.005*SL	0.360 + 0.004*SL
	t_{PHL}	0.693	0.679 + 0.007*SL	0.688 + 0.005*SL	0.707 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	0	x	x	x	x	x	1
x	x	x	0	0	0	x	x	1
x	x	x	x	x	x	0	0	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
OA332								*OA332*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	1.0	3.00
OA332D2								*OA332D2*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	1.0	4.33
OA332D4								*OA332D4*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	1.0	4.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA332

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.945	0.738 + 0.104*SL	0.718 + 0.109*SL	0.708 + 0.109*SL
	t_F	0.478	0.327 + 0.076*SL	0.317 + 0.078*SL	0.312 + 0.078*SL
	t_{PLH}	0.285	0.184 + 0.050*SL	0.191 + 0.049*SL	0.217 + 0.048*SL
	t_{PHL}	0.308	0.233 + 0.037*SL	0.237 + 0.037*SL	0.242 + 0.036*SL
B to Y	t_R	0.951	0.743 + 0.104*SL	0.727 + 0.108*SL	0.708 + 0.109*SL
	t_F	0.544	0.390 + 0.077*SL	0.382 + 0.079*SL	0.377 + 0.079*SL
	t_{PLH}	0.322	0.220 + 0.051*SL	0.228 + 0.049*SL	0.258 + 0.048*SL
	t_{PHL}	0.357	0.281 + 0.038*SL	0.284 + 0.037*SL	0.290 + 0.037*SL
C to Y	t_R	0.947	0.738 + 0.105*SL	0.723 + 0.108*SL	0.708 + 0.109*SL
	t_F	0.619	0.465 + 0.077*SL	0.457 + 0.079*SL	0.444 + 0.079*SL
	t_{PLH}	0.341	0.239 + 0.051*SL	0.248 + 0.049*SL	0.279 + 0.048*SL
	t_{PHL}	0.392	0.314 + 0.039*SL	0.320 + 0.037*SL	0.332 + 0.037*SL
D to Y	t_R	0.866	0.656 + 0.105*SL	0.642 + 0.109*SL	0.642 + 0.109*SL
	t_F	0.648	0.464 + 0.092*SL	0.457 + 0.094*SL	0.444 + 0.094*SL
	t_{PLH}	0.336	0.238 + 0.049*SL	0.242 + 0.048*SL	0.248 + 0.048*SL
	t_{PHL}	0.425	0.333 + 0.046*SL	0.342 + 0.044*SL	0.358 + 0.043*SL
E to Y	t_R	0.874	0.663 + 0.106*SL	0.651 + 0.109*SL	0.642 + 0.109*SL
	t_F	0.728	0.543 + 0.092*SL	0.538 + 0.094*SL	0.525 + 0.094*SL
	t_{PLH}	0.382	0.282 + 0.050*SL	0.289 + 0.048*SL	0.299 + 0.048*SL
	t_{PHL}	0.488	0.397 + 0.045*SL	0.404 + 0.044*SL	0.418 + 0.043*SL
F to Y	t_R	0.871	0.658 + 0.106*SL	0.649 + 0.109*SL	0.642 + 0.109*SL
	t_F	0.799	0.617 + 0.091*SL	0.611 + 0.092*SL	0.593 + 0.093*SL
	t_{PLH}	0.398	0.298 + 0.050*SL	0.305 + 0.048*SL	0.316 + 0.048*SL
	t_{PHL}	0.525	0.434 + 0.045*SL	0.442 + 0.043*SL	0.461 + 0.043*SL
G to Y	t_R	0.639	0.502 + 0.068*SL	0.484 + 0.073*SL	0.468 + 0.073*SL
	t_F	0.743	0.560 + 0.092*SL	0.552 + 0.093*SL	0.532 + 0.094*SL
	t_{PLH}	0.280	0.213 + 0.034*SL	0.217 + 0.033*SL	0.229 + 0.032*SL
	t_{PHL}	0.492	0.399 + 0.047*SL	0.409 + 0.044*SL	0.433 + 0.043*SL
H to Y	t_R	0.635	0.495 + 0.070*SL	0.483 + 0.073*SL	0.468 + 0.073*SL
	t_F	0.798	0.616 + 0.091*SL	0.610 + 0.092*SL	0.593 + 0.093*SL
	t_{PLH}	0.286	0.218 + 0.034*SL	0.224 + 0.033*SL	0.237 + 0.032*SL
	t_{PHL}	0.538	0.447 + 0.045*SL	0.456 + 0.043*SL	0.475 + 0.043*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA332D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.117	0.083 + 0.017*SL	0.075 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.086	0.054 + 0.016*SL	0.053 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.447	0.425 + 0.011*SL	0.435 + 0.009*SL	0.438 + 0.009*SL
	t_{PHL}	0.468	0.445 + 0.011*SL	0.455 + 0.009*SL	0.461 + 0.009*SL
B to Y	t_R	0.117	0.084 + 0.017*SL	0.075 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.088	0.056 + 0.016*SL	0.054 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.483	0.461 + 0.011*SL	0.471 + 0.009*SL	0.474 + 0.009*SL
	t_{PHL}	0.527	0.505 + 0.011*SL	0.514 + 0.009*SL	0.521 + 0.009*SL
C to Y	t_R	0.117	0.083 + 0.017*SL	0.075 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.090	0.058 + 0.016*SL	0.056 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.502	0.479 + 0.011*SL	0.489 + 0.009*SL	0.492 + 0.009*SL
	t_{PHL}	0.573	0.550 + 0.011*SL	0.560 + 0.009*SL	0.566 + 0.009*SL
D to Y	t_R	0.119	0.086 + 0.017*SL	0.077 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.092	0.061 + 0.016*SL	0.057 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.490	0.467 + 0.011*SL	0.477 + 0.009*SL	0.481 + 0.009*SL
	t_{PHL}	0.602	0.579 + 0.012*SL	0.590 + 0.009*SL	0.596 + 0.009*SL
E to Y	t_R	0.119	0.086 + 0.017*SL	0.077 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.094	0.062 + 0.016*SL	0.060 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.535	0.513 + 0.011*SL	0.523 + 0.009*SL	0.527 + 0.009*SL
	t_{PHL}	0.679	0.656 + 0.012*SL	0.666 + 0.009*SL	0.673 + 0.009*SL
F to Y	t_R	0.119	0.085 + 0.017*SL	0.077 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.096	0.065 + 0.015*SL	0.061 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.552	0.529 + 0.011*SL	0.539 + 0.009*SL	0.542 + 0.009*SL
	t_{PHL}	0.727	0.704 + 0.012*SL	0.714 + 0.009*SL	0.721 + 0.009*SL
G to Y	t_R	0.107	0.074 + 0.017*SL	0.065 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.094	0.062 + 0.016*SL	0.060 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.437	0.416 + 0.011*SL	0.424 + 0.009*SL	0.425 + 0.009*SL
	t_{PHL}	0.683	0.660 + 0.012*SL	0.670 + 0.009*SL	0.677 + 0.009*SL
H to Y	t_R	0.107	0.074 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.096	0.064 + 0.016*SL	0.062 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.443	0.422 + 0.011*SL	0.429 + 0.009*SL	0.431 + 0.009*SL
	t_{PHL}	0.740	0.716 + 0.012*SL	0.727 + 0.009*SL	0.734 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

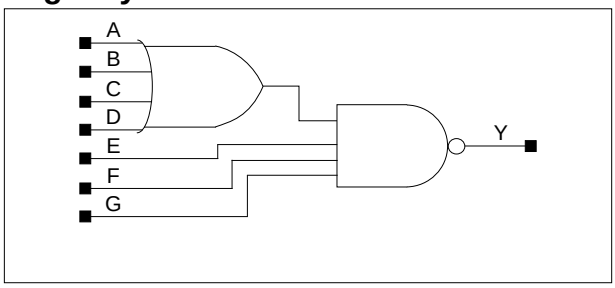
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA332D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.120	0.105 + 0.008*SL	0.099 + 0.009*SL	0.060 + 0.010*SL
	t_F	0.089	0.072 + 0.008*SL	0.073 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.504	0.490 + 0.007*SL	0.499 + 0.005*SL	0.513 + 0.004*SL
	t_{PHL}	0.509	0.495 + 0.007*SL	0.504 + 0.005*SL	0.521 + 0.004*SL
B to Y	t_R	0.121	0.105 + 0.008*SL	0.101 + 0.009*SL	0.061 + 0.010*SL
	t_F	0.090	0.074 + 0.008*SL	0.074 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.539	0.525 + 0.007*SL	0.535 + 0.005*SL	0.548 + 0.004*SL
	t_{PHL}	0.569	0.555 + 0.007*SL	0.564 + 0.005*SL	0.582 + 0.004*SL
C to Y	t_R	0.120	0.104 + 0.008*SL	0.099 + 0.009*SL	0.060 + 0.010*SL
	t_F	0.092	0.076 + 0.008*SL	0.076 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.558	0.544 + 0.007*SL	0.554 + 0.005*SL	0.567 + 0.004*SL
	t_{PHL}	0.616	0.602 + 0.007*SL	0.611 + 0.005*SL	0.629 + 0.004*SL
D to Y	t_R	0.123	0.108 + 0.008*SL	0.102 + 0.009*SL	0.061 + 0.010*SL
	t_F	0.094	0.078 + 0.008*SL	0.079 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.547	0.533 + 0.007*SL	0.543 + 0.005*SL	0.556 + 0.004*SL
	t_{PHL}	0.647	0.633 + 0.007*SL	0.642 + 0.005*SL	0.661 + 0.004*SL
E to Y	t_R	0.123	0.107 + 0.008*SL	0.103 + 0.009*SL	0.062 + 0.010*SL
	t_F	0.096	0.079 + 0.008*SL	0.081 + 0.008*SL	0.051 + 0.008*SL
	t_{PLH}	0.593	0.579 + 0.007*SL	0.589 + 0.005*SL	0.602 + 0.004*SL
	t_{PHL}	0.724	0.710 + 0.007*SL	0.720 + 0.005*SL	0.738 + 0.004*SL
F to Y	t_R	0.123	0.107 + 0.008*SL	0.103 + 0.009*SL	0.062 + 0.010*SL
	t_F	0.098	0.082 + 0.008*SL	0.083 + 0.008*SL	0.052 + 0.008*SL
	t_{PLH}	0.609	0.595 + 0.007*SL	0.605 + 0.005*SL	0.618 + 0.004*SL
	t_{PHL}	0.773	0.760 + 0.007*SL	0.769 + 0.005*SL	0.787 + 0.004*SL
G to Y	t_R	0.118	0.101 + 0.008*SL	0.098 + 0.009*SL	0.058 + 0.010*SL
	t_F	0.097	0.080 + 0.008*SL	0.083 + 0.008*SL	0.052 + 0.008*SL
	t_{PLH}	0.490	0.476 + 0.007*SL	0.486 + 0.005*SL	0.498 + 0.004*SL
	t_{PHL}	0.729	0.715 + 0.007*SL	0.724 + 0.005*SL	0.743 + 0.004*SL
H to Y	t_R	0.118	0.102 + 0.008*SL	0.098 + 0.009*SL	0.058 + 0.010*SL
	t_F	0.098	0.082 + 0.008*SL	0.083 + 0.008*SL	0.052 + 0.008*SL
	t_{PLH}	0.497	0.483 + 0.007*SL	0.492 + 0.005*SL	0.504 + 0.004*SL
	t_{PHL}	0.786	0.772 + 0.007*SL	0.782 + 0.005*SL	0.800 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
0	0	0	0	x	x	x	1
x	x	x	x	0	x	x	1
x	x	x	x	x	0	x	1
x	x	x	x	x	x	0	1
Other States							0

Cell Data

Input Load (SL)							Gate Count
OA4111							*OA4111*
A	B	C	D	E	F	G	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	2.67
OA4111D2							*OA4111D2*
A	B	C	D	E	F	G	
0.9	0.9	0.9	0.9	0.9	0.9	1.0	3.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA4111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.803	0.517 + 0.143*SL	0.510 + 0.145*SL	0.530 + 0.144*SL
	t_F	0.585	0.352 + 0.116*SL	0.346 + 0.118*SL	0.349 + 0.118*SL
	t_{PLH}	0.310	0.184 + 0.063*SL	0.182 + 0.063*SL	0.182 + 0.063*SL
	t_{PHL}	0.302	0.196 + 0.053*SL	0.197 + 0.053*SL	0.199 + 0.053*SL
B to Y	t_R	0.829	0.545 + 0.142*SL	0.535 + 0.144*SL	0.530 + 0.144*SL
	t_F	0.681	0.449 + 0.116*SL	0.442 + 0.118*SL	0.442 + 0.118*SL
	t_{PLH}	0.381	0.253 + 0.064*SL	0.256 + 0.064*SL	0.260 + 0.063*SL
	t_{PHL}	0.373	0.266 + 0.054*SL	0.268 + 0.053*SL	0.271 + 0.053*SL
C to Y	t_R	0.830	0.547 + 0.141*SL	0.537 + 0.144*SL	0.530 + 0.144*SL
	t_F	0.796	0.567 + 0.114*SL	0.555 + 0.117*SL	0.542 + 0.118*SL
	t_{PLH}	0.434	0.305 + 0.065*SL	0.309 + 0.064*SL	0.315 + 0.063*SL
	t_{PHL}	0.430	0.320 + 0.055*SL	0.328 + 0.053*SL	0.341 + 0.053*SL
D to Y	t_R	0.829	0.545 + 0.142*SL	0.536 + 0.144*SL	0.530 + 0.144*SL
	t_F	0.897	0.671 + 0.113*SL	0.662 + 0.115*SL	0.636 + 0.116*SL
	t_{PLH}	0.453	0.324 + 0.065*SL	0.329 + 0.064*SL	0.335 + 0.063*SL
	t_{PHL}	0.459	0.346 + 0.057*SL	0.361 + 0.053*SL	0.390 + 0.052*SL
E to Y	t_R	0.300	0.233 + 0.033*SL	0.217 + 0.037*SL	0.187 + 0.038*SL
	t_F	0.895	0.668 + 0.114*SL	0.662 + 0.115*SL	0.636 + 0.116*SL
	t_{PLH}	0.166	0.131 + 0.018*SL	0.132 + 0.017*SL	0.136 + 0.017*SL
	t_{PHL}	0.507	0.392 + 0.057*SL	0.409 + 0.053*SL	0.442 + 0.052*SL
F to Y	t_R	0.313	0.246 + 0.034*SL	0.229 + 0.038*SL	0.198 + 0.039*SL
	t_F	0.895	0.668 + 0.114*SL	0.662 + 0.115*SL	0.636 + 0.116*SL
	t_{PLH}	0.173	0.138 + 0.018*SL	0.138 + 0.018*SL	0.142 + 0.017*SL
	t_{PHL}	0.508	0.393 + 0.057*SL	0.409 + 0.053*SL	0.443 + 0.052*SL
G to Y	t_R	0.324	0.257 + 0.034*SL	0.240 + 0.038*SL	0.208 + 0.039*SL
	t_F	0.895	0.668 + 0.114*SL	0.662 + 0.115*SL	0.636 + 0.116*SL
	t_{PLH}	0.177	0.142 + 0.018*SL	0.143 + 0.018*SL	0.147 + 0.017*SL
	t_{PHL}	0.506	0.391 + 0.058*SL	0.408 + 0.053*SL	0.441 + 0.052*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

OA4111D2

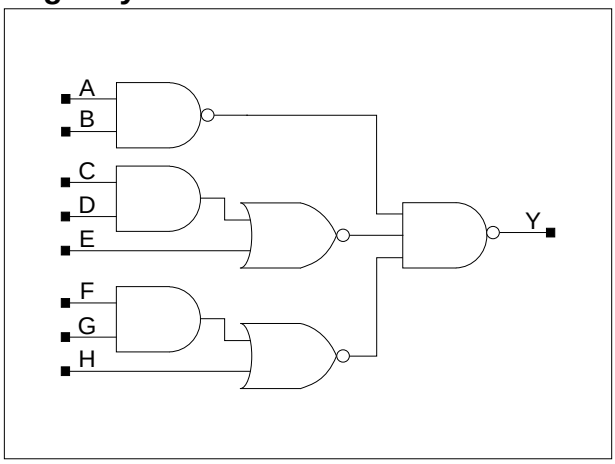
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.106	0.071 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.100	0.068 + 0.016*SL	0.065 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.555	0.533 + 0.011*SL	0.541 + 0.009*SL	0.543 + 0.009*SL
	t_{PHL}	0.636	0.613 + 0.012*SL	0.624 + 0.009*SL	0.632 + 0.009*SL
B to Y	t_R	0.107	0.073 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.095	0.064 + 0.016*SL	0.061 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.533	0.511 + 0.011*SL	0.519 + 0.009*SL	0.521 + 0.009*SL
	t_{PHL}	0.584	0.561 + 0.012*SL	0.572 + 0.009*SL	0.579 + 0.009*SL
C to Y	t_R	0.106	0.073 + 0.017*SL	0.064 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.092	0.060 + 0.016*SL	0.057 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.482	0.460 + 0.011*SL	0.468 + 0.009*SL	0.470 + 0.009*SL
	t_{PHL}	0.512	0.489 + 0.012*SL	0.499 + 0.009*SL	0.507 + 0.009*SL
D to Y	t_R	0.106	0.072 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.089	0.057 + 0.016*SL	0.055 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.418	0.396 + 0.011*SL	0.404 + 0.009*SL	0.406 + 0.009*SL
	t_{PHL}	0.425	0.402 + 0.012*SL	0.412 + 0.009*SL	0.419 + 0.009*SL
E to Y	t_R	0.094	0.060 + 0.017*SL	0.052 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.091	0.060 + 0.015*SL	0.056 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.292	0.271 + 0.010*SL	0.277 + 0.009*SL	0.279 + 0.009*SL
	t_{PHL}	0.506	0.483 + 0.012*SL	0.494 + 0.009*SL	0.501 + 0.009*SL
F to Y	t_R	0.094	0.059 + 0.018*SL	0.052 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.091	0.060 + 0.016*SL	0.056 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.300	0.279 + 0.010*SL	0.285 + 0.009*SL	0.287 + 0.009*SL
	t_{PHL}	0.504	0.481 + 0.011*SL	0.491 + 0.009*SL	0.498 + 0.009*SL
G to Y	t_R	0.095	0.061 + 0.017*SL	0.053 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.090	0.058 + 0.016*SL	0.057 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.305	0.285 + 0.010*SL	0.291 + 0.009*SL	0.293 + 0.009*SL
	t_{PHL}	0.501	0.477 + 0.012*SL	0.488 + 0.009*SL	0.495 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

SCG1

2-NAND and two (2-AND into 2-NOR)s into 3-NAND

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	x	x	x	x	x	x	1
x	x	1	1	x	x	x	x	1
x	x	x	x	1	x	x	x	1
x	x	x	x	x	1	1	x	1
x	x	x	x	x	x	x	1	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
A	B	C	D	E	F	G	H	
0.7	0.7	0.8	0.8	0.8	0.8	0.8	0.8	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

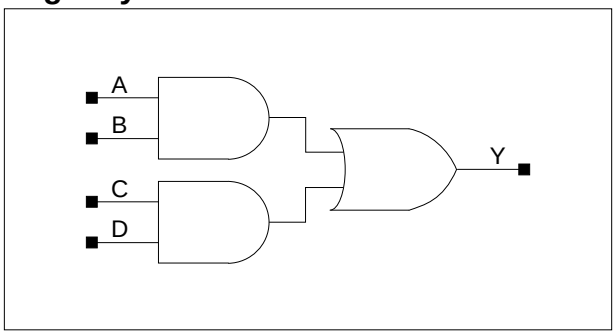
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.190	0.111 + 0.039*SL	0.102 + 0.042*SL	0.083 + 0.042*SL
	t_F	0.219	0.119 + 0.050*SL	0.112 + 0.052*SL	0.103 + 0.052*SL
	t_{PLH}	0.246	0.204 + 0.021*SL	0.212 + 0.019*SL	0.215 + 0.019*SL
	t_{PHL}	0.233	0.184 + 0.025*SL	0.187 + 0.024*SL	0.189 + 0.024*SL
B to Y	t_R	0.190	0.112 + 0.039*SL	0.102 + 0.042*SL	0.083 + 0.042*SL
	t_F	0.220	0.119 + 0.050*SL	0.113 + 0.052*SL	0.103 + 0.052*SL
	t_{PLH}	0.233	0.190 + 0.021*SL	0.198 + 0.019*SL	0.201 + 0.019*SL
	t_{PHL}	0.242	0.192 + 0.025*SL	0.196 + 0.024*SL	0.197 + 0.024*SL
C to Y	t_R	0.207	0.128 + 0.039*SL	0.119 + 0.042*SL	0.101 + 0.042*SL
	t_F	0.229	0.129 + 0.050*SL	0.123 + 0.052*SL	0.108 + 0.052*SL
	t_{PLH}	0.255	0.214 + 0.020*SL	0.220 + 0.019*SL	0.221 + 0.019*SL
	t_{PHL}	0.269	0.218 + 0.025*SL	0.224 + 0.024*SL	0.229 + 0.024*SL
D to Y	t_R	0.207	0.129 + 0.039*SL	0.119 + 0.042*SL	0.101 + 0.042*SL
	t_F	0.233	0.134 + 0.049*SL	0.125 + 0.051*SL	0.108 + 0.052*SL
	t_{PLH}	0.242	0.201 + 0.020*SL	0.207 + 0.019*SL	0.209 + 0.019*SL
	t_{PHL}	0.283	0.232 + 0.026*SL	0.239 + 0.024*SL	0.244 + 0.024*SL
E to Y	t_R	0.203	0.124 + 0.039*SL	0.114 + 0.042*SL	0.100 + 0.042*SL
	t_F	0.233	0.134 + 0.050*SL	0.126 + 0.051*SL	0.108 + 0.052*SL
	t_{PLH}	0.258	0.218 + 0.020*SL	0.221 + 0.019*SL	0.223 + 0.019*SL
	t_{PHL}	0.311	0.259 + 0.026*SL	0.267 + 0.024*SL	0.272 + 0.024*SL
F to Y	t_R	0.229	0.152 + 0.039*SL	0.140 + 0.042*SL	0.120 + 0.042*SL
	t_F	0.225	0.125 + 0.050*SL	0.119 + 0.052*SL	0.107 + 0.052*SL
	t_{PLH}	0.264	0.223 + 0.020*SL	0.228 + 0.019*SL	0.230 + 0.019*SL
	t_{PHL}	0.267	0.216 + 0.025*SL	0.222 + 0.024*SL	0.227 + 0.024*SL
G to Y	t_R	0.229	0.152 + 0.039*SL	0.140 + 0.042*SL	0.120 + 0.042*SL
	t_F	0.227	0.126 + 0.050*SL	0.120 + 0.052*SL	0.107 + 0.052*SL
	t_{PLH}	0.249	0.209 + 0.020*SL	0.213 + 0.019*SL	0.216 + 0.019*SL
	t_{PHL}	0.280	0.229 + 0.025*SL	0.235 + 0.024*SL	0.240 + 0.024*SL
H to Y	t_R	0.224	0.146 + 0.039*SL	0.135 + 0.042*SL	0.119 + 0.042*SL
	t_F	0.227	0.127 + 0.050*SL	0.121 + 0.052*SL	0.107 + 0.052*SL
	t_{PLH}	0.265	0.225 + 0.020*SL	0.228 + 0.019*SL	0.231 + 0.019*SL
	t_{PHL}	0.306	0.255 + 0.025*SL	0.261 + 0.024*SL	0.265 + 0.024*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

SCG2

Two 2-ANDs into 2-OR

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	1
x	x	1	1	1
Other States				0

Cell Data

Input Load (SL)				Gate Count
A	B	C	D	
0.8	0.8	0.8	0.8	2.33

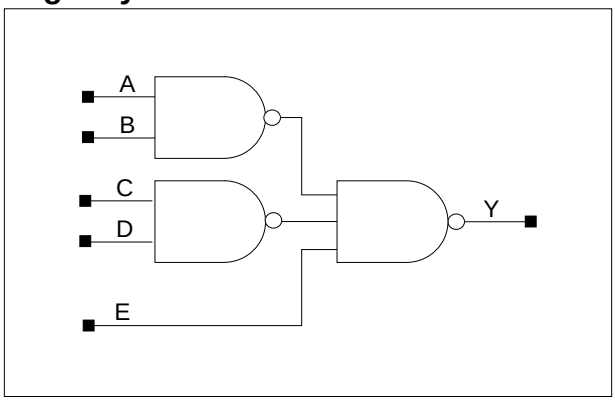
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.153	0.081 + 0.036*SL	0.072 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.140	0.074 + 0.033*SL	0.074 + 0.033*SL	0.049 + 0.033*SL
	t_{PLH}	0.212	0.171 + 0.020*SL	0.183 + 0.018*SL	0.186 + 0.017*SL
	t_{PHL}	0.245	0.200 + 0.022*SL	0.217 + 0.018*SL	0.232 + 0.018*SL
B to Y	t_R	0.153	0.081 + 0.036*SL	0.072 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.145	0.080 + 0.033*SL	0.080 + 0.033*SL	0.050 + 0.033*SL
	t_{PLH}	0.199	0.158 + 0.020*SL	0.169 + 0.018*SL	0.173 + 0.017*SL
	t_{PHL}	0.260	0.215 + 0.023*SL	0.233 + 0.018*SL	0.248 + 0.018*SL
C to Y	t_R	0.166	0.096 + 0.035*SL	0.084 + 0.038*SL	0.054 + 0.039*SL
	t_F	0.142	0.078 + 0.032*SL	0.076 + 0.033*SL	0.049 + 0.033*SL
	t_{PLH}	0.296	0.255 + 0.021*SL	0.267 + 0.018*SL	0.272 + 0.017*SL
	t_{PHL}	0.286	0.241 + 0.022*SL	0.258 + 0.018*SL	0.273 + 0.018*SL
D to Y	t_R	0.166	0.096 + 0.035*SL	0.085 + 0.038*SL	0.054 + 0.039*SL
	t_F	0.146	0.081 + 0.033*SL	0.081 + 0.033*SL	0.050 + 0.033*SL
	t_{PLH}	0.281	0.240 + 0.021*SL	0.252 + 0.018*SL	0.257 + 0.017*SL
	t_{PHL}	0.300	0.254 + 0.023*SL	0.273 + 0.018*SL	0.288 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	1
x	x	1	1	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)					Gate Count
A	B	C	D	E	
0.9	0.9	0.9	0.9	1.1	2.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

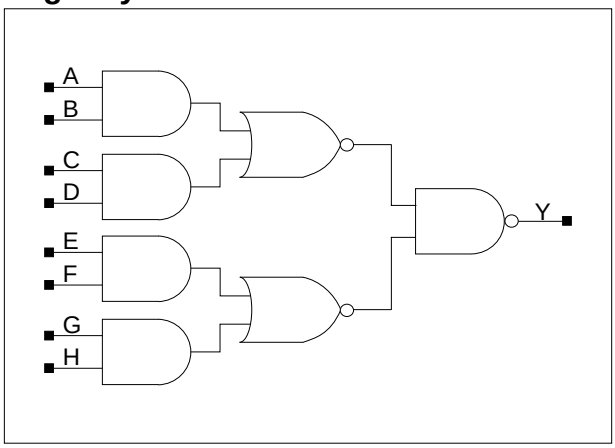
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.182	0.102 + 0.040*SL	0.095 + 0.042*SL	0.082 + 0.042*SL
	t_F	0.217	0.116 + 0.051*SL	0.110 + 0.052*SL	0.103 + 0.052*SL
	t_{PLH}	0.213	0.173 + 0.020*SL	0.178 + 0.019*SL	0.180 + 0.019*SL
	t_{PHL}	0.217	0.168 + 0.025*SL	0.171 + 0.024*SL	0.172 + 0.024*SL
B to Y	t_R	0.182	0.103 + 0.040*SL	0.095 + 0.042*SL	0.082 + 0.042*SL
	t_F	0.218	0.117 + 0.051*SL	0.111 + 0.052*SL	0.104 + 0.052*SL
	t_{PLH}	0.200	0.159 + 0.020*SL	0.165 + 0.019*SL	0.167 + 0.019*SL
	t_{PHL}	0.228	0.179 + 0.025*SL	0.182 + 0.024*SL	0.183 + 0.024*SL
C to Y	t_R	0.202	0.123 + 0.040*SL	0.114 + 0.042*SL	0.100 + 0.042*SL
	t_F	0.218	0.117 + 0.050*SL	0.111 + 0.052*SL	0.104 + 0.052*SL
	t_{PLH}	0.228	0.188 + 0.020*SL	0.191 + 0.019*SL	0.193 + 0.019*SL
	t_{PHL}	0.224	0.175 + 0.025*SL	0.178 + 0.024*SL	0.181 + 0.024*SL
D to Y	t_R	0.202	0.123 + 0.040*SL	0.115 + 0.042*SL	0.100 + 0.042*SL
	t_F	0.219	0.118 + 0.050*SL	0.111 + 0.052*SL	0.104 + 0.052*SL
	t_{PLH}	0.215	0.175 + 0.020*SL	0.179 + 0.019*SL	0.180 + 0.019*SL
	t_{PHL}	0.235	0.186 + 0.025*SL	0.189 + 0.024*SL	0.191 + 0.024*SL
E to Y	t_R	0.242	0.170 + 0.036*SL	0.149 + 0.041*SL	0.115 + 0.042*SL
	t_F	0.230	0.132 + 0.049*SL	0.120 + 0.052*SL	0.104 + 0.052*SL
	t_{PLH}	0.159	0.121 + 0.019*SL	0.122 + 0.019*SL	0.120 + 0.019*SL
	t_{PHL}	0.122	0.072 + 0.025*SL	0.077 + 0.024*SL	0.077 + 0.024*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

SCG4

Two (two 2-ANDs into 2-NOR)s into 2-NAND

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	x	x	x	x	x	x	1
x	x	1	1	x	x	x	x	1
x	x	x	x	1	1	x	x	1
x	x	x	x	x	x	1	1	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
A	B	C	D	E	F	G	H	
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	4.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

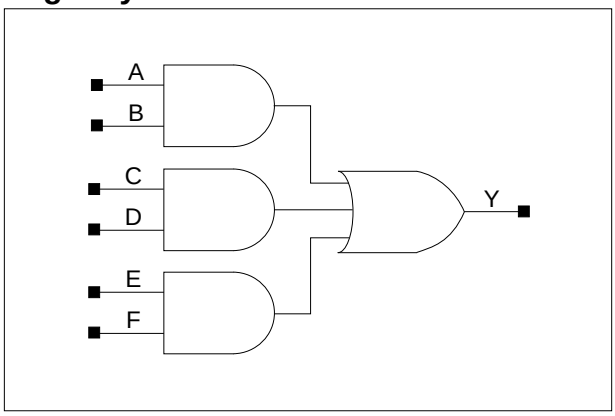
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.161	0.088 + 0.036*SL	0.081 + 0.038*SL	0.058 + 0.039*SL
	t_F	0.180	0.092 + 0.044*SL	0.093 + 0.044*SL	0.069 + 0.044*SL
	t_{PLH}	0.225	0.184 + 0.020*SL	0.195 + 0.018*SL	0.199 + 0.017*SL
	t_{PHL}	0.263	0.212 + 0.025*SL	0.227 + 0.022*SL	0.239 + 0.021*SL
B to Y	t_R	0.161	0.090 + 0.036*SL	0.080 + 0.038*SL	0.058 + 0.039*SL
	t_F	0.186	0.100 + 0.043*SL	0.097 + 0.044*SL	0.070 + 0.044*SL
	t_{PLH}	0.211	0.170 + 0.020*SL	0.181 + 0.018*SL	0.185 + 0.017*SL
	t_{PHL}	0.278	0.227 + 0.025*SL	0.243 + 0.022*SL	0.254 + 0.021*SL
C to Y	t_R	0.175	0.106 + 0.035*SL	0.093 + 0.038*SL	0.063 + 0.039*SL
	t_F	0.183	0.097 + 0.043*SL	0.095 + 0.044*SL	0.070 + 0.044*SL
	t_{PLH}	0.312	0.270 + 0.021*SL	0.282 + 0.018*SL	0.289 + 0.017*SL
	t_{PHL}	0.304	0.254 + 0.025*SL	0.269 + 0.022*SL	0.280 + 0.021*SL
D to Y	t_R	0.175	0.105 + 0.035*SL	0.094 + 0.038*SL	0.063 + 0.039*SL
	t_F	0.187	0.102 + 0.043*SL	0.098 + 0.044*SL	0.071 + 0.044*SL
	t_{PLH}	0.297	0.256 + 0.021*SL	0.268 + 0.018*SL	0.274 + 0.017*SL
	t_{PHL}	0.318	0.267 + 0.025*SL	0.283 + 0.022*SL	0.294 + 0.021*SL
E to Y	t_R	0.177	0.107 + 0.035*SL	0.095 + 0.038*SL	0.072 + 0.039*SL
	t_F	0.173	0.088 + 0.043*SL	0.082 + 0.044*SL	0.065 + 0.045*SL
	t_{PLH}	0.233	0.194 + 0.020*SL	0.202 + 0.018*SL	0.205 + 0.017*SL
	t_{PHL}	0.254	0.207 + 0.024*SL	0.215 + 0.021*SL	0.222 + 0.021*SL
F to Y	t_R	0.177	0.107 + 0.035*SL	0.096 + 0.038*SL	0.072 + 0.039*SL
	t_F	0.177	0.093 + 0.042*SL	0.085 + 0.044*SL	0.065 + 0.045*SL
	t_{PLH}	0.220	0.180 + 0.020*SL	0.189 + 0.018*SL	0.192 + 0.017*SL
	t_{PHL}	0.267	0.220 + 0.024*SL	0.228 + 0.021*SL	0.235 + 0.021*SL
G to Y	t_R	0.195	0.126 + 0.035*SL	0.114 + 0.038*SL	0.082 + 0.039*SL
	t_F	0.175	0.091 + 0.042*SL	0.083 + 0.044*SL	0.065 + 0.045*SL
	t_{PLH}	0.303	0.262 + 0.020*SL	0.273 + 0.018*SL	0.281 + 0.017*SL
	t_{PHL}	0.293	0.246 + 0.024*SL	0.254 + 0.021*SL	0.261 + 0.021*SL
H to Y	t_R	0.196	0.127 + 0.035*SL	0.115 + 0.038*SL	0.082 + 0.039*SL
	t_F	0.179	0.096 + 0.041*SL	0.086 + 0.044*SL	0.066 + 0.045*SL
	t_{PLH}	0.288	0.247 + 0.020*SL	0.258 + 0.018*SL	0.266 + 0.017*SL
	t_{PHL}	0.306	0.259 + 0.024*SL	0.267 + 0.021*SL	0.274 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

SCG5

Three 2-ANDs into 3-OR

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	x	x	x	x	1
x	x	1	1	x	x	1
x	x	x	x	1	1	1
Other States						0

Cell Data

Input Load (SL)						Gate Count
A	B	C	D	E	F	
0.8	0.8	0.8	0.8	0.8	0.8	3.00

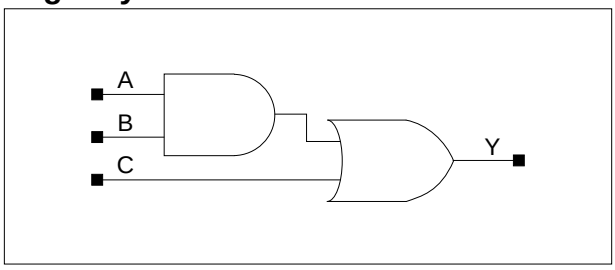
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.163	0.091 + 0.036*SL	0.085 + 0.038*SL	0.056 + 0.039*SL
	t_F	0.177	0.107 + 0.035*SL	0.117 + 0.032*SL	0.096 + 0.033*SL
	t_{PLH}	0.244	0.202 + 0.021*SL	0.216 + 0.018*SL	0.223 + 0.017*SL
	t_{PHL}	0.309	0.257 + 0.026*SL	0.286 + 0.019*SL	0.333 + 0.018*SL
B to Y	t_R	0.163	0.089 + 0.037*SL	0.086 + 0.038*SL	0.056 + 0.039*SL
	t_F	0.183	0.114 + 0.035*SL	0.124 + 0.032*SL	0.099 + 0.033*SL
	t_{PLH}	0.229	0.186 + 0.021*SL	0.201 + 0.018*SL	0.209 + 0.017*SL
	t_{PHL}	0.324	0.270 + 0.027*SL	0.301 + 0.019*SL	0.349 + 0.018*SL
C to Y	t_R	0.178	0.107 + 0.035*SL	0.099 + 0.037*SL	0.061 + 0.039*SL
	t_F	0.184	0.115 + 0.034*SL	0.124 + 0.032*SL	0.098 + 0.033*SL
	t_{PLH}	0.337	0.294 + 0.022*SL	0.310 + 0.018*SL	0.318 + 0.017*SL
	t_{PHL}	0.401	0.348 + 0.026*SL	0.378 + 0.019*SL	0.425 + 0.018*SL
D to Y	t_R	0.179	0.108 + 0.035*SL	0.100 + 0.037*SL	0.061 + 0.039*SL
	t_F	0.191	0.123 + 0.034*SL	0.131 + 0.032*SL	0.101 + 0.033*SL
	t_{PLH}	0.325	0.282 + 0.022*SL	0.298 + 0.018*SL	0.306 + 0.017*SL
	t_{PHL}	0.421	0.368 + 0.027*SL	0.399 + 0.019*SL	0.447 + 0.018*SL
E to Y	t_R	0.194	0.124 + 0.035*SL	0.116 + 0.037*SL	0.075 + 0.038*SL
	t_F	0.185	0.116 + 0.034*SL	0.125 + 0.032*SL	0.098 + 0.033*SL
	t_{PLH}	0.394	0.349 + 0.023*SL	0.367 + 0.018*SL	0.383 + 0.017*SL
	t_{PHL}	0.441	0.388 + 0.026*SL	0.418 + 0.019*SL	0.465 + 0.018*SL
F to Y	t_R	0.194	0.124 + 0.035*SL	0.116 + 0.037*SL	0.075 + 0.038*SL
	t_F	0.192	0.124 + 0.034*SL	0.131 + 0.032*SL	0.101 + 0.033*SL
	t_{PLH}	0.379	0.334 + 0.023*SL	0.353 + 0.018*SL	0.369 + 0.017*SL
	t_{PHL}	0.459	0.405 + 0.027*SL	0.436 + 0.019*SL	0.484 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Logic Symbol



Truth Table

A	B	C	Y
1	1	x	1
x	x	1	1
Other States			0

Cell Data

Input Load (SL)			Gate Count
A	B	C	
0.8	0.8	0.8	1.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

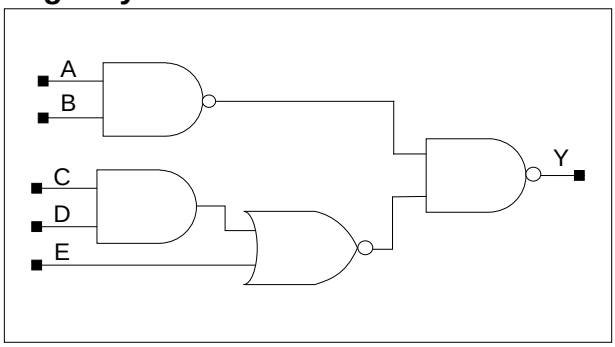
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.150	0.079 + 0.036*SL	0.070 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.135	0.070 + 0.032*SL	0.069 + 0.033*SL	0.045 + 0.033*SL
	t_{PLH}	0.215	0.175 + 0.020*SL	0.184 + 0.018*SL	0.187 + 0.017*SL
	t_{PHL}	0.226	0.183 + 0.022*SL	0.198 + 0.018*SL	0.210 + 0.018*SL
B to Y	t_R	0.150	0.079 + 0.036*SL	0.070 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.138	0.073 + 0.033*SL	0.073 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.201	0.161 + 0.020*SL	0.170 + 0.018*SL	0.173 + 0.017*SL
	t_{PHL}	0.240	0.196 + 0.022*SL	0.212 + 0.018*SL	0.224 + 0.018*SL
C to Y	t_R	0.144	0.075 + 0.035*SL	0.061 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.140	0.075 + 0.032*SL	0.073 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.235	0.197 + 0.019*SL	0.202 + 0.017*SL	0.202 + 0.017*SL
	t_{PHL}	0.267	0.223 + 0.022*SL	0.239 + 0.018*SL	0.251 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

SCG7

2-NAND and (2-AND into 2-NOR) into 2-NAND

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	1
x	x	1	1	x	1
x	x	x	x	1	1
Other States					0

Cell Data

Input Load (SL)					Gate Count
A	B	C	D	E	
0.8	0.8	0.7	0.7	0.8	2.67

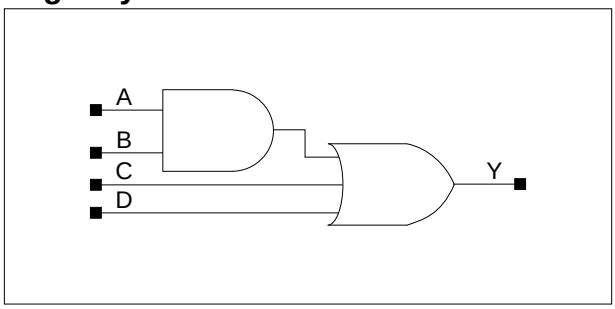
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.154	0.082 + 0.036*SL	0.074 + 0.038*SL	0.056 + 0.039*SL
	t_F	0.159	0.077 + 0.041*SL	0.067 + 0.044*SL	0.057 + 0.044*SL
	t_{PLH}	0.207	0.168 + 0.019*SL	0.176 + 0.018*SL	0.179 + 0.017*SL
	t_{PHL}	0.198	0.153 + 0.022*SL	0.159 + 0.021*SL	0.161 + 0.021*SL
B to Y	t_R	0.155	0.083 + 0.036*SL	0.074 + 0.038*SL	0.057 + 0.039*SL
	t_F	0.160	0.078 + 0.041*SL	0.068 + 0.044*SL	0.057 + 0.044*SL
	t_{PLH}	0.194	0.155 + 0.020*SL	0.163 + 0.018*SL	0.166 + 0.017*SL
	t_{PHL}	0.209	0.164 + 0.022*SL	0.169 + 0.021*SL	0.171 + 0.021*SL
C to Y	t_R	0.176	0.105 + 0.035*SL	0.094 + 0.038*SL	0.072 + 0.039*SL
	t_F	0.168	0.085 + 0.042*SL	0.078 + 0.043*SL	0.061 + 0.044*SL
	t_{PLH}	0.240	0.201 + 0.019*SL	0.209 + 0.017*SL	0.211 + 0.017*SL
	t_{PHL}	0.240	0.195 + 0.023*SL	0.202 + 0.021*SL	0.207 + 0.021*SL
D to Y	t_R	0.176	0.106 + 0.035*SL	0.094 + 0.038*SL	0.072 + 0.039*SL
	t_F	0.171	0.089 + 0.041*SL	0.081 + 0.043*SL	0.062 + 0.044*SL
	t_{PLH}	0.225	0.186 + 0.019*SL	0.194 + 0.017*SL	0.196 + 0.017*SL
	t_{PHL}	0.252	0.206 + 0.023*SL	0.214 + 0.021*SL	0.219 + 0.021*SL
E to Y	t_R	0.168	0.098 + 0.035*SL	0.085 + 0.038*SL	0.069 + 0.039*SL
	t_F	0.173	0.091 + 0.041*SL	0.082 + 0.043*SL	0.062 + 0.044*SL
	t_{PLH}	0.256	0.220 + 0.018*SL	0.223 + 0.017*SL	0.223 + 0.017*SL
	t_{PHL}	0.279	0.233 + 0.023*SL	0.241 + 0.021*SL	0.246 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	1
x	x	1	x	1
x	x	x	1	1
	Other States			0

Cell Data

Input Load (SL)				Gate Count
A	B	C	D	
0.7	0.8	0.8	0.8	2.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

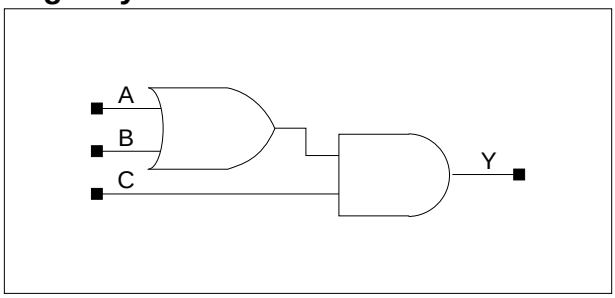
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.153	0.081 + 0.036*SL	0.074 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.159	0.089 + 0.035*SL	0.098 + 0.033*SL	0.078 + 0.033*SL
	t_{PLH}	0.231	0.191 + 0.020*SL	0.202 + 0.018*SL	0.206 + 0.017*SL
	t_{PHL}	0.267	0.217 + 0.025*SL	0.241 + 0.019*SL	0.277 + 0.018*SL
B to Y	t_R	0.154	0.083 + 0.036*SL	0.074 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.163	0.095 + 0.034*SL	0.102 + 0.033*SL	0.080 + 0.033*SL
	t_{PLH}	0.217	0.176 + 0.020*SL	0.187 + 0.018*SL	0.192 + 0.017*SL
	t_{PHL}	0.280	0.230 + 0.025*SL	0.255 + 0.019*SL	0.292 + 0.018*SL
C to Y	t_R	0.148	0.078 + 0.035*SL	0.065 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.169	0.101 + 0.034*SL	0.108 + 0.032*SL	0.081 + 0.033*SL
	t_{PLH}	0.253	0.215 + 0.019*SL	0.221 + 0.017*SL	0.221 + 0.017*SL
	t_{PHL}	0.349	0.299 + 0.025*SL	0.324 + 0.019*SL	0.361 + 0.018*SL
D to Y	t_R	0.154	0.085 + 0.034*SL	0.071 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.169	0.102 + 0.034*SL	0.107 + 0.032*SL	0.081 + 0.033*SL
	t_{PLH}	0.272	0.233 + 0.020*SL	0.240 + 0.018*SL	0.243 + 0.017*SL
	t_{PHL}	0.361	0.311 + 0.025*SL	0.336 + 0.019*SL	0.373 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 36, *Group3 : 36 < SL

SCG9

2-OR into 2-AND

Logic Symbol



Truth Table

A	B	C	Y
0	0	x	0
x	x	0	0
Other States			1

Cell Data

Input Load (SL)			Gate Count
A	B	C	
0.7	0.8	0.8	1.67

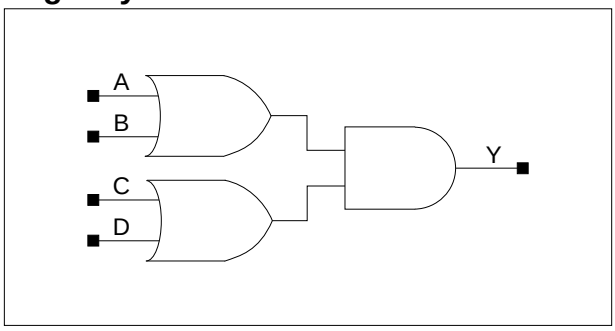
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.153	0.082 + 0.036*SL	0.073 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.136	0.071 + 0.033*SL	0.070 + 0.033*SL	0.045 + 0.033*SL
	t_{PLH}	0.218	0.178 + 0.020*SL	0.189 + 0.018*SL	0.192 + 0.017*SL
	t_{PHL}	0.237	0.193 + 0.022*SL	0.208 + 0.018*SL	0.219 + 0.018*SL
B to Y	t_R	0.160	0.089 + 0.036*SL	0.080 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.137	0.071 + 0.033*SL	0.071 + 0.033*SL	0.045 + 0.033*SL
	t_{PLH}	0.259	0.218 + 0.021*SL	0.230 + 0.018*SL	0.234 + 0.017*SL
	t_{PHL}	0.240	0.196 + 0.022*SL	0.212 + 0.018*SL	0.222 + 0.018*SL
C to Y	t_R	0.161	0.090 + 0.035*SL	0.080 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.130	0.067 + 0.032*SL	0.062 + 0.033*SL	0.038 + 0.034*SL
	t_{PLH}	0.256	0.215 + 0.021*SL	0.227 + 0.018*SL	0.231 + 0.017*SL
	t_{PHL}	0.206	0.163 + 0.021*SL	0.176 + 0.018*SL	0.183 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	0
x	x	0	0	0
Other States				1

Cell Data

Input Load (SL)				Gate Count
A	B	C	D	
0.8	0.8	0.8	0.8	2.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

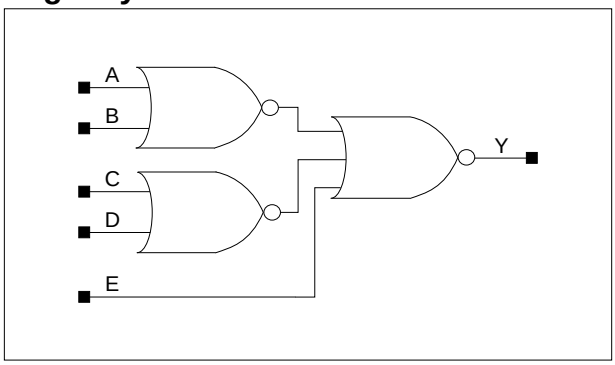
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.161	0.089 + 0.036*SL	0.081 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.153	0.086 + 0.033*SL	0.090 + 0.032*SL	0.060 + 0.033*SL
	t_{PLH}	0.270	0.229 + 0.021*SL	0.241 + 0.018*SL	0.246 + 0.017*SL
	t_{PHL}	0.245	0.198 + 0.024*SL	0.220 + 0.018*SL	0.243 + 0.018*SL
B to Y	t_R	0.170	0.099 + 0.035*SL	0.090 + 0.038*SL	0.055 + 0.039*SL
	t_F	0.153	0.086 + 0.033*SL	0.090 + 0.032*SL	0.060 + 0.033*SL
	t_{PLH}	0.314	0.272 + 0.021*SL	0.285 + 0.018*SL	0.290 + 0.017*SL
	t_{PHL}	0.249	0.201 + 0.024*SL	0.224 + 0.018*SL	0.247 + 0.018*SL
C to Y	t_R	0.161	0.089 + 0.036*SL	0.081 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.161	0.095 + 0.033*SL	0.098 + 0.032*SL	0.063 + 0.033*SL
	t_{PLH}	0.271	0.229 + 0.021*SL	0.242 + 0.018*SL	0.246 + 0.017*SL
	t_{PHL}	0.272	0.223 + 0.024*SL	0.247 + 0.018*SL	0.272 + 0.018*SL
D to Y	t_R	0.170	0.099 + 0.035*SL	0.090 + 0.038*SL	0.055 + 0.039*SL
	t_F	0.161	0.096 + 0.033*SL	0.098 + 0.032*SL	0.064 + 0.033*SL
	t_{PLH}	0.314	0.272 + 0.021*SL	0.286 + 0.018*SL	0.291 + 0.017*SL
	t_{PHL}	0.275	0.226 + 0.024*SL	0.251 + 0.018*SL	0.275 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

SCG11

Two 2-NORs into 3-NOR

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	x	x	x	0
x	x	0	0	x	0
x	x	x	x	1	0
Other States					1

Cell Data

Input Load (SL)					Gate Count
A	B	C	D	E	
0.9	0.9	0.9	0.9	0.9	2.67

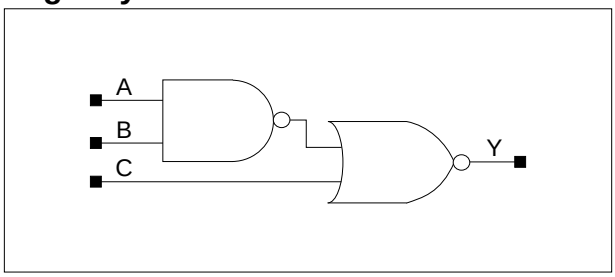
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.410	0.192 + 0.109*SL	0.193 + 0.109*SL	0.198 + 0.108*SL
	t_F	0.160	0.081 + 0.039*SL	0.076 + 0.040*SL	0.056 + 0.041*SL
	t_{PLH}	0.218	0.122 + 0.048*SL	0.123 + 0.048*SL	0.125 + 0.048*SL
	t_{PHL}	0.262	0.212 + 0.025*SL	0.224 + 0.022*SL	0.231 + 0.022*SL
B to Y	t_R	0.411	0.194 + 0.109*SL	0.194 + 0.109*SL	0.198 + 0.108*SL
	t_F	0.160	0.082 + 0.039*SL	0.077 + 0.040*SL	0.056 + 0.041*SL
	t_{PLH}	0.240	0.144 + 0.048*SL	0.144 + 0.048*SL	0.146 + 0.048*SL
	t_{PHL}	0.261	0.211 + 0.025*SL	0.223 + 0.022*SL	0.230 + 0.022*SL
C to Y	t_R	0.422	0.208 + 0.107*SL	0.201 + 0.108*SL	0.198 + 0.108*SL
	t_F	0.196	0.121 + 0.037*SL	0.114 + 0.039*SL	0.089 + 0.040*SL
	t_{PLH}	0.274	0.177 + 0.049*SL	0.181 + 0.048*SL	0.185 + 0.048*SL
	t_{PHL}	0.293	0.244 + 0.024*SL	0.256 + 0.021*SL	0.264 + 0.021*SL
D to Y	t_R	0.422	0.209 + 0.107*SL	0.202 + 0.108*SL	0.198 + 0.108*SL
	t_F	0.196	0.122 + 0.037*SL	0.115 + 0.039*SL	0.089 + 0.040*SL
	t_{PLH}	0.293	0.196 + 0.049*SL	0.200 + 0.048*SL	0.204 + 0.048*SL
	t_{PHL}	0.293	0.244 + 0.024*SL	0.256 + 0.021*SL	0.264 + 0.021*SL
E to Y	t_R	0.430	0.221 + 0.105*SL	0.207 + 0.108*SL	0.198 + 0.108*SL
	t_F	0.236	0.163 + 0.036*SL	0.149 + 0.040*SL	0.115 + 0.041*SL
	t_{PLH}	0.249	0.153 + 0.048*SL	0.155 + 0.048*SL	0.157 + 0.048*SL
	t_{PHL}	0.153	0.105 + 0.024*SL	0.112 + 0.022*SL	0.122 + 0.022*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Logic Symbol



Truth Table

A	B	C	Y
1	1	0	1
Other States			0

Cell Data

Input Load (SL)			Gate Count
A	B	C	
0.9	0.9	1.0	1.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

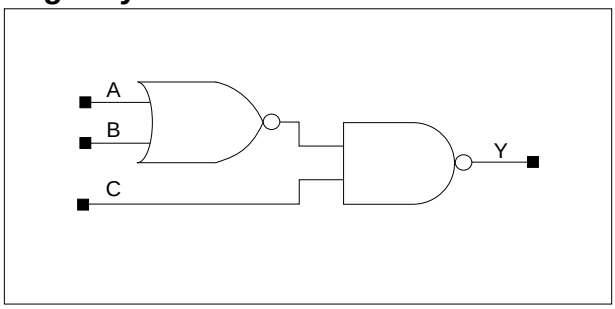
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.260	0.118 + 0.071*SL	0.110 + 0.073*SL	0.103 + 0.073*SL
	t_F	0.118	0.055 + 0.031*SL	0.048 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.221	0.155 + 0.033*SL	0.158 + 0.032*SL	0.159 + 0.032*SL
	t_{PHL}	0.187	0.148 + 0.019*SL	0.155 + 0.018*SL	0.157 + 0.018*SL
B to Y	t_R	0.260	0.118 + 0.071*SL	0.110 + 0.073*SL	0.103 + 0.073*SL
	t_F	0.119	0.056 + 0.031*SL	0.049 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.210	0.144 + 0.033*SL	0.147 + 0.032*SL	0.148 + 0.032*SL
	t_{PHL}	0.200	0.161 + 0.020*SL	0.168 + 0.018*SL	0.170 + 0.018*SL
C to Y	t_R	0.272	0.134 + 0.069*SL	0.118 + 0.073*SL	0.103 + 0.073*SL
	t_F	0.179	0.124 + 0.027*SL	0.104 + 0.032*SL	0.061 + 0.034*SL
	t_{PLH}	0.165	0.099 + 0.033*SL	0.102 + 0.032*SL	0.101 + 0.032*SL
	t_{PHL}	0.112	0.071 + 0.021*SL	0.083 + 0.018*SL	0.083 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

SCG13

2-NOR into 2-NAND

Logic Symbol



Truth Table

A	B	C	Y
0	0	1	0
Other States			1

Cell Data

Input Load (SL)			Gate Count
A	B	C	
0.8	0.8	1.1	1.67

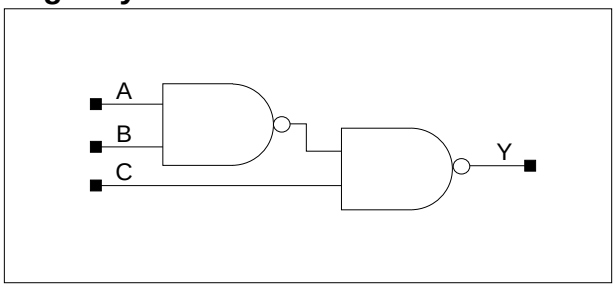
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.145	0.073 + 0.036*SL	0.064 + 0.038*SL	0.054 + 0.039*SL
	t_F	0.171	0.085 + 0.043*SL	0.084 + 0.043*SL	0.063 + 0.044*SL
	t_{PLH}	0.190	0.153 + 0.018*SL	0.157 + 0.017*SL	0.157 + 0.017*SL
	t_{PHL}	0.235	0.187 + 0.024*SL	0.198 + 0.021*SL	0.204 + 0.021*SL
B to Y	t_R	0.152	0.081 + 0.035*SL	0.069 + 0.038*SL	0.055 + 0.039*SL
	t_F	0.172	0.087 + 0.043*SL	0.084 + 0.043*SL	0.063 + 0.044*SL
	t_{PLH}	0.224	0.186 + 0.019*SL	0.192 + 0.017*SL	0.193 + 0.017*SL
	t_{PHL}	0.239	0.191 + 0.024*SL	0.203 + 0.021*SL	0.209 + 0.021*SL
C to Y	t_R	0.191	0.129 + 0.031*SL	0.103 + 0.038*SL	0.066 + 0.039*SL
	t_F	0.178	0.101 + 0.038*SL	0.082 + 0.043*SL	0.059 + 0.044*SL
	t_{PLH}	0.128	0.090 + 0.019*SL	0.097 + 0.017*SL	0.093 + 0.017*SL
	t_{PHL}	0.098	0.052 + 0.023*SL	0.060 + 0.021*SL	0.060 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	x	1	0
x	0	1	0
Other States			1

Cell Data

Input Load (SL)			Gate Count
A	B	C	
0.8	0.8	1.1	1.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

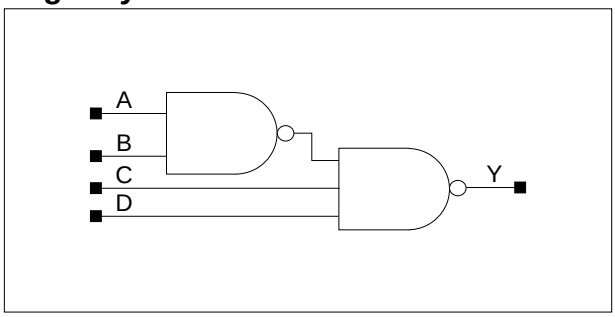
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.153	0.081 + 0.036*SL	0.072 + 0.038*SL	0.056 + 0.039*SL
	t_F	0.161	0.077 + 0.042*SL	0.069 + 0.044*SL	0.058 + 0.044*SL
	t_{PLH}	0.192	0.154 + 0.019*SL	0.161 + 0.017*SL	0.163 + 0.017*SL
	t_{PHL}	0.206	0.161 + 0.022*SL	0.167 + 0.021*SL	0.168 + 0.021*SL
B to Y	t_R	0.153	0.080 + 0.036*SL	0.072 + 0.038*SL	0.056 + 0.039*SL
	t_F	0.161	0.078 + 0.042*SL	0.070 + 0.044*SL	0.058 + 0.044*SL
	t_{PLH}	0.180	0.141 + 0.019*SL	0.149 + 0.018*SL	0.152 + 0.017*SL
	t_{PHL}	0.219	0.174 + 0.022*SL	0.179 + 0.021*SL	0.181 + 0.021*SL
C to Y	t_R	0.190	0.127 + 0.032*SL	0.103 + 0.038*SL	0.065 + 0.039*SL
	t_F	0.178	0.101 + 0.039*SL	0.081 + 0.044*SL	0.058 + 0.044*SL
	t_{PLH}	0.128	0.089 + 0.019*SL	0.097 + 0.017*SL	0.092 + 0.017*SL
	t_{PHL}	0.098	0.052 + 0.023*SL	0.060 + 0.021*SL	0.060 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

SCG15

2-NAND into 3-NAND

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	1	1	0
x	0	1	1	0
Other States				1

Cell Data

Input Load (SL)				Gate Count
A	B	C	D	
0.8	0.9	1.1	1.1	2.00

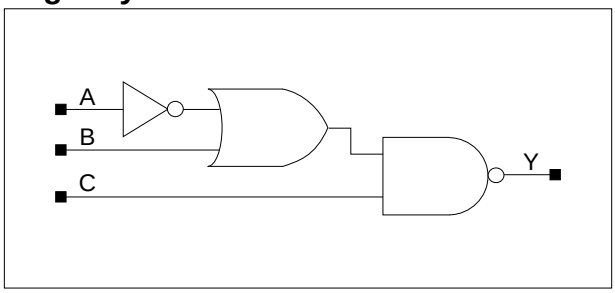
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.183	0.104 + 0.040*SL	0.096 + 0.042*SL	0.082 + 0.042*SL
	t_F	0.219	0.118 + 0.051*SL	0.111 + 0.052*SL	0.104 + 0.052*SL
	t_{PLH}	0.215	0.174 + 0.020*SL	0.179 + 0.019*SL	0.181 + 0.019*SL
	t_{PHL}	0.222	0.173 + 0.025*SL	0.176 + 0.024*SL	0.178 + 0.024*SL
B to Y	t_R	0.183	0.103 + 0.040*SL	0.096 + 0.042*SL	0.082 + 0.042*SL
	t_F	0.220	0.120 + 0.050*SL	0.112 + 0.052*SL	0.104 + 0.052*SL
	t_{PLH}	0.202	0.161 + 0.021*SL	0.167 + 0.019*SL	0.169 + 0.019*SL
	t_{PHL}	0.234	0.185 + 0.025*SL	0.188 + 0.024*SL	0.189 + 0.024*SL
C to Y	t_R	0.220	0.148 + 0.036*SL	0.126 + 0.041*SL	0.096 + 0.042*SL
	t_F	0.237	0.141 + 0.048*SL	0.125 + 0.052*SL	0.104 + 0.052*SL
	t_{PLH}	0.148	0.109 + 0.020*SL	0.112 + 0.019*SL	0.109 + 0.019*SL
	t_{PHL}	0.128	0.077 + 0.025*SL	0.083 + 0.024*SL	0.083 + 0.024*SL
D to Y	t_R	0.242	0.170 + 0.036*SL	0.149 + 0.041*SL	0.115 + 0.042*SL
	t_F	0.229	0.132 + 0.049*SL	0.119 + 0.052*SL	0.104 + 0.052*SL
	t_{PLH}	0.160	0.122 + 0.019*SL	0.122 + 0.019*SL	0.120 + 0.019*SL
	t_{PHL}	0.122	0.073 + 0.025*SL	0.077 + 0.024*SL	0.077 + 0.024*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	x	1	0
x	1	1	0
Other States			1

Cell Data

Input Load (SL)			Gate Count
A	B	C	
0.8	1.0	1.0	1.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

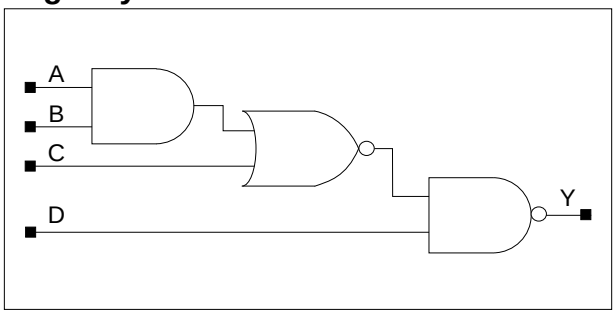
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.264	0.119 + 0.072*SL	0.113 + 0.074*SL	0.111 + 0.074*SL
	t_F	0.203	0.085 + 0.059*SL	0.078 + 0.061*SL	0.073 + 0.061*SL
	t_{PLH}	0.207	0.141 + 0.033*SL	0.142 + 0.033*SL	0.144 + 0.033*SL
	t_{PHL}	0.223	0.163 + 0.030*SL	0.167 + 0.029*SL	0.170 + 0.029*SL
B to Y	t_R	0.281	0.143 + 0.069*SL	0.126 + 0.074*SL	0.111 + 0.074*SL
	t_F	0.277	0.168 + 0.055*SL	0.143 + 0.061*SL	0.118 + 0.062*SL
	t_{PLH}	0.168	0.101 + 0.034*SL	0.105 + 0.033*SL	0.105 + 0.033*SL
	t_{PHL}	0.174	0.114 + 0.030*SL	0.116 + 0.030*SL	0.117 + 0.029*SL
C to Y	t_R	0.195	0.131 + 0.032*SL	0.108 + 0.038*SL	0.071 + 0.039*SL
	t_F	0.262	0.147 + 0.058*SL	0.132 + 0.061*SL	0.118 + 0.062*SL
	t_{PLH}	0.130	0.092 + 0.019*SL	0.099 + 0.017*SL	0.096 + 0.017*SL
	t_{PHL}	0.171	0.110 + 0.030*SL	0.113 + 0.030*SL	0.117 + 0.030*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 36, *Group3 : 36 < SL

SCG17

2-AND into 2-NOR into 2-NAND

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	0	1	0
x	0	0	1	0
Other States				1

Cell Data

Input Load (SL)				Gate Count
A	B	C	D	
0.8	0.8	0.8	1.1	2.00

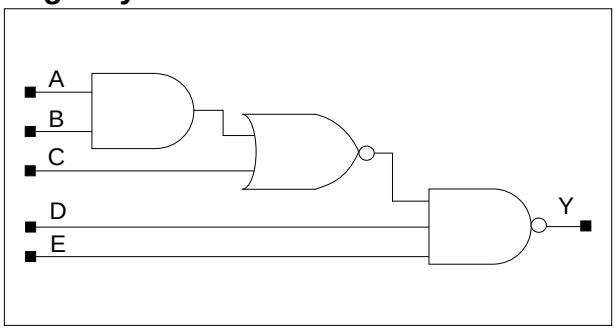
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.159	0.087 + 0.036*SL	0.079 + 0.038*SL	0.058 + 0.039*SL
	t_F	0.175	0.090 + 0.043*SL	0.088 + 0.043*SL	0.066 + 0.044*SL
	t_{PLH}	0.226	0.187 + 0.020*SL	0.196 + 0.018*SL	0.199 + 0.017*SL
	t_{PHL}	0.247	0.198 + 0.025*SL	0.211 + 0.021*SL	0.220 + 0.021*SL
B to Y	t_R	0.160	0.089 + 0.035*SL	0.079 + 0.038*SL	0.058 + 0.039*SL
	t_F	0.178	0.093 + 0.043*SL	0.092 + 0.043*SL	0.068 + 0.044*SL
	t_{PLH}	0.212	0.172 + 0.020*SL	0.182 + 0.018*SL	0.186 + 0.017*SL
	t_{PHL}	0.261	0.212 + 0.025*SL	0.226 + 0.021*SL	0.235 + 0.021*SL
C to Y	t_R	0.152	0.082 + 0.035*SL	0.070 + 0.038*SL	0.055 + 0.039*SL
	t_F	0.181	0.097 + 0.042*SL	0.093 + 0.043*SL	0.068 + 0.044*SL
	t_{PLH}	0.244	0.207 + 0.019*SL	0.211 + 0.017*SL	0.213 + 0.017*SL
	t_{PHL}	0.287	0.238 + 0.025*SL	0.252 + 0.021*SL	0.262 + 0.021*SL
D to Y	t_R	0.190	0.127 + 0.031*SL	0.102 + 0.038*SL	0.065 + 0.039*SL
	t_F	0.177	0.100 + 0.038*SL	0.081 + 0.043*SL	0.059 + 0.044*SL
	t_{PLH}	0.127	0.089 + 0.019*SL	0.096 + 0.017*SL	0.092 + 0.017*SL
	t_{PHL}	0.097	0.051 + 0.023*SL	0.060 + 0.021*SL	0.060 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	0	1	1	0
x	0	0	1	1	0
Other States					1

Cell Data

Input Load (SL)					Gate Count
A	B	C	D	E	
0.7	0.8	0.8	1.1	1.1	2.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

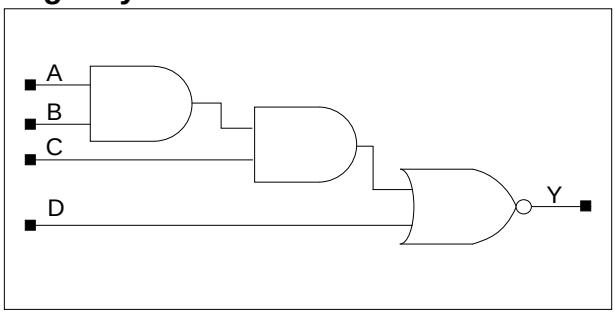
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.191	0.112 + 0.040*SL	0.104 + 0.042*SL	0.085 + 0.042*SL
	t_F	0.234	0.133 + 0.051*SL	0.131 + 0.051*SL	0.111 + 0.052*SL
	t_{PLH}	0.255	0.213 + 0.021*SL	0.221 + 0.019*SL	0.224 + 0.019*SL
	t_{PHL}	0.268	0.215 + 0.026*SL	0.226 + 0.024*SL	0.233 + 0.024*SL
B to Y	t_R	0.191	0.112 + 0.040*SL	0.103 + 0.042*SL	0.085 + 0.042*SL
	t_F	0.237	0.136 + 0.051*SL	0.133 + 0.051*SL	0.112 + 0.052*SL
	t_{PLH}	0.241	0.199 + 0.021*SL	0.207 + 0.019*SL	0.210 + 0.019*SL
	t_{PHL}	0.282	0.228 + 0.027*SL	0.239 + 0.024*SL	0.247 + 0.024*SL
C to Y	t_R	0.183	0.104 + 0.039*SL	0.094 + 0.042*SL	0.081 + 0.042*SL
	t_F	0.238	0.137 + 0.050*SL	0.134 + 0.051*SL	0.112 + 0.052*SL
	t_{PLH}	0.272	0.232 + 0.020*SL	0.236 + 0.019*SL	0.237 + 0.019*SL
	t_{PHL}	0.309	0.256 + 0.027*SL	0.266 + 0.024*SL	0.274 + 0.024*SL
D to Y	t_R	0.220	0.149 + 0.036*SL	0.127 + 0.041*SL	0.096 + 0.042*SL
	t_F	0.236	0.140 + 0.048*SL	0.125 + 0.051*SL	0.105 + 0.052*SL
	t_{PLH}	0.149	0.109 + 0.020*SL	0.112 + 0.019*SL	0.109 + 0.019*SL
	t_{PHL}	0.128	0.077 + 0.025*SL	0.083 + 0.024*SL	0.084 + 0.024*SL
E to Y	t_R	0.244	0.173 + 0.036*SL	0.150 + 0.041*SL	0.117 + 0.042*SL
	t_F	0.228	0.131 + 0.049*SL	0.119 + 0.052*SL	0.105 + 0.052*SL
	t_{PLH}	0.160	0.122 + 0.019*SL	0.123 + 0.019*SL	0.121 + 0.019*SL
	t_{PHL}	0.123	0.073 + 0.025*SL	0.078 + 0.024*SL	0.079 + 0.024*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

SCG19

2-AND into 2-AND into 2-NOR

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	1	x	0
x	x	x	1	0
Other States				1

Cell Data

Input Load (SL)				Gate Count
A	B	C	D	
0.8	0.8	1.0	1.0	2.33

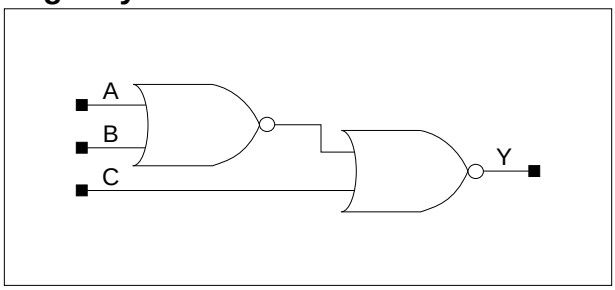
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.267	0.121 + 0.073*SL	0.119 + 0.074*SL	0.120 + 0.074*SL
	t_F	0.211	0.086 + 0.063*SL	0.080 + 0.064*SL	0.075 + 0.064*SL
	t_{PLH}	0.286	0.221 + 0.033*SL	0.221 + 0.032*SL	0.223 + 0.032*SL
	t_{PHL}	0.291	0.227 + 0.032*SL	0.231 + 0.031*SL	0.233 + 0.031*SL
B to Y	t_R	0.268	0.122 + 0.073*SL	0.119 + 0.074*SL	0.120 + 0.074*SL
	t_F	0.211	0.085 + 0.063*SL	0.080 + 0.064*SL	0.075 + 0.064*SL
	t_{PLH}	0.300	0.234 + 0.033*SL	0.235 + 0.032*SL	0.237 + 0.032*SL
	t_{PHL}	0.279	0.215 + 0.032*SL	0.219 + 0.031*SL	0.222 + 0.031*SL
C to Y	t_R	0.315	0.180 + 0.068*SL	0.153 + 0.074*SL	0.136 + 0.075*SL
	t_F	0.227	0.108 + 0.059*SL	0.089 + 0.064*SL	0.076 + 0.064*SL
	t_{PLH}	0.173	0.109 + 0.032*SL	0.106 + 0.033*SL	0.102 + 0.033*SL
	t_{PHL}	0.138	0.074 + 0.032*SL	0.079 + 0.031*SL	0.079 + 0.031*SL
D to Y	t_R	0.305	0.164 + 0.071*SL	0.149 + 0.074*SL	0.136 + 0.075*SL
	t_F	0.223	0.152 + 0.036*SL	0.138 + 0.039*SL	0.109 + 0.040*SL
	t_{PLH}	0.196	0.130 + 0.033*SL	0.131 + 0.033*SL	0.132 + 0.033*SL
	t_{PHL}	0.164	0.120 + 0.022*SL	0.123 + 0.021*SL	0.126 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Logic Symbol



Truth Table

A	B	C	Y
1	x	0	1
x	1	0	1
Other States			0

Cell Data

Input Load (SL)			Gate Count
A	B	C	
0.8	0.9	1.1	1.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

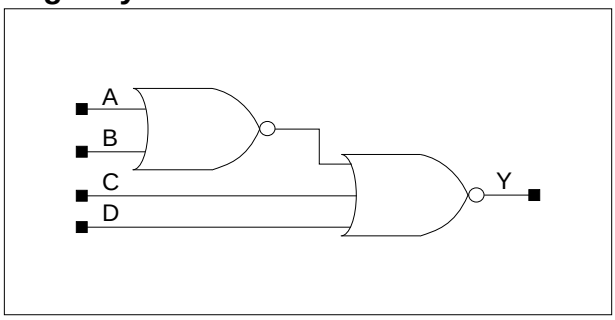
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.257	0.114 + 0.072*SL	0.108 + 0.073*SL	0.106 + 0.073*SL
	t_F	0.127	0.068 + 0.029*SL	0.067 + 0.030*SL	0.046 + 0.030*SL
	t_{PLH}	0.200	0.136 + 0.032*SL	0.136 + 0.032*SL	0.138 + 0.032*SL
	t_{PHL}	0.231	0.191 + 0.020*SL	0.206 + 0.016*SL	0.216 + 0.016*SL
B to Y	t_R	0.259	0.116 + 0.071*SL	0.109 + 0.073*SL	0.106 + 0.073*SL
	t_F	0.128	0.069 + 0.030*SL	0.070 + 0.030*SL	0.046 + 0.030*SL
	t_{PLH}	0.226	0.162 + 0.032*SL	0.161 + 0.032*SL	0.163 + 0.032*SL
	t_{PHL}	0.232	0.192 + 0.020*SL	0.207 + 0.016*SL	0.218 + 0.016*SL
C to Y	t_R	0.274	0.137 + 0.069*SL	0.121 + 0.073*SL	0.106 + 0.073*SL
	t_F	0.170	0.120 + 0.025*SL	0.104 + 0.029*SL	0.057 + 0.030*SL
	t_{PLH}	0.167	0.102 + 0.033*SL	0.104 + 0.032*SL	0.102 + 0.032*SL
	t_{PHL}	0.104	0.066 + 0.019*SL	0.079 + 0.016*SL	0.080 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

SCG21

2-NOR into 3-NOR

Logic Symbol



Truth Table

A	B	C	D	Y
1	x	0	0	1
x	1	0	0	1
Other States				0

Cell Data

Input Load (SL)				Gate Count
A	B	C	D	
0.8	0.8	1.0	1.0	2.00

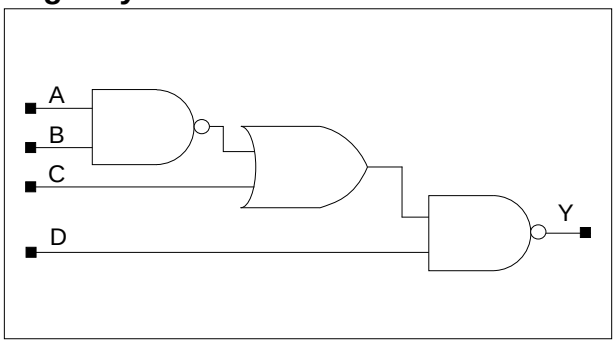
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.420	0.203 + 0.109*SL	0.203 + 0.109*SL	0.207 + 0.108*SL
	t_F	0.152	0.084 + 0.034*SL	0.080 + 0.035*SL	0.057 + 0.035*SL
	t_{PLH}	0.236	0.140 + 0.048*SL	0.141 + 0.048*SL	0.144 + 0.048*SL
	t_{PHL}	0.260	0.215 + 0.023*SL	0.229 + 0.019*SL	0.238 + 0.019*SL
B to Y	t_R	0.421	0.204 + 0.108*SL	0.204 + 0.109*SL	0.207 + 0.108*SL
	t_F	0.152	0.085 + 0.034*SL	0.080 + 0.035*SL	0.057 + 0.035*SL
	t_{PLH}	0.258	0.162 + 0.048*SL	0.162 + 0.048*SL	0.165 + 0.048*SL
	t_{PHL}	0.260	0.215 + 0.023*SL	0.230 + 0.019*SL	0.239 + 0.019*SL
C to Y	t_R	0.442	0.232 + 0.105*SL	0.219 + 0.108*SL	0.207 + 0.108*SL
	t_F	0.188	0.129 + 0.030*SL	0.110 + 0.034*SL	0.072 + 0.036*SL
	t_{PLH}	0.240	0.144 + 0.048*SL	0.144 + 0.048*SL	0.145 + 0.048*SL
	t_{PHL}	0.126	0.084 + 0.021*SL	0.093 + 0.019*SL	0.094 + 0.019*SL
D to Y	t_R	0.438	0.228 + 0.105*SL	0.215 + 0.108*SL	0.207 + 0.108*SL
	t_F	0.218	0.156 + 0.031*SL	0.142 + 0.034*SL	0.105 + 0.035*SL
	t_{PLH}	0.253	0.157 + 0.048*SL	0.159 + 0.048*SL	0.162 + 0.048*SL
	t_{PHL}	0.136	0.094 + 0.021*SL	0.102 + 0.019*SL	0.111 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	0	x	1
x	x	x	0	1
Other States				0

Cell Data

Input Load (SL)				Gate Count
A	B	C	D	
0.8	0.8	1.0	1.0	2.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

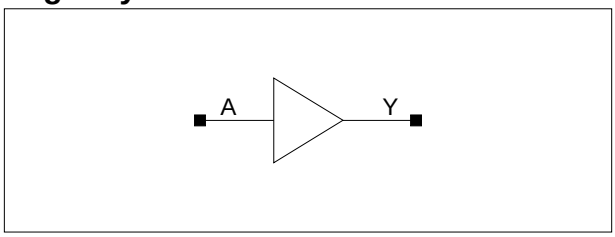
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.272	0.128 + 0.072*SL	0.120 + 0.074*SL	0.114 + 0.074*SL
	t_F	0.205	0.087 + 0.059*SL	0.080 + 0.061*SL	0.074 + 0.061*SL
	t_{PLH}	0.230	0.162 + 0.034*SL	0.166 + 0.033*SL	0.168 + 0.033*SL
	t_{PHL}	0.234	0.173 + 0.030*SL	0.178 + 0.029*SL	0.180 + 0.029*SL
B to Y	t_R	0.272	0.128 + 0.072*SL	0.120 + 0.074*SL	0.114 + 0.074*SL
	t_F	0.206	0.089 + 0.059*SL	0.082 + 0.061*SL	0.074 + 0.061*SL
	t_{PLH}	0.219	0.151 + 0.034*SL	0.155 + 0.033*SL	0.157 + 0.033*SL
	t_{PHL}	0.247	0.186 + 0.030*SL	0.191 + 0.029*SL	0.194 + 0.029*SL
C to Y	t_R	0.284	0.145 + 0.069*SL	0.129 + 0.074*SL	0.114 + 0.074*SL
	t_F	0.279	0.169 + 0.055*SL	0.144 + 0.061*SL	0.119 + 0.062*SL
	t_{PLH}	0.170	0.102 + 0.034*SL	0.107 + 0.033*SL	0.107 + 0.033*SL
	t_{PHL}	0.175	0.115 + 0.030*SL	0.117 + 0.030*SL	0.118 + 0.030*SL
D to Y	t_R	0.195	0.131 + 0.032*SL	0.108 + 0.038*SL	0.072 + 0.039*SL
	t_F	0.264	0.149 + 0.058*SL	0.134 + 0.061*SL	0.119 + 0.062*SL
	t_{PLH}	0.130	0.092 + 0.019*SL	0.099 + 0.017*SL	0.096 + 0.017*SL
	t_{PHL}	0.171	0.110 + 0.030*SL	0.113 + 0.030*SL	0.117 + 0.030*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

DL1D2/DL1D4

1ns Delay Cell with 2X/4X Drive

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)		Gate Count	
DL1D2	*DL1D4*	*DL1D2*	*DL1D4*
A	A	3.33	4.00
0.6	0.6		

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

DL1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.101	0.067 + 0.017*SL	0.057 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.098	0.054 + 0.022*SL	0.049 + 0.023*SL	0.032 + 0.024*SL
	t_{PLH}	0.968	0.946 + 0.011*SL	0.954 + 0.009*SL	0.957 + 0.009*SL
	t_{PHL}	0.963	0.934 + 0.014*SL	0.942 + 0.012*SL	0.946 + 0.012*SL

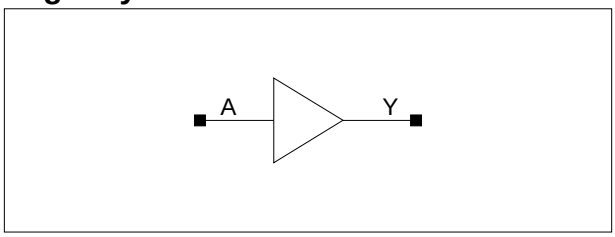
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

DL1D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.086 + 0.008*SL	0.082 + 0.009*SL	0.051 + 0.010*SL
	t_F	0.086	0.065 + 0.010*SL	0.064 + 0.011*SL	0.040 + 0.011*SL
	t_{PLH}	1.008	0.994 + 0.007*SL	1.003 + 0.005*SL	1.016 + 0.004*SL
	t_{PHL}	0.991	0.975 + 0.008*SL	0.983 + 0.006*SL	0.994 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)		Gate Count	
DL2D2	*DL2D4*	*DL2D2*	*DL2D4*
A	A	3.67	4.33
0.6	0.6		

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

DL2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.069 + 0.017*SL	0.060 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.102	0.059 + 0.022*SL	0.053 + 0.023*SL	0.032 + 0.024*SL
	t_{PLH}	1.939	1.918 + 0.011*SL	1.925 + 0.009*SL	1.928 + 0.009*SL
	t_{PHL}	1.941	1.912 + 0.014*SL	1.920 + 0.012*SL	1.924 + 0.012*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

DL2D4

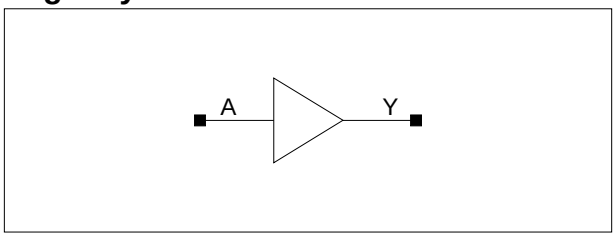
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.105	0.088 + 0.009*SL	0.085 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.090	0.069 + 0.011*SL	0.069 + 0.011*SL	0.042 + 0.011*SL
	t_{PLH}	1.980	1.967 + 0.007*SL	1.976 + 0.005*SL	1.989 + 0.004*SL
	t_{PHL}	1.973	1.957 + 0.008*SL	1.965 + 0.006*SL	1.977 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

DL3D2/DL3D4

3ns Delay Cell with 2X/4X Drive

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)		Gate Count	
DL3D2	*DL3D4*	*DL3D2*	*DL3D4*
A	A	4.67	5.33
0.6	0.6		

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

DL3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.101	0.066 + 0.018*SL	0.059 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.101	0.055 + 0.023*SL	0.053 + 0.023*SL	0.032 + 0.024*SL
	t_{PLH}	2.964	2.942 + 0.011*SL	2.950 + 0.009*SL	2.953 + 0.009*SL
	t_{PHL}	2.972	2.943 + 0.014*SL	2.951 + 0.012*SL	2.955 + 0.012*SL

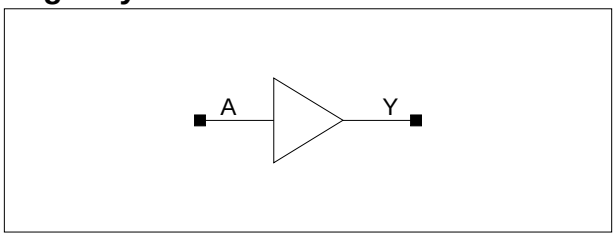
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

DL3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.086 + 0.008*SL	0.083 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.090	0.069 + 0.011*SL	0.069 + 0.011*SL	0.041 + 0.011*SL
	t_{PLH}	2.994	2.981 + 0.007*SL	2.989 + 0.005*SL	3.003 + 0.004*SL
	t_{PHL}	2.989	2.973 + 0.008*SL	2.982 + 0.006*SL	2.993 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)		Gate Count	
DL4D2	*DL4D4*	*DL4D2*	*DL4D4*
A	A	5.00	5.33
0.6	0.6		

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

DL4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.069 + 0.017*SL	0.059 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.102	0.057 + 0.023*SL	0.055 + 0.023*SL	0.033 + 0.024*SL
	t_{PLH}	3.978	3.956 + 0.011*SL	3.964 + 0.009*SL	3.967 + 0.009*SL
	t_{PHL}	3.972	3.944 + 0.014*SL	3.951 + 0.012*SL	3.955 + 0.012*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

DL4D4

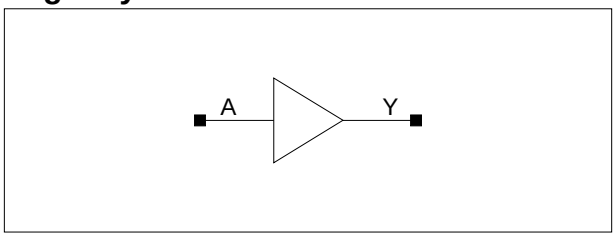
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.105	0.088 + 0.009*SL	0.085 + 0.009*SL	0.053 + 0.010*SL
	t_F	0.092	0.071 + 0.011*SL	0.071 + 0.011*SL	0.042 + 0.011*SL
	t_{PLH}	4.008	3.995 + 0.007*SL	4.004 + 0.005*SL	4.017 + 0.004*SL
	t_{PHL}	3.988	3.972 + 0.008*SL	3.981 + 0.006*SL	3.992 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

DL5D2/DL5D4

5ns Delay Cell with 2X/4X Drive

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)		Gate Count	
DL5D2	*DL5D4*	*DL5D2*	*DL5D4*
A	A	5.00	5.67
0.6	0.6		

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

DL5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.102	0.069 + 0.017*SL	0.059 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.103	0.060 + 0.021*SL	0.052 + 0.023*SL	0.033 + 0.024*SL
	t_{PLH}	4.971	4.949 + 0.011*SL	4.957 + 0.009*SL	4.960 + 0.009*SL
	t_{PHL}	4.941	4.912 + 0.014*SL	4.920 + 0.012*SL	4.924 + 0.012*SL

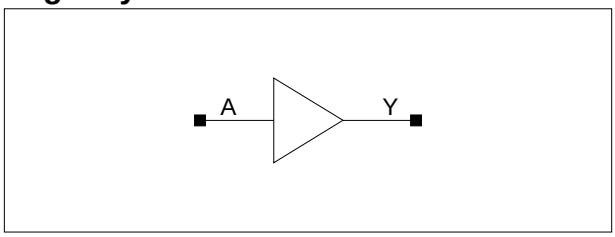
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

DL5D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.087 + 0.008*SL	0.083 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.092	0.071 + 0.010*SL	0.070 + 0.011*SL	0.043 + 0.011*SL
	t_{PLH}	5.012	4.998 + 0.007*SL	5.007 + 0.005*SL	5.020 + 0.004*SL
	t_{PHL}	4.973	4.957 + 0.008*SL	4.965 + 0.006*SL	4.977 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)		Gate Count	
DL10D2	*DL10D4*	*DL10D2*	*DL2D4*
A	A	7.00	7.67
0.6	0.6		

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

DL10D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.102	0.068 + 0.017*SL	0.059 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.104	0.060 + 0.022*SL	0.055 + 0.023*SL	0.033 + 0.024*SL
	t_{PLH}	9.981	9.960 + 0.011*SL	9.967 + 0.009*SL	9.971 + 0.009*SL
	t_{PHL}	9.971	9.943 + 0.014*SL	9.950 + 0.012*SL	9.954 + 0.012*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

DL10D4

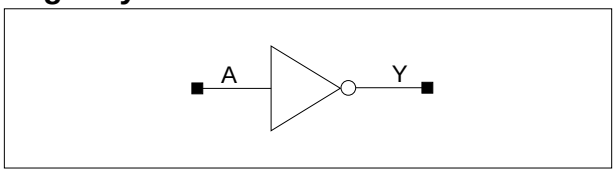
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.104	0.087 + 0.008*SL	0.084 + 0.009*SL	0.052 + 0.010*SL
	t_F	0.092	0.071 + 0.011*SL	0.071 + 0.011*SL	0.042 + 0.011*SL
	t_{PLH}	10.021	10.007 + 0.007*SL	10.016 + 0.005*SL	10.028 + 0.004*SL
	t_{PHL}	10.004	9.988 + 0.008*SL	9.996 + 0.006*SL	10.008 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

IVDH/IV/IVD2/IVD3/IVD4/IVD6/IVD8/IVD16

Inverter with 0.5X/1X/2X/3X/4X/6X/8X/16X Drive

Logic Symbol



Truth Table

A	Y
0	1
1	0

Cell Data

Input Load (SL)							
IVDH	*IV*	*IVD2*	*IVD3*	*IVD4*	*IVD6*	*IVD8*	*IVD16*
A	A	A	A	A	A	A	A
0.5	1.0	2.0	3.0	4.0	6.0	8.2	16.6
Gate Count							
IVDH	*IV*	*IVD2*	*IVD3*	*IVD4*	*IVD6*	*IVD8*	*IVD16*
0.67	0.67	1.00	1.33	1.67	2.33	2.67	5.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

IVDH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.223	0.099 + 0.062*SL	0.067 + 0.070*SL	0.043 + 0.071*SL
	t_F	0.181	0.087 + 0.047*SL	0.059 + 0.054*SL	0.029 + 0.055*SL
	t_{PLH}	0.144	0.079 + 0.033*SL	0.083 + 0.032*SL	0.078 + 0.032*SL
	t_{PHL}	0.115	0.051 + 0.032*SL	0.064 + 0.029*SL	0.061 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

IV

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.167	0.103 + 0.032*SL	0.080 + 0.037*SL	0.042 + 0.039*SL
	t_F	0.144	0.088 + 0.028*SL	0.071 + 0.032*SL	0.030 + 0.033*SL
	t_{PLH}	0.110	0.069 + 0.021*SL	0.083 + 0.017*SL	0.078 + 0.017*SL
	t_{PHL}	0.090	0.046 + 0.022*SL	0.063 + 0.017*SL	0.062 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

IVD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.123	0.091 + 0.016*SL	0.081 + 0.019*SL	0.030 + 0.020*SL
	t_F	0.105	0.073 + 0.016*SL	0.072 + 0.016*SL	0.020 + 0.017*SL
	t_{PLH}	0.081	0.056 + 0.013*SL	0.072 + 0.009*SL	0.073 + 0.009*SL
	t_{PHL}	0.059	0.032 + 0.013*SL	0.050 + 0.009*SL	0.057 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

IVD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.117	0.093 + 0.012*SL	0.092 + 0.012*SL	0.037 + 0.013*SL
	t_F	0.098	0.075 + 0.011*SL	0.078 + 0.011*SL	0.029 + 0.011*SL
	t_{PLH}	0.076	0.058 + 0.009*SL	0.071 + 0.006*SL	0.077 + 0.006*SL
	t_{PHL}	0.054	0.035 + 0.009*SL	0.048 + 0.006*SL	0.060 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

IVD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.107	0.087 + 0.010*SL	0.090 + 0.009*SL	0.041 + 0.010*SL
	t_F	0.089	0.071 + 0.009*SL	0.076 + 0.008*SL	0.035 + 0.008*SL
	t_{PLH}	0.069	0.055 + 0.007*SL	0.066 + 0.004*SL	0.076 + 0.004*SL
	t_{PHL}	0.046	0.031 + 0.008*SL	0.043 + 0.005*SL	0.059 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

IVD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.101	0.088 + 0.006*SL	0.089 + 0.006*SL	0.031 + 0.007*SL
	t_F	0.083	0.071 + 0.006*SL	0.074 + 0.005*SL	0.021 + 0.006*SL
	t_{PLH}	0.067	0.056 + 0.005*SL	0.065 + 0.003*SL	0.076 + 0.003*SL
	t_{PHL}	0.043	0.032 + 0.006*SL	0.042 + 0.003*SL	0.060 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

IVD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.097	0.087 + 0.005*SL	0.089 + 0.005*SL	0.030 + 0.005*SL
	t_F	0.080	0.070 + 0.005*SL	0.073 + 0.004*SL	0.021 + 0.004*SL
	t_{PLH}	0.061	0.053 + 0.004*SL	0.061 + 0.002*SL	0.074 + 0.002*SL
	t_{PHL}	0.038	0.029 + 0.004*SL	0.037 + 0.002*SL	0.058 + 0.002*SL

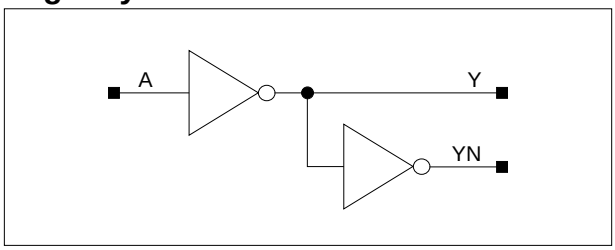
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

IVD16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.094	0.089 + 0.003*SL	0.090 + 0.002*SL	0.042 + 0.002*SL
	t_F	0.076	0.071 + 0.003*SL	0.073 + 0.002*SL	0.036 + 0.002*SL
	t_{PLH}	0.061	0.057 + 0.002*SL	0.061 + 0.001*SL	0.080 + 0.001*SL
	t_{PHL}	0.038	0.033 + 0.002*SL	0.038 + 0.001*SL	0.063 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

Logic Symbol



Truth Table

A	Y	YN
1	0	1
0	1	0

Cell Data

Input Load (SL)					Gate Count				
IVCD11	*IVCD13*	*IVCD22*	*IVCD26*	*IVCD44*	*IVCD11*	*IVCD13*	*IVCD22*	*IVCD26*	*IVCD44*
A	A	A	A	A					
1.0	1.0	2.0	2.0	4.0	1.00	1.67	1.67	2.67	2.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

IVCD11

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.211	0.149 + 0.031*SL	0.123 + 0.038*SL	0.087 + 0.039*SL
	t_F	0.184	0.127 + 0.028*SL	0.111 + 0.033*SL	0.072 + 0.034*SL
	t_{PLH}	0.135	0.097 + 0.019*SL	0.103 + 0.017*SL	0.100 + 0.017*SL
	t_{PHL}	0.112	0.071 + 0.020*SL	0.082 + 0.018*SL	0.080 + 0.018*SL
Y to YN	t_R	0.168	0.105 + 0.032*SL	0.081 + 0.038*SL	0.043 + 0.039*SL
	t_F	0.145	0.088 + 0.028*SL	0.071 + 0.032*SL	0.031 + 0.034*SL
	t_{PLH}	0.111	0.070 + 0.021*SL	0.083 + 0.017*SL	0.079 + 0.017*SL
	t_{PHL}	0.091	0.048 + 0.022*SL	0.064 + 0.018*SL	0.063 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

IVCD13

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.282	0.213 + 0.034*SL	0.197 + 0.038*SL	0.170 + 0.039*SL
	t_F	0.256	0.198 + 0.029*SL	0.182 + 0.033*SL	0.150 + 0.034*SL
	t_{PLH}	0.176	0.141 + 0.017*SL	0.141 + 0.017*SL	0.142 + 0.017*SL
	t_{PHL}	0.146	0.110 + 0.018*SL	0.112 + 0.018*SL	0.111 + 0.018*SL
Y to YN	t_R	0.116	0.093 + 0.012*SL	0.092 + 0.012*SL	0.037 + 0.013*SL
	t_F	0.098	0.075 + 0.011*SL	0.079 + 0.011*SL	0.029 + 0.011*SL
	t_{PLH}	0.076	0.058 + 0.009*SL	0.071 + 0.006*SL	0.076 + 0.006*SL
	t_{PHL}	0.053	0.034 + 0.010*SL	0.048 + 0.006*SL	0.060 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

IVCD22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.164	0.133 + 0.016*SL	0.120 + 0.019*SL	0.073 + 0.020*SL
	t_F	0.147	0.119 + 0.014*SL	0.111 + 0.016*SL	0.061 + 0.017*SL
	t_{PLH}	0.108	0.087 + 0.011*SL	0.095 + 0.009*SL	0.095 + 0.009*SL
	t_{PHL}	0.082	0.059 + 0.012*SL	0.070 + 0.009*SL	0.073 + 0.009*SL
Y to YN	t_R	0.124	0.091 + 0.016*SL	0.082 + 0.019*SL	0.030 + 0.020*SL
	t_F	0.105	0.073 + 0.016*SL	0.073 + 0.016*SL	0.021 + 0.017*SL
	t_{PLH}	0.081	0.056 + 0.013*SL	0.072 + 0.009*SL	0.073 + 0.009*SL
	t_{PHL}	0.059	0.032 + 0.013*SL	0.050 + 0.009*SL	0.057 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

IVCD26

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.239	0.206 + 0.017*SL	0.194 + 0.019*SL	0.158 + 0.020*SL
	t_F	0.220	0.192 + 0.014*SL	0.181 + 0.017*SL	0.139 + 0.017*SL
	t_{PLH}	0.152	0.134 + 0.009*SL	0.135 + 0.009*SL	0.141 + 0.009*SL
	t_{PHL}	0.120	0.100 + 0.010*SL	0.105 + 0.009*SL	0.104 + 0.009*SL
Y to YN	t_R	0.101	0.087 + 0.007*SL	0.089 + 0.006*SL	0.030 + 0.007*SL
	t_F	0.083	0.070 + 0.006*SL	0.073 + 0.005*SL	0.021 + 0.006*SL
	t_{PLH}	0.065	0.054 + 0.005*SL	0.063 + 0.003*SL	0.074 + 0.003*SL
	t_{PHL}	0.041	0.030 + 0.006*SL	0.040 + 0.003*SL	0.058 + 0.003*SL

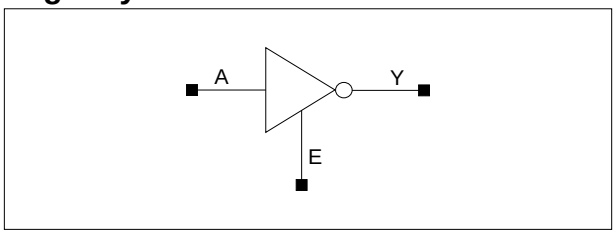
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

IVCD44

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.149	0.136 + 0.007*SL	0.127 + 0.009*SL	0.083 + 0.010*SL
	t_F	0.133	0.119 + 0.007*SL	0.115 + 0.008*SL	0.074 + 0.008*SL
	t_{PLH}	0.098	0.086 + 0.006*SL	0.092 + 0.004*SL	0.096 + 0.004*SL
	t_{PHL}	0.071	0.058 + 0.006*SL	0.066 + 0.005*SL	0.075 + 0.004*SL
Y to YN	t_R	0.107	0.087 + 0.010*SL	0.090 + 0.009*SL	0.041 + 0.010*SL
	t_F	0.089	0.071 + 0.009*SL	0.076 + 0.008*SL	0.035 + 0.008*SL
	t_{PLH}	0.069	0.054 + 0.007*SL	0.065 + 0.004*SL	0.076 + 0.004*SL
	t_{PHL}	0.045	0.030 + 0.008*SL	0.042 + 0.005*SL	0.059 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	1
1	1	0

Cell Data

Input Load (SL)										Output Load (SL)				
IVT		*IVTD2*		*IVTD4*		*IVTD8*		*IVTD16*		*IVT*	*IVTD2*	*IVTD4*	*IVTD8*	*IVTD16*
A	E	A	E	A	E	A	E	A	E	Y	Y	Y	Y	Y
0.7	1.6	0.7	1.6	0.8	1.9	1.0	3.2	1.0	3.2	0.9	1.0	2.0	4.0	8.0

Gate Count				
IVT	*IVTD2*	*IVTD4*	*IVTD8*	*IVTD16*
3.00	3.00	3.67	5.67	8.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

IVT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.142	0.070 + 0.036*SL	0.063 + 0.038*SL	0.049 + 0.038*SL
	t_F	0.120	0.055 + 0.033*SL	0.056 + 0.032*SL	0.039 + 0.033*SL
	t_{PLH}	0.291	0.252 + 0.020*SL	0.261 + 0.017*SL	0.264 + 0.017*SL
	t_{PHL}	0.243	0.203 + 0.020*SL	0.214 + 0.017*SL	0.220 + 0.017*SL
E to Y	t_R	0.163	0.085 + 0.039*SL	0.072 + 0.042*SL	0.055 + 0.043*SL
	t_F	0.134	0.066 + 0.034*SL	0.064 + 0.035*SL	0.042 + 0.035*SL
	t_{PLH}	0.166	0.126 + 0.020*SL	0.138 + 0.017*SL	0.229 + 0.015*SL
	t_{PHL}	0.219	0.176 + 0.021*SL	0.192 + 0.017*SL	0.293 + 0.014*SL
	t_{PLZ}	0.218	0.218 + 0.000*SL	0.218 + 0.000*SL	0.218 + 0.000*SL
	t_{PHZ}	0.160	0.160 + 0.000*SL	0.160 + 0.000*SL	0.160 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

IVTD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.100	0.061 + 0.019*SL	0.061 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.083	0.049 + 0.017*SL	0.051 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.280	0.254 + 0.013*SL	0.269 + 0.009*SL	0.282 + 0.009*SL
	t_{PHL}	0.226	0.203 + 0.012*SL	0.213 + 0.009*SL	0.227 + 0.009*SL
E to Y	t_R	0.119	0.080 + 0.020*SL	0.073 + 0.021*SL	0.043 + 0.022*SL
	t_F	0.092	0.055 + 0.019*SL	0.059 + 0.018*SL	0.032 + 0.018*SL
	t_{PLH}	0.158	0.132 + 0.013*SL	0.149 + 0.009*SL	0.248 + 0.007*SL
	t_{PHL}	0.196	0.169 + 0.013*SL	0.187 + 0.009*SL	0.297 + 0.007*SL
	t_{PLZ}	0.230	0.230 + 0.000*SL	0.229 + 0.000*SL	0.229 + 0.000*SL
	t_{PHZ}	0.193	0.193 + 0.000*SL	0.193 + 0.000*SL	0.192 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

IVTD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.088	0.065 + 0.011*SL	0.073 + 0.009*SL	0.056 + 0.010*SL
	t_F	0.078	0.063 + 0.008*SL	0.061 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.273	0.257 + 0.008*SL	0.271 + 0.005*SL	0.298 + 0.004*SL
	t_{PHL}	0.270	0.257 + 0.006*SL	0.264 + 0.005*SL	0.283 + 0.004*SL
E to Y	t_R	0.109	0.087 + 0.011*SL	0.088 + 0.010*SL	0.063 + 0.011*SL
	t_F	0.080	0.060 + 0.010*SL	0.065 + 0.009*SL	0.053 + 0.009*SL
	t_{PLH}	0.159	0.142 + 0.008*SL	0.157 + 0.005*SL	0.187 + 0.004*SL
	t_{PHL}	0.223	0.206 + 0.008*SL	0.219 + 0.005*SL	0.254 + 0.004*SL
	t_{PLZ}	0.230	0.230 + 0.000*SL	0.230 + 0.000*SL	0.229 + 0.000*SL
	t_{PHZ}	0.240	0.240 + 0.000*SL	0.238 + 0.000*SL	0.236 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

IVTD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.078	0.066 + 0.006*SL	0.070 + 0.005*SL	0.045 + 0.005*SL
	t_F	0.072	0.064 + 0.004*SL	0.063 + 0.004*SL	0.035 + 0.004*SL
	t_{PLH}	0.298	0.289 + 0.005*SL	0.299 + 0.002*SL	0.333 + 0.002*SL
	t_{PHL}	0.284	0.278 + 0.003*SL	0.282 + 0.002*SL	0.300 + 0.002*SL
E to Y	t_R	0.097	0.086 + 0.005*SL	0.086 + 0.005*SL	0.047 + 0.005*SL
	t_F	0.068	0.057 + 0.006*SL	0.062 + 0.004*SL	0.033 + 0.005*SL
	t_{PLH}	0.148	0.138 + 0.005*SL	0.149 + 0.002*SL	0.282 + 0.002*SL
	t_{PHL}	0.220	0.211 + 0.004*SL	0.220 + 0.002*SL	0.361 + 0.002*SL
	t_{PLZ}	0.246	0.246 + 0.000*SL	0.246 + 0.000*SL	0.245 + 0.000*SL
	t_{PHZ}	0.236	0.236 + 0.000*SL	0.235 + 0.000*SL	0.232 + 0.000*SL

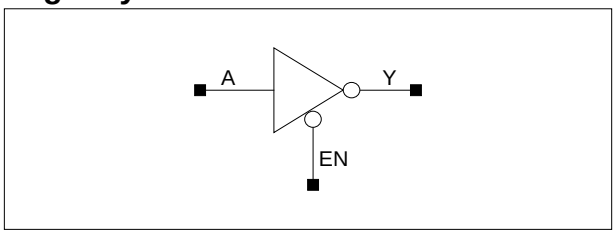
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

IVTD16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.088	0.079 + 0.004*SL	0.086 + 0.002*SL	0.093 + 0.002*SL
	t_F	0.107	0.103 + 0.002*SL	0.103 + 0.002*SL	0.065 + 0.002*SL
	t_{PLH}	0.339	0.333 + 0.003*SL	0.340 + 0.001*SL	0.412 + 0.001*SL
	t_{PHL}	0.329	0.325 + 0.002*SL	0.329 + 0.001*SL	0.351 + 0.001*SL
E to Y	t_R	0.116	0.111 + 0.002*SL	0.110 + 0.003*SL	0.101 + 0.003*SL
	t_F	0.076	0.070 + 0.003*SL	0.074 + 0.002*SL	0.071 + 0.002*SL
	t_{PLH}	0.191	0.184 + 0.004*SL	0.193 + 0.001*SL	0.267 + 0.001*SL
	t_{PHL}	0.243	0.237 + 0.003*SL	0.243 + 0.001*SL	0.303 + 0.001*SL
	t_{PLZ}	0.286	0.286 + 0.000*SL	0.286 + 0.000*SL	0.284 + 0.000*SL
	t_{PHZ}	0.362	0.362 + 0.000*SL	0.358 + 0.000*SL	0.346 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

Logic Symbol



Truth Table

A	EN	Y
x	1	Hi-Z
0	0	1
1	0	0

Cell Data

Input Load (SL)										Output Load (SL)				
IVTN		*IVTND2*		*IVTND4*		*IVTND8*		*IVTND16*		*IVTN*	*IVTND2*	*IVTND4*	*IVTND8*	*IVTND16*
A	EN	A	EN	A	EN	A	EN	A	EN	Y	Y	Y	Y	Y
0.7	1.4	0.7	1.4	0.8	1.8	1.0	3.1	1.0	3.1	0.8	1.0	2.0	4.0	8.0

Gate Count				
IVTN	*IVTND2*	*IVTND4*	*IVTND8*	*IVTND16*
2.67	3.00	3.67	5.67	8.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

IVTN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.141	0.067 + 0.037*SL	0.061 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.120	0.054 + 0.033*SL	0.054 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.290	0.250 + 0.020*SL	0.260 + 0.018*SL	0.263 + 0.017*SL
	t_{PHL}	0.241	0.199 + 0.021*SL	0.211 + 0.018*SL	0.217 + 0.018*SL
EN to Y	t_R	0.157	0.076 + 0.040*SL	0.067 + 0.043*SL	0.052 + 0.043*SL
	t_F	0.138	0.070 + 0.034*SL	0.064 + 0.035*SL	0.039 + 0.036*SL
	t_{PLH}	0.260	0.220 + 0.020*SL	0.231 + 0.017*SL	0.322 + 0.015*SL
	t_{PHL}	0.183	0.140 + 0.022*SL	0.157 + 0.018*SL	0.259 + 0.015*SL
	t_{PLZ}	0.125	0.125 + 0.000*SL	0.125 + 0.000*SL	0.125 + 0.000*SL
	t_{PHZ}	0.181	0.181 + 0.000*SL	0.181 + 0.000*SL	0.181 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

IVTND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.100	0.062 + 0.019*SL	0.062 + 0.019*SL	0.039 + 0.019*SL
	t_F	0.083	0.049 + 0.017*SL	0.050 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.280	0.255 + 0.013*SL	0.270 + 0.009*SL	0.284 + 0.009*SL
	t_{PHL}	0.226	0.202 + 0.012*SL	0.213 + 0.009*SL	0.227 + 0.009*SL
EN to Y	t_R	0.115	0.074 + 0.020*SL	0.070 + 0.021*SL	0.043 + 0.022*SL
	t_F	0.097	0.060 + 0.019*SL	0.063 + 0.018*SL	0.032 + 0.018*SL
	t_{PLH}	0.252	0.226 + 0.013*SL	0.243 + 0.009*SL	0.340 + 0.007*SL
	t_{PHL}	0.162	0.135 + 0.014*SL	0.153 + 0.009*SL	0.264 + 0.007*SL
	t_{PLZ}	0.140	0.140 + 0.000*SL	0.140 + 0.000*SL	0.140 + 0.000*SL
	t_{PHZ}	0.216	0.216 + 0.000*SL	0.215 + 0.000*SL	0.214 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

IVTND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.088	0.065 + 0.011*SL	0.073 + 0.009*SL	0.056 + 0.010*SL
	t_F	0.078	0.063 + 0.008*SL	0.061 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.274	0.258 + 0.008*SL	0.271 + 0.005*SL	0.299 + 0.004*SL
	t_{PHL}	0.270	0.257 + 0.006*SL	0.264 + 0.005*SL	0.283 + 0.004*SL
EN to Y	t_R	0.104	0.082 + 0.011*SL	0.084 + 0.010*SL	0.062 + 0.011*SL
	t_F	0.084	0.064 + 0.010*SL	0.069 + 0.009*SL	0.054 + 0.009*SL
	t_{PLH}	0.244	0.228 + 0.008*SL	0.242 + 0.005*SL	0.272 + 0.004*SL
	t_{PHL}	0.161	0.145 + 0.008*SL	0.158 + 0.005*SL	0.195 + 0.004*SL
	t_{PLZ}	0.148	0.148 + 0.000*SL	0.148 + 0.000*SL	0.148 + 0.000*SL
	t_{PHZ}	0.293	0.293 + 0.000*SL	0.291 + 0.000*SL	0.289 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

IVTND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.077	0.064 + 0.007*SL	0.071 + 0.005*SL	0.045 + 0.005*SL
	t_F	0.072	0.064 + 0.004*SL	0.063 + 0.004*SL	0.035 + 0.004*SL
	t_{PLH}	0.299	0.290 + 0.005*SL	0.299 + 0.002*SL	0.334 + 0.002*SL
	t_{PHL}	0.284	0.277 + 0.003*SL	0.282 + 0.002*SL	0.300 + 0.002*SL
EN to Y	t_R	0.092	0.081 + 0.006*SL	0.083 + 0.005*SL	0.047 + 0.005*SL
	t_F	0.071	0.060 + 0.006*SL	0.064 + 0.004*SL	0.034 + 0.005*SL
	t_{PLH}	0.255	0.246 + 0.005*SL	0.256 + 0.002*SL	0.388 + 0.002*SL
	t_{PHL}	0.148	0.138 + 0.005*SL	0.148 + 0.002*SL	0.290 + 0.002*SL
	t_{PLZ}	0.141	0.141 + 0.000*SL	0.141 + 0.000*SL	0.140 + 0.000*SL
	t_{PHZ}	0.302	0.302 + 0.000*SL	0.301 + 0.000*SL	0.298 + 0.000*SL

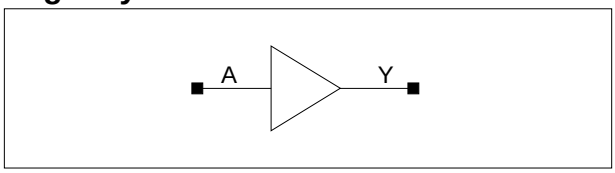
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

IVTND16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.088	0.079 + 0.004*SL	0.087 + 0.002*SL	0.094 + 0.002*SL
	t_F	0.106	0.103 + 0.002*SL	0.102 + 0.002*SL	0.065 + 0.002*SL
	t_{PLH}	0.340	0.334 + 0.003*SL	0.342 + 0.001*SL	0.414 + 0.001*SL
	t_{PHL}	0.329	0.325 + 0.002*SL	0.329 + 0.001*SL	0.351 + 0.001*SL
EN to Y	t_R	0.113	0.107 + 0.003*SL	0.108 + 0.003*SL	0.102 + 0.003*SL
	t_F	0.078	0.072 + 0.003*SL	0.076 + 0.002*SL	0.071 + 0.002*SL
	t_{PLH}	0.298	0.291 + 0.003*SL	0.299 + 0.001*SL	0.373 + 0.001*SL
	t_{PHL}	0.169	0.163 + 0.003*SL	0.170 + 0.001*SL	0.230 + 0.001*SL
	t_{PLZ}	0.182	0.182 + 0.000*SL	0.182 + 0.000*SL	0.180 + 0.000*SL
	t_{PHZ}	0.430	0.430 + 0.000*SL	0.426 + 0.000*SL	0.413 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)							
NIDH	*NID*	*NID2*	*NID3*	*NID4*	*NID6*	*NID8*	*NID16*
A	A	A	A	A	A	A	A
0.5	0.8	0.8	1.0	1.0	1.5	1.9	2.9
Gate Count							
NIDH	*NID*	*NID2*	*NID3*	*NID4*	*NID6*	*NID8*	*NID16*
1.00	1.00	1.33	1.67	2.00	2.67	3.33	6.00

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NIDH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.196	0.057 + 0.070*SL	0.047 + 0.072*SL	0.044 + 0.072*SL
	t_F	0.152	0.048 + 0.052*SL	0.038 + 0.054*SL	0.029 + 0.055*SL
	t_{PLH}	0.173	0.108 + 0.033*SL	0.108 + 0.033*SL	0.108 + 0.033*SL
	t_{PHL}	0.196	0.136 + 0.030*SL	0.140 + 0.029*SL	0.140 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

NID

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.135	0.064 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.114	0.051 + 0.032*SL	0.045 + 0.033*SL	0.032 + 0.034*SL
	t_{PLH}	0.158	0.122 + 0.018*SL	0.125 + 0.017*SL	0.124 + 0.017*SL
	t_{PHL}	0.175	0.137 + 0.019*SL	0.143 + 0.018*SL	0.144 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

NID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.099	0.064 + 0.018*SL	0.057 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.086	0.056 + 0.015*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.168	0.148 + 0.010*SL	0.154 + 0.009*SL	0.156 + 0.009*SL
	t_{PHL}	0.180	0.158 + 0.011*SL	0.167 + 0.009*SL	0.174 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NID3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.092	0.070 + 0.011*SL	0.064 + 0.013*SL	0.041 + 0.013*SL
	t_F	0.079	0.058 + 0.011*SL	0.057 + 0.011*SL	0.034 + 0.011*SL
	t_{PLH}	0.165	0.151 + 0.007*SL	0.156 + 0.006*SL	0.160 + 0.006*SL
	t_{PHL}	0.187	0.171 + 0.008*SL	0.179 + 0.006*SL	0.189 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NID4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.092	0.073 + 0.009*SL	0.073 + 0.009*SL	0.045 + 0.010*SL
	t_F	0.078	0.061 + 0.008*SL	0.062 + 0.008*SL	0.041 + 0.008*SL
	t_{PLH}	0.181	0.170 + 0.006*SL	0.175 + 0.005*SL	0.184 + 0.004*SL
	t_{PHL}	0.202	0.189 + 0.007*SL	0.197 + 0.005*SL	0.213 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NID6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.082	0.071 + 0.006*SL	0.068 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.070	0.059 + 0.005*SL	0.058 + 0.006*SL	0.027 + 0.006*SL
	t_{PLH}	0.169	0.161 + 0.004*SL	0.166 + 0.003*SL	0.174 + 0.003*SL
	t_{PHL}	0.187	0.178 + 0.004*SL	0.183 + 0.003*SL	0.198 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

NID8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.082	0.074 + 0.004*SL	0.072 + 0.005*SL	0.038 + 0.005*SL
	t_F	0.068	0.059 + 0.004*SL	0.060 + 0.004*SL	0.030 + 0.004*SL
	t_{PLH}	0.176	0.170 + 0.003*SL	0.174 + 0.002*SL	0.185 + 0.002*SL
	t_{PHL}	0.189	0.182 + 0.004*SL	0.187 + 0.002*SL	0.204 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

NID16

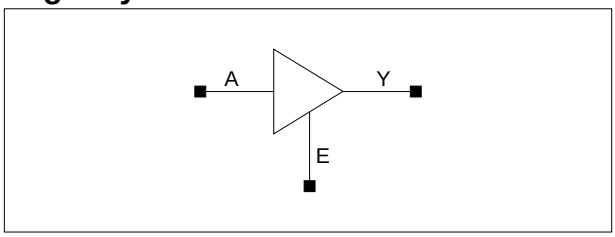
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.090	0.086 + 0.002*SL	0.085 + 0.002*SL	0.056 + 0.002*SL
	t_F	0.077	0.072 + 0.002*SL	0.073 + 0.002*SL	0.051 + 0.002*SL
	t_{PLH}	0.202	0.198 + 0.002*SL	0.201 + 0.001*SL	0.221 + 0.001*SL
	t_{PHL}	0.216	0.212 + 0.002*SL	0.215 + 0.001*SL	0.243 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

NIT/NITD2/NITD4/NITD8/NITD16

Non-Inverting Tri-State Buffer with Enable High, 1X/2X/4X/8X/16X Drive

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	0
1	1	1

Cell Data

Input Load (SL)										Output Load (SL)				
NIT		*NITD2*		*NITD4*		*NITD8*		*NITD16*		*NIT*	*NITD2*	*NITD4*	*NITD8*	*NITD16*
A	E	A	E	A	E	A	E	A	E	Y	Y	Y	Y	Y
1.4	1.5	1.4	1.5	1.8	1.7	3.6	2.9	3.7	2.9	0.8	1.1	2.0	4.1	8.3

Gate Count				
NIT	*NITD2*	*NITD4*	*NITD8*	*NITD16*
2.67	2.67	3.33	5.33	7.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NIT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.142	0.070 + 0.036*SL	0.061 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.121	0.056 + 0.033*SL	0.055 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.153	0.113 + 0.020*SL	0.123 + 0.018*SL	0.125 + 0.017*SL
	t_{PHL}	0.190	0.149 + 0.021*SL	0.161 + 0.018*SL	0.167 + 0.018*SL
E to Y	t_R	0.161	0.082 + 0.039*SL	0.069 + 0.043*SL	0.052 + 0.043*SL
	t_F	0.133	0.063 + 0.035*SL	0.061 + 0.036*SL	0.039 + 0.036*SL
	t_{PLH}	0.165	0.125 + 0.020*SL	0.137 + 0.017*SL	0.229 + 0.015*SL
	t_{PHL}	0.214	0.171 + 0.022*SL	0.187 + 0.018*SL	0.289 + 0.015*SL
	t_{PLZ}	0.214	0.214 + 0.000*SL	0.214 + 0.000*SL	0.214 + 0.000*SL
	t_{PHZ}	0.164	0.164 + 0.000*SL	0.164 + 0.000*SL	0.164 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

NITD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.066 + 0.019*SL	0.064 + 0.019*SL	0.039 + 0.019*SL
	t_F	0.085	0.052 + 0.017*SL	0.052 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.144	0.118 + 0.013*SL	0.133 + 0.009*SL	0.145 + 0.009*SL
	t_{PHL}	0.176	0.153 + 0.012*SL	0.163 + 0.009*SL	0.176 + 0.009*SL
E to Y	t_R	0.119	0.079 + 0.020*SL	0.074 + 0.021*SL	0.044 + 0.022*SL
	t_F	0.093	0.056 + 0.018*SL	0.058 + 0.018*SL	0.032 + 0.018*SL
	t_{PLH}	0.160	0.134 + 0.013*SL	0.151 + 0.009*SL	0.249 + 0.007*SL
	t_{PHL}	0.194	0.168 + 0.013*SL	0.185 + 0.009*SL	0.294 + 0.007*SL
	t_{PLZ}	0.228	0.228 + 0.000*SL	0.227 + 0.000*SL	0.227 + 0.000*SL
	t_{PHZ}	0.198	0.198 + 0.000*SL	0.197 + 0.000*SL	0.197 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NITD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.088	0.066 + 0.011*SL	0.072 + 0.009*SL	0.055 + 0.010*SL
	t_F	0.078	0.064 + 0.007*SL	0.061 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.145	0.129 + 0.008*SL	0.142 + 0.005*SL	0.169 + 0.004*SL
	t_{PHL}	0.185	0.172 + 0.006*SL	0.179 + 0.005*SL	0.197 + 0.004*SL
E to Y	t_R	0.107	0.086 + 0.011*SL	0.087 + 0.010*SL	0.061 + 0.011*SL
	t_F	0.078	0.057 + 0.010*SL	0.064 + 0.009*SL	0.051 + 0.009*SL
	t_{PLH}	0.159	0.142 + 0.008*SL	0.156 + 0.005*SL	0.186 + 0.004*SL
	t_{PHL}	0.200	0.183 + 0.008*SL	0.196 + 0.005*SL	0.231 + 0.004*SL
	t_{PLZ}	0.247	0.247 + 0.000*SL	0.247 + 0.000*SL	0.246 + 0.000*SL
	t_{PHZ}	0.241	0.241 + 0.000*SL	0.239 + 0.000*SL	0.238 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NITD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.078	0.068 + 0.005*SL	0.070 + 0.005*SL	0.044 + 0.005*SL
	t_F	0.072	0.065 + 0.004*SL	0.063 + 0.004*SL	0.033 + 0.004*SL
	t_{PLH}	0.136	0.127 + 0.005*SL	0.136 + 0.002*SL	0.169 + 0.002*SL
	t_{PHL}	0.173	0.166 + 0.003*SL	0.171 + 0.002*SL	0.187 + 0.002*SL
E to Y	t_R	0.097	0.087 + 0.005*SL	0.086 + 0.005*SL	0.047 + 0.005*SL
	t_F	0.067	0.055 + 0.006*SL	0.061 + 0.004*SL	0.033 + 0.005*SL
	t_{PLH}	0.148	0.138 + 0.005*SL	0.149 + 0.002*SL	0.281 + 0.002*SL
	t_{PHL}	0.218	0.209 + 0.005*SL	0.218 + 0.002*SL	0.358 + 0.002*SL
	t_{PLZ}	0.245	0.245 + 0.000*SL	0.245 + 0.000*SL	0.244 + 0.000*SL
	t_{PHZ}	0.236	0.236 + 0.000*SL	0.235 + 0.000*SL	0.231 + 0.000*SL

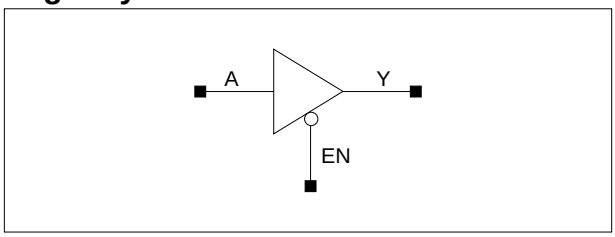
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

NITD16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.087	0.079 + 0.004*SL	0.086 + 0.002*SL	0.089 + 0.002*SL
	t_F	0.100	0.097 + 0.002*SL	0.096 + 0.002*SL	0.064 + 0.002*SL
	t_{PLH}	0.178	0.171 + 0.003*SL	0.179 + 0.001*SL	0.245 + 0.001*SL
	t_{PHL}	0.216	0.213 + 0.002*SL	0.215 + 0.001*SL	0.239 + 0.001*SL
E to Y	t_R	0.115	0.110 + 0.003*SL	0.110 + 0.003*SL	0.098 + 0.003*SL
	t_F	0.075	0.068 + 0.004*SL	0.073 + 0.002*SL	0.071 + 0.002*SL
	t_{PLH}	0.192	0.185 + 0.003*SL	0.193 + 0.001*SL	0.264 + 0.001*SL
	t_{PHL}	0.240	0.234 + 0.003*SL	0.240 + 0.001*SL	0.300 + 0.001*SL
	t_{PLZ}	0.287	0.287 + 0.000*SL	0.286 + 0.000*SL	0.285 + 0.000*SL
	t_{PHZ}	0.359	0.359 + 0.000*SL	0.355 + 0.000*SL	0.343 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 269, *Group3 : 269 < SL

Logic Symbol



Truth Table

A	EN	Y
x	1	Hi-Z
0	0	0
1	0	1

Cell Data

Input Load (SL)										Output Load (SL)				
NITN		*NITND2*		*NITND4*		*NITND8*		*NITND16*		*NITN*	*NITND2*	*NITND4*	*NITND8*	*NITND16*
A	EN	A	EN	A	EN	A	EN	A	EN	Y	Y	Y	Y	Y
1.7	1.5	1.6	1.4	2.1	1.7	4.3	3.1	4.3	3.1	0.8	1.1	2.1	4.1	8.3

Gate Count				
NITN	*NITND2*	*NITND4*	*NITND8*	*NITND16*
2.67	2.67	3.33	5.33	7.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26‘ns, SL: Standard Load)

NITN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.142	0.070 + 0.036*SL	0.062 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.122	0.057 + 0.033*SL	0.055 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.154	0.114 + 0.020*SL	0.123 + 0.018*SL	0.127 + 0.017*SL
	t_{PHL}	0.191	0.149 + 0.021*SL	0.161 + 0.018*SL	0.167 + 0.018*SL
EN to Y	t_R	0.158	0.078 + 0.040*SL	0.067 + 0.043*SL	0.052 + 0.043*SL
	t_F	0.137	0.069 + 0.034*SL	0.064 + 0.035*SL	0.039 + 0.036*SL
	t_{PLH}	0.263	0.223 + 0.020*SL	0.233 + 0.017*SL	0.325 + 0.015*SL
	t_{PHL}	0.182	0.139 + 0.022*SL	0.156 + 0.018*SL	0.257 + 0.015*SL
	t_{PLZ}	0.122	0.122 + 0.000*SL	0.122 + 0.000*SL	0.122 + 0.000*SL
	t_{PHZ}	0.187	0.187 + 0.000*SL	0.186 + 0.000*SL	0.186 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

NITND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.104	0.066 + 0.019*SL	0.065 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.086	0.053 + 0.016*SL	0.054 + 0.016*SL	0.032 + 0.017*SL
	t_{PLH}	0.147	0.121 + 0.013*SL	0.136 + 0.009*SL	0.149 + 0.009*SL
	t_{PHL}	0.177	0.154 + 0.011*SL	0.164 + 0.009*SL	0.178 + 0.009*SL
EN to Y	t_R	0.118	0.078 + 0.020*SL	0.073 + 0.021*SL	0.045 + 0.022*SL
	t_F	0.098	0.061 + 0.018*SL	0.064 + 0.017*SL	0.033 + 0.018*SL
	t_{PLH}	0.256	0.230 + 0.013*SL	0.246 + 0.009*SL	0.343 + 0.007*SL
	t_{PHL}	0.161	0.135 + 0.013*SL	0.153 + 0.009*SL	0.261 + 0.007*SL
	t_{PLZ}	0.139	0.139 + 0.000*SL	0.139 + 0.000*SL	0.138 + 0.000*SL
	t_{PHZ}	0.222	0.222 + 0.000*SL	0.220 + 0.000*SL	0.219 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

NITND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.089	0.068 + 0.011*SL	0.072 + 0.009*SL	0.056 + 0.010*SL
	t_F	0.079	0.064 + 0.007*SL	0.061 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.147	0.131 + 0.008*SL	0.144 + 0.005*SL	0.171 + 0.004*SL
	t_{PHL}	0.185	0.173 + 0.006*SL	0.179 + 0.005*SL	0.198 + 0.004*SL
EN to Y	t_R	0.104	0.083 + 0.011*SL	0.084 + 0.010*SL	0.061 + 0.011*SL
	t_F	0.085	0.066 + 0.009*SL	0.068 + 0.009*SL	0.052 + 0.009*SL
	t_{PLH}	0.265	0.249 + 0.008*SL	0.263 + 0.005*SL	0.292 + 0.004*SL
	t_{PHL}	0.159	0.142 + 0.008*SL	0.156 + 0.005*SL	0.191 + 0.004*SL
	t_{PLZ}	0.147	0.147 + 0.000*SL	0.146 + 0.000*SL	0.146 + 0.000*SL
	t_{PHZ}	0.277	0.277 + 0.000*SL	0.275 + 0.000*SL	0.273 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

NITND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.079	0.068 + 0.005*SL	0.071 + 0.005*SL	0.045 + 0.005*SL
	t_F	0.072	0.064 + 0.004*SL	0.063 + 0.004*SL	0.033 + 0.004*SL
	t_{PLH}	0.137	0.127 + 0.005*SL	0.137 + 0.002*SL	0.171 + 0.002*SL
	t_{PHL}	0.173	0.166 + 0.003*SL	0.171 + 0.002*SL	0.187 + 0.002*SL
EN to Y	t_R	0.092	0.081 + 0.006*SL	0.082 + 0.005*SL	0.047 + 0.005*SL
	t_F	0.071	0.060 + 0.005*SL	0.063 + 0.004*SL	0.033 + 0.005*SL
	t_{PLH}	0.255	0.245 + 0.005*SL	0.255 + 0.002*SL	0.387 + 0.002*SL
	t_{PHL}	0.146	0.137 + 0.005*SL	0.147 + 0.002*SL	0.288 + 0.002*SL
	t_{PLZ}	0.141	0.141 + 0.000*SL	0.141 + 0.000*SL	0.141 + 0.000*SL
	t_{PHZ}	0.302	0.302 + 0.000*SL	0.300 + 0.000*SL	0.297 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 269, *Group3 : 269 < SL

NITND16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.087	0.079 + 0.004*SL	0.086 + 0.002*SL	0.090 + 0.002*SL
	t_F	0.100	0.097 + 0.002*SL	0.096 + 0.002*SL	0.063 + 0.002*SL
	t_{PLH}	0.179	0.172 + 0.003*SL	0.180 + 0.001*SL	0.247 + 0.001*SL
	t_{PHL}	0.216	0.212 + 0.002*SL	0.215 + 0.001*SL	0.239 + 0.001*SL
EN to Y	t_R	0.114	0.108 + 0.003*SL	0.109 + 0.003*SL	0.098 + 0.003*SL
	t_F	0.079	0.074 + 0.003*SL	0.076 + 0.002*SL	0.072 + 0.002*SL
	t_{PLH}	0.297	0.291 + 0.003*SL	0.299 + 0.001*SL	0.370 + 0.001*SL
	t_{PHL}	0.169	0.163 + 0.003*SL	0.170 + 0.001*SL	0.230 + 0.001*SL
	t_{PLZ}	0.182	0.182 + 0.000*SL	0.182 + 0.000*SL	0.181 + 0.000*SL
	t_{PHZ}	0.425	0.425 + 0.000*SL	0.422 + 0.000*SL	0.410 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 269, *Group3 : 269 < SL

FLIP-FLOPS

Cell List

Cell Name	Function Description
FD1	D Flip-Flop
FD1D2	D Flip-Flop with 2X Drive
FD1CS	D Flip-Flop with Scan Clock
FD1CSD2	D Flip-Flop with Scan Clock, 2X Drive
FD1S	D Flip-Flop with Scan
FD1SD2	D Flip-Flop with Scan, 2X Drive
FD1SQ	D Flip-Flop with Scan, Q Output Only
FD1SQD2	D Flip-Flop with Scan, Q Output Only, 2X Drive
FD1Q	D Flip-Flop with Q Output Only
FD1QD2	D Flip-Flop with Q Output Only, 2X Drive
FD2	D Flip-Flop with Reset
FD2D2	D Flip-Flop with Reset, 2X Drive
FD2CS	D Flip-Flop with Reset, Scan Clock
FD2CSD2	D Flip-Flop with Reset, Scan Clock, 2X Drive
FD2S	D Flip-Flop with Reset, Scan
FD2SD2	D Flip-Flop with Reset, Scan, 2X Drive
FD2SQ	D Flip-Flop with Reset, Scan, Q Output Only
FD2SQD2	D Flip-Flop with Reset, Scan, Q Output Only, 2X Drive
FD2Q	D Flip-Flop with Reset, Q Output Only
FD2QD2	D Flip-Flop with Reset, Q Output Only, 2X Drive
FD3	D Flip-Flop with Set
FD3D2	D Flip-Flop with Set, 2X Drive
FD3CS	D Flip-Flop with Set, Scan Clock
FD3CSD2	D Flip-Flop with Set, Scan Clock, 2X Drive
FD3S	D Flip-Flop with Set, Scan
FD3SD2	D Flip-Flop with Set, Scan, 2X Drive
FD3SQ	D Flip-Flop with Set, Scan, Q Output Only
FD3SQD2	D Flip-Flop with Set, Scan, Q Output Only, 2X Drive
FD3Q	D Flip-Flop with Set, Q Output Only
FD3QD2	D Flip-Flop with Set, Q Output Only, 2X Drive
FD4	D Flip-Flop with Reset, Set
FD4D2	D Flip-Flop with Reset, Set, 2X Drive
FD4CS	D Flip-Flop with Reset, Set, Scan Clock
FD4CSD2	D Flip-Flop with Reset, Set, Scan Clock, 2X Drive
FD4S	D Flip-Flop with Reset, Set, Scan
FD4SD2	D Flip-Flop with Reset, Set, Scan, 2X Drive
FD4SQ	D Flip-Flop with Reset, Set, Scan, Q Output Only
FD4SQD2	D Flip-Flop with Reset, Set, Scan, Q Output Only, 2X Drive

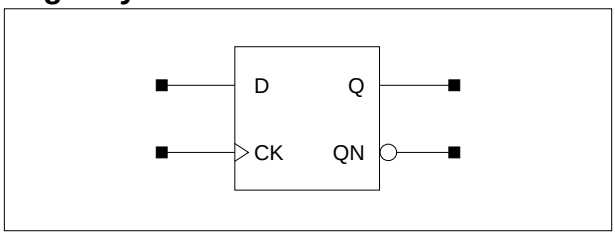
Cell List (Continued)

Cell Name	Function Description
FD4Q	D Flip-Flop with Reset, Set, Q Output Only
FD4QD2	D Flip-Flop with Reset, Set, Q Output Only, 2X Drive
FD5	D Flip-Flop with Negative Edge Trigger
FD5D2	D Flip-Flop with Negative Edge Trigger, 2X Drive
FD5S	D Flip-Flop with Negative Edge Trigger, Scan
FD5SD2	D Flip-Flop with Negative Edge Trigger, Scan, 2X Drive
FD6	D Flip-Flop with Negative Edge Trigger, Reset
FD6D2	D Flip-Flop with Negative Edge Trigger, Reset, 2X Drive
FD6S	D Flip-Flop with Negative Edge Trigger, Reset, Scan
FD6SD2	D Flip-Flop with Negative Edge Trigger, Reset, Scan, 2X Drive
FD7	D Flip-Flop with Negative Edge Trigger, Set
FD7D2	D Flip-Flop with Negative Edge Trigger, Set, 2X Drive
FD7S	D Flip-Flop with Negative Edge Trigger, Set, Scan
FD7SD2	D Flip-Flop with Negative Edge Trigger, Set, Scan, 2X Drive
FD8	D Flip-Flop with Negative Edge Trigger, Reset, Set
FD8D2	D Flip-Flop with Negative Edge Trigger, Reset, Set, 2X Drive
FD8S	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan
FD8SD2	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 2X Drive
FDS2	D Flip-Flop with Synchronous Clear
FDS2D2	D Flip-Flop with Synchronous Clear, 2X Drive
FDS2CS	D Flip-Flop with Synchronous Clear, Scan Clock
FDS2CSD2	D Flip-Flop with Synchronous Clear, Scan Clock, 2X Drive
FDS2S	D Flip-Flop with Synchronous Clear, Scan
FDS2SD2	D Flip-Flop with Synchronous Clear, Scan, 2X Drive
FDS3	D Flip-Flop with Synchronous Set
FDS3D2	D Flip-Flop with Synchronous Set, 2X Drive
FDS3CS	D Flip-Flop with Synchronous Set, Scan Clock
FDS3CSD2	D Flip-Flop with Synchronous Set, Scan Clock, 2X Drive
FDS3S	Flip-Flop with Synchronous Set, Scan
FDS3SD2	Flip-Flop with Synchronous Set, Scan, 2x Drive
FJ1	JK Flip-Flop
FJ1D2	JK Flip-Flop with 2X Drive
FJ1S	JK Flip-Flop with Scan
FJ1SD2	JK Flip-Flop with Scan, 2X Drive
FJ2	JK Flip-Flop with Reset
FJ2D2	JK Flip-Flop with Reset, 2X Drive
FJ2S	JK Flip-Flop with Reset, Scan
FJ2SD2	JK Flip-Flop with Reset, Scan, 2X Drive

Cell List (Continued)

Cell Name	Function Description
FJ4	JK Flip-Flop with Reset, Set
FJ4D2	JK Flip-Flop with Reset, Set, 2X Drive
FJ4S	JK Flip-Flop with Reset, Set, Scan
FJ4SD2	JK Flip-Flop with Reset, Set, Scan, 2X Drive
FT2	Toggle Flip-Flop with Reset
FT2D2	Toggle Flip-Flop with Reset, 2X Drive

Logic Symbol



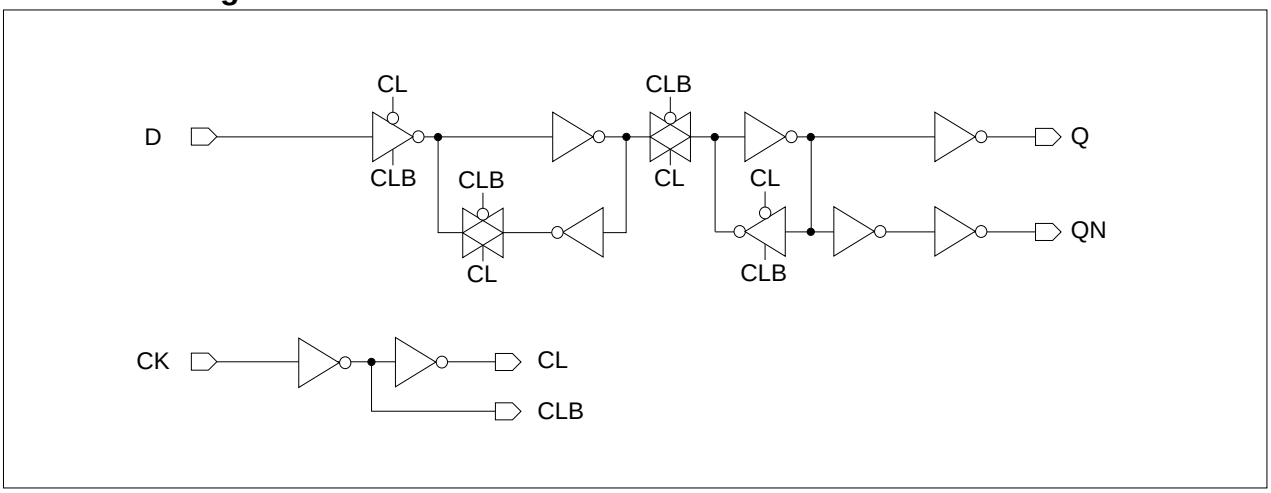
Truth Table

D	CK	Q (n+1)	QN (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
FD1		*FD1D2*		*FD1*	*FD1D2*
D	CK	D	CK		
0.7	0.7	0.7	0.7	5.33	5.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1	FD1D2
Pulse Width Low (CK)	t_{PWL}	0.421	0.423
Pulse Width High (CK)	t_{PWH}	0.394	0.408
Input Setup Time (D to CK)	t_{SU}	0.727	0.724
Input Hold Time (D to CK)	t_{HD}	0.092	0.092

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.146	0.074 + 0.036*SL	0.065 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.124	0.060 + 0.032*SL	0.056 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.403	0.365 + 0.019*SL	0.372 + 0.017*SL	0.374 + 0.017*SL
	t_{PHL}	0.402	0.361 + 0.020*SL	0.371 + 0.018*SL	0.376 + 0.018*SL
CK to QN	t_R	0.133	0.060 + 0.036*SL	0.052 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.114	0.052 + 0.031*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.468	0.432 + 0.018*SL	0.434 + 0.017*SL	0.435 + 0.017*SL
	t_{PHL}	0.470	0.431 + 0.019*SL	0.437 + 0.018*SL	0.439 + 0.018*SL

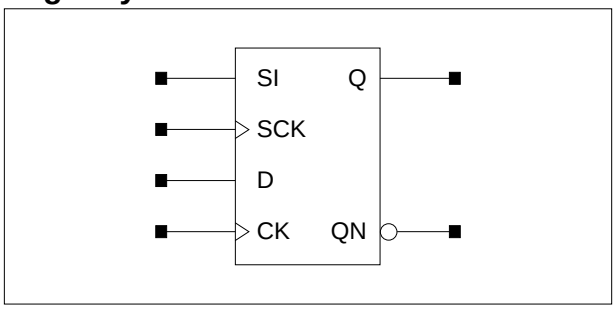
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.107	0.071 + 0.018*SL	0.067 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.090	0.058 + 0.016*SL	0.056 + 0.016*SL	0.030 + 0.017*SL
	t_{PLH}	0.403	0.380 + 0.011*SL	0.390 + 0.009*SL	0.397 + 0.009*SL
	t_{PHL}	0.397	0.373 + 0.012*SL	0.385 + 0.009*SL	0.398 + 0.009*SL
CK to QN	t_R	0.099	0.064 + 0.018*SL	0.058 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.085	0.054 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.510	0.489 + 0.011*SL	0.496 + 0.009*SL	0.499 + 0.009*SL
	t_{PHL}	0.506	0.484 + 0.011*SL	0.493 + 0.009*SL	0.501 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



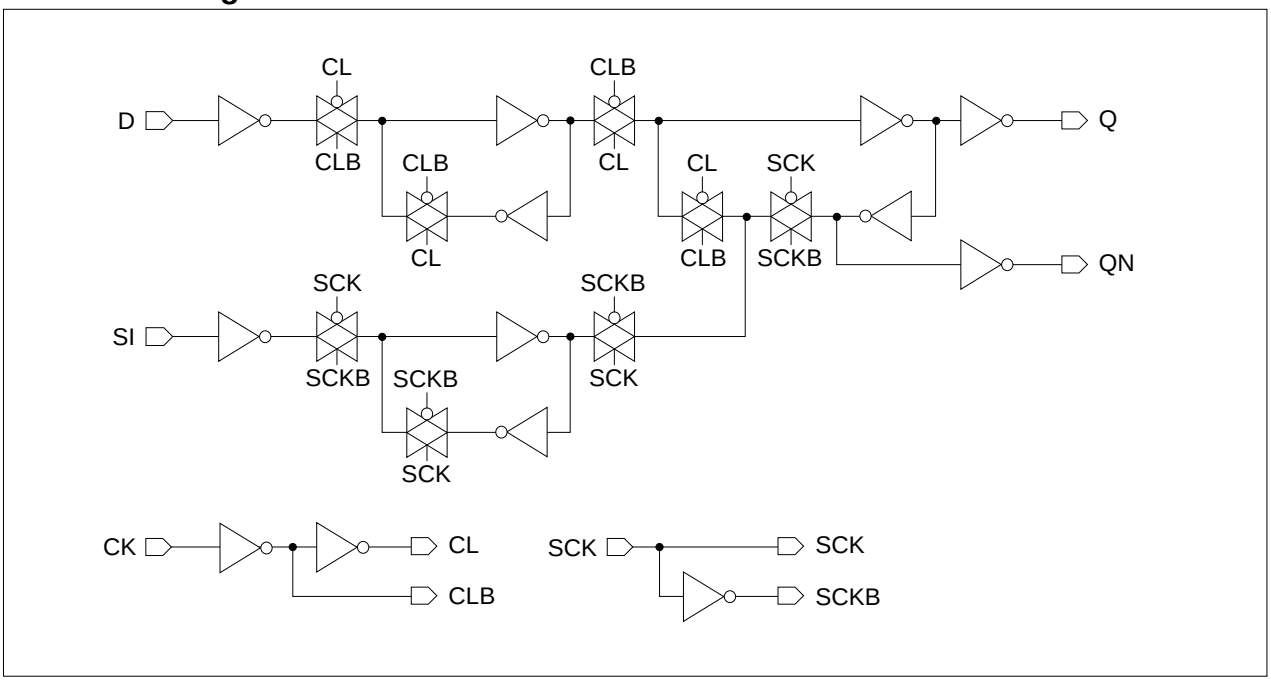
Truth Table

SI	SCK	D	CK	Q (n+1)	QN (n+1)
x	0	0	↑	0	1
x	0	1	↑	1	0
0	↑	x	0	0	1
1	↑	x	0	1	0
x	0	x	↓	Q(n)	QN(n)
x	↓	x	0	Q(n)	QN(n)

Cell Data

Input Load (SL)								Gate Count	
FD1CS				*FD1CSD2*				*FD1CS*	*FD1CSD2*
SI	SCK	D	CK	SI	SCK	D	CK		
0.8	1.9	0.8	0.8	0.8	1.9	0.8	0.8	8.00	8.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1CS	FD1CSD2
Pulse Width Low (CK)	t_{PWL}	0.381	0.382
Pulse Width High (CK)	t_{PWH}	0.428	0.449
Pulse Width Low (SCK)	t_{PWL}	0.373	0.374
Pulse Width High (SCK)	t_{PWH}	0.428	0.455
Input Setup Time (D to CK)	t_{SU}	0.515	0.516
Input Hold Time (D to CK)	t_{HD}	0.018	0.019
Input Setup Time (SI to SCK)	t_{SU}	1.208	1.207
Input Hold Time (SI to SCK)	t_{HD}	0.000	0.000

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD1CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.143	0.071 + 0.036*SL	0.063 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.123	0.060 + 0.031*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.418	0.380 + 0.019*SL	0.386 + 0.018*SL	0.389 + 0.017*SL
	t_{PHL}	0.431	0.390 + 0.020*SL	0.400 + 0.018*SL	0.404 + 0.018*SL
SCK to Q	t_R	0.152	0.081 + 0.035*SL	0.070 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.126	0.062 + 0.032*SL	0.057 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.432	0.393 + 0.019*SL	0.401 + 0.017*SL	0.404 + 0.017*SL
	t_{PHL}	0.372	0.332 + 0.020*SL	0.342 + 0.018*SL	0.347 + 0.018*SL
CK to QN	t_R	0.156	0.086 + 0.035*SL	0.075 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.131	0.066 + 0.033*SL	0.065 + 0.033*SL	0.044 + 0.033*SL
	t_{PLH}	0.562	0.521 + 0.020*SL	0.533 + 0.018*SL	0.536 + 0.017*SL
	t_{PHL}	0.533	0.490 + 0.021*SL	0.504 + 0.018*SL	0.515 + 0.018*SL
SCK to QN	t_R	0.136	0.064 + 0.036*SL	0.055 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.116	0.053 + 0.032*SL	0.047 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.452	0.415 + 0.018*SL	0.419 + 0.017*SL	0.419 + 0.017*SL
	t_{PHL}	0.510	0.471 + 0.020*SL	0.478 + 0.018*SL	0.480 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD1CSD2

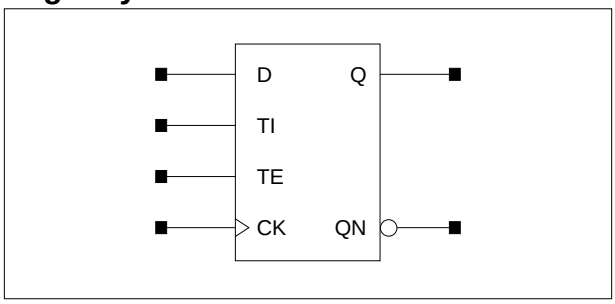
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.102	0.067 + 0.017*SL	0.060 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.088	0.056 + 0.016*SL	0.053 + 0.017*SL	0.028 + 0.017*SL
	t_{PLH}	0.413	0.391 + 0.011*SL	0.400 + 0.009*SL	0.406 + 0.009*SL
	t_{PHL}	0.426	0.402 + 0.012*SL	0.414 + 0.009*SL	0.425 + 0.009*SL
SCK to Q	t_R	0.110	0.074 + 0.018*SL	0.069 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.092	0.060 + 0.016*SL	0.057 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.428	0.406 + 0.011*SL	0.416 + 0.009*SL	0.423 + 0.009*SL
	t_{PHL}	0.375	0.351 + 0.012*SL	0.363 + 0.009*SL	0.376 + 0.009*SL
CK to QN	t_R	0.108	0.072 + 0.018*SL	0.068 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.092	0.058 + 0.017*SL	0.060 + 0.016*SL	0.034 + 0.017*SL
	t_{PLH}	0.560	0.537 + 0.012*SL	0.548 + 0.009*SL	0.555 + 0.009*SL
	t_{PHL}	0.538	0.513 + 0.012*SL	0.526 + 0.009*SL	0.544 + 0.009*SL
SCK to QN	t_R	0.094	0.060 + 0.017*SL	0.052 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.082	0.051 + 0.015*SL	0.047 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.473	0.452 + 0.010*SL	0.459 + 0.009*SL	0.462 + 0.009*SL
	t_{PHL}	0.527	0.504 + 0.011*SL	0.514 + 0.009*SL	0.521 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD1S/FD1SD2

D Flip-Flop with Scan, 1X/2X Drive

Logic Symbol



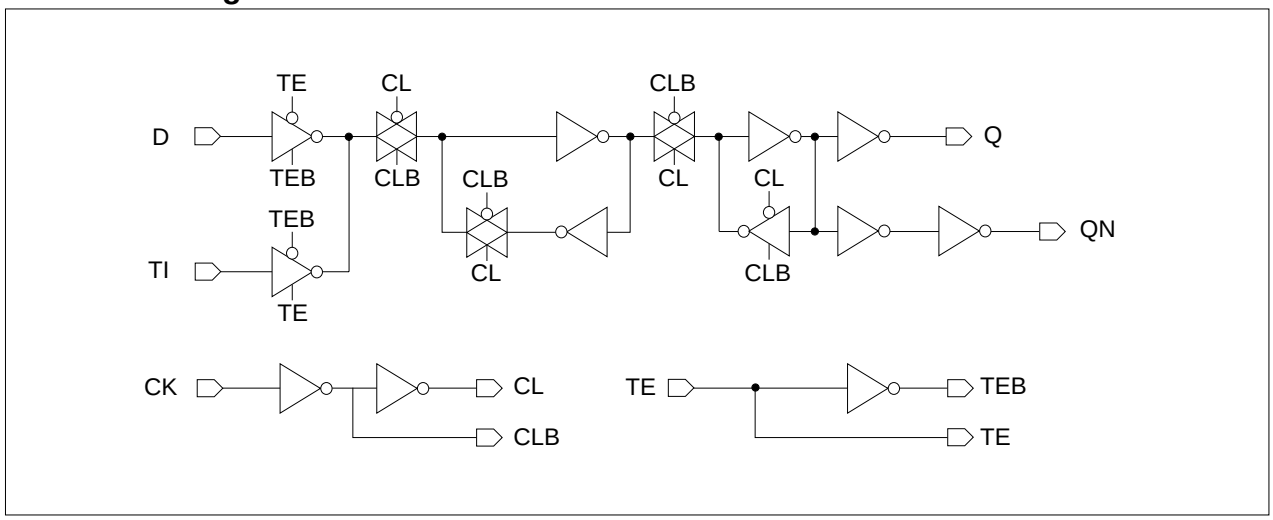
Truth Table

D	TI	TE	CK	Q (n+1)	QN (n+1)
0	x	0	↑	0	1
1	x	0	↑	1	0
x	0	1	↑	0	1
x	1	1	↑	1	0
x	x	x	↓	Q(n)	QN(n)

Cell Data

Input Load (SL)								Gate Count	
FD1S				*FD1SD2*				*FD1S*	*FD1SD2*
D	TI	TE	CK	D	TI	TE	CK		
0.7	0.7	1.3	0.7	0.7	0.7	1.3	0.7	6.67	6.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1S	FD1SD2
Pulse Width Low (CK)	t_{PWL}	0.399	0.399
Pulse Width High (CK)	t_{PWH}	0.391	0.404
Input Setup Time (D to CK)	t_{SU}	0.985	0.987
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (TI to CK)	t_{SU}	0.988	0.988
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	1.504	1.504
Input Hold Time (TE to CK)	t_{HD}	0.043	0.043

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.144	0.072 + 0.036*SL	0.063 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.121	0.058 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.398	0.360 + 0.019*SL	0.367 + 0.017*SL	0.369 + 0.017*SL
	t_{PHL}	0.394	0.354 + 0.020*SL	0.364 + 0.018*SL	0.368 + 0.018*SL
CK to QN	t_R	0.133	0.061 + 0.036*SL	0.051 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.113	0.049 + 0.032*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.459	0.423 + 0.018*SL	0.426 + 0.017*SL	0.426 + 0.017*SL
	t_{PHL}	0.464	0.426 + 0.019*SL	0.432 + 0.018*SL	0.433 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD1SD2

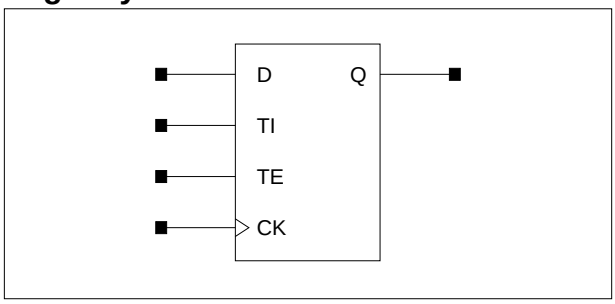
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.105	0.070 + 0.018*SL	0.064 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.087	0.054 + 0.016*SL	0.054 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.397	0.374 + 0.011*SL	0.384 + 0.009*SL	0.390 + 0.009*SL
	t_{PHL}	0.388	0.364 + 0.012*SL	0.376 + 0.009*SL	0.387 + 0.009*SL
CK to QN	t_R	0.099	0.064 + 0.017*SL	0.057 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.085	0.054 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.500	0.479 + 0.011*SL	0.486 + 0.009*SL	0.489 + 0.009*SL
	t_{PHL}	0.500	0.478 + 0.011*SL	0.488 + 0.009*SL	0.494 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD1SQ/FD1SQD2

D Flip-Flop with Scan, Q Output Only, 1X/2X Drive

Logic Symbol



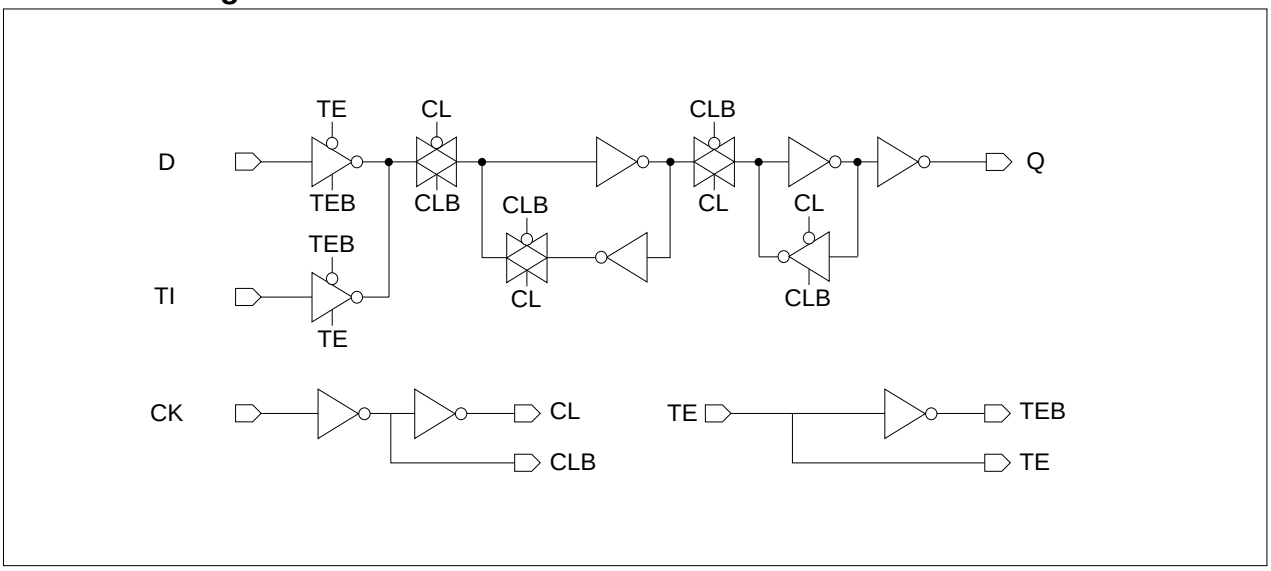
Truth Table

D	TI	TE	CK	Q (n+1)
0	x	0	↑	0
1	x	0	↑	1
x	0	1	↑	0
x	1	1	↑	1
x	x	x	↓	Q(n)

Cell Data

Input Load (SL)								Gate Count	
FD1SQ				*FD1SQD2*				*FD1SQ*	*FD1SQD2*
D	TI	TE	CK	D	TI	TE	CK		
0.7	0.7	1.3	0.7	0.7	0.7	1.3	0.7	5.67	6.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1SQ	FD1SQD2
Pulse Width Low (CK)	t_{PWL}	0.399	0.399
Pulse Width High (CK)	t_{PWH}	0.381	0.393
Input Setup Time (D to CK)	t_{SU}	0.985	0.985
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (TI to CK)	t_{SU}	0.988	0.988
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	1.054	1.054
Input Hold Time (TE to CK)	t_{HD}	0.043	0.043

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD1SQ

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.136	0.064 + 0.036*SL	0.055 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.116	0.052 + 0.032*SL	0.046 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.375	0.338 + 0.019*SL	0.343 + 0.017*SL	0.343 + 0.017*SL
	t_{PHL}	0.374	0.335 + 0.020*SL	0.342 + 0.018*SL	0.344 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD1SQD2

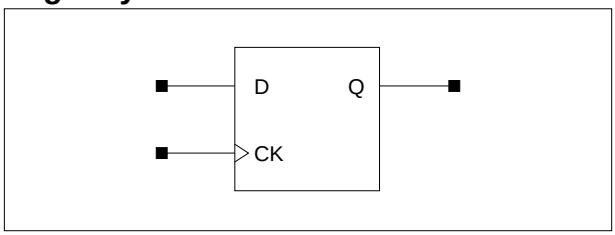
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.099	0.065 + 0.017*SL	0.057 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.080	0.047 + 0.017*SL	0.048 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.377	0.355 + 0.011*SL	0.363 + 0.009*SL	0.366 + 0.009*SL
	t_{PHL}	0.369	0.346 + 0.012*SL	0.357 + 0.009*SL	0.364 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD1Q/FD1QD2

D Flip-Flop with Q Output Only, 1X/2X Drive

Logic Symbol



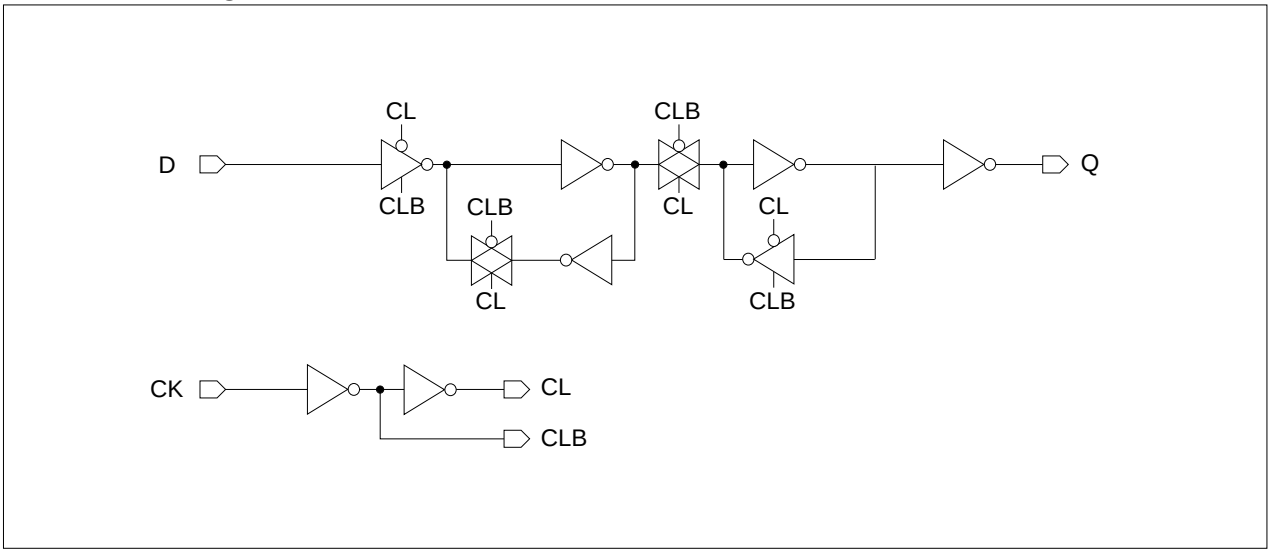
Truth Table

D	CK	Q (n+1)
0	↑	0
1	↑	1
x	↓	Q (n)

Cell Data

Input Load (SL)				Gate Count	
FD1Q		*FD1QD2*		*FD1Q*	*FD1QD2*
D	CK	D	CK		
0.7	0.7	0.7	0.7	4.33	4.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1Q	FD1QD2
Pulse Width Low (CK)	t_{PWL}	0.424	0.423
Pulse Width High (CK)	t_{PWH}	0.383	0.396
Input Setup Time (D to CK)	t_{SU}	0.725	0.724
Input Hold Time (D to CK)	t_{HD}	0.092	0.092

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD1Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.138	0.066 + 0.036*SL	0.056 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.052 + 0.032*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.378	0.342 + 0.018*SL	0.346 + 0.017*SL	0.346 + 0.017*SL
	t_{PHL}	0.380	0.341 + 0.019*SL	0.348 + 0.018*SL	0.350 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD1QD2

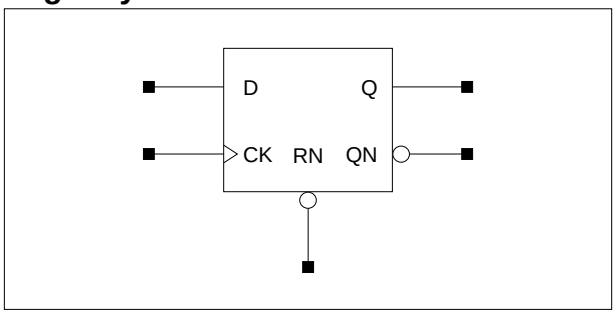
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.099	0.064 + 0.018*SL	0.058 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.082	0.048 + 0.017*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.380	0.359 + 0.011*SL	0.367 + 0.009*SL	0.370 + 0.009*SL
	t_{PHL}	0.377	0.354 + 0.012*SL	0.364 + 0.009*SL	0.372 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD2/FD2D2

D Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



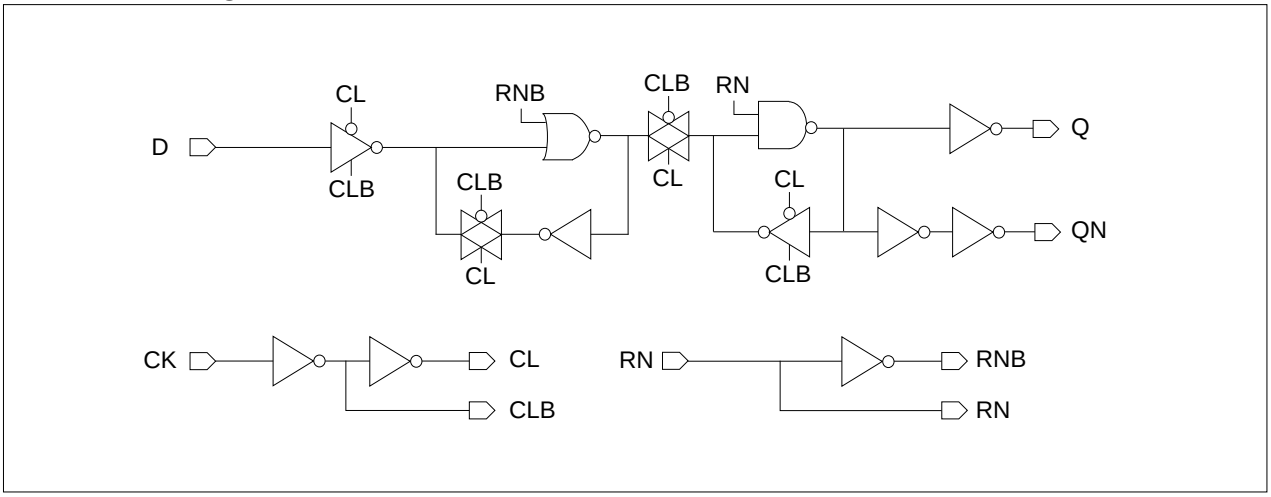
Truth Table

D	CK	RN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FD2			*FD2D2*			*FD2*	*FD2D2*
D	CK	RN	D	CK	RN		
0.7	0.7	1.8	0.7	0.7	1.9	6.33	6.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2	FD2D2
Pulse Width Low (CK)	t_{PWL}	0.428	0.429
Pulse Width High (CK)	t_{PWH}	0.401	0.419
Pulse Width Low (RN)	t_{PWL}	0.352	0.381
Input Setup Time (D to CK)	t_{SU}	0.734	0.734
Input Hold Time (D to CK)	t_{HD}	0.055	0.055
Recovery Time (RN)	t_{RC}	0.307	0.306
Removal Time (RN)	t_{RM}	0.094	0.094

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.158	0.085 + 0.036*SL	0.079 + 0.038*SL	0.056 + 0.039*SL
	t_F	0.132	0.068 + 0.032*SL	0.064 + 0.033*SL	0.041 + 0.034*SL
	t_{PLH}	0.423	0.382 + 0.020*SL	0.393 + 0.018*SL	0.400 + 0.017*SL
	t_{PHL}	0.421	0.379 + 0.021*SL	0.391 + 0.018*SL	0.398 + 0.018*SL
RN to Q	t_F	0.135	0.073 + 0.031*SL	0.066 + 0.033*SL	0.039 + 0.034*SL
	t_{PHL}	0.252	0.210 + 0.021*SL	0.223 + 0.018*SL	0.227 + 0.018*SL
CK to QN	t_R	0.134	0.061 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.116	0.053 + 0.031*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.486	0.450 + 0.018*SL	0.453 + 0.017*SL	0.453 + 0.017*SL
	t_{PHL}	0.488	0.449 + 0.019*SL	0.455 + 0.018*SL	0.457 + 0.018*SL
RN to QN	t_R	0.134	0.062 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_{PLH}	0.318	0.282 + 0.018*SL	0.285 + 0.017*SL	0.285 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD2D2

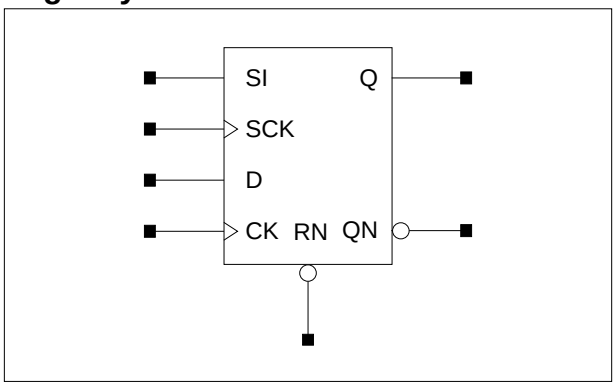
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.121	0.084 + 0.019*SL	0.083 + 0.019*SL	0.051 + 0.019*SL
	t_F	0.102	0.068 + 0.017*SL	0.070 + 0.016*SL	0.038 + 0.017*SL
	t_{PLH}	0.427	0.403 + 0.012*SL	0.416 + 0.009*SL	0.434 + 0.009*SL
	t_{PHL}	0.422	0.396 + 0.013*SL	0.411 + 0.009*SL	0.430 + 0.009*SL
RN to Q	t_F	0.107	0.074 + 0.016*SL	0.074 + 0.016*SL	0.031 + 0.017*SL
	t_{PHL}	0.252	0.226 + 0.013*SL	0.241 + 0.009*SL	0.254 + 0.009*SL
CK to QN	t_R	0.102	0.067 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.088	0.058 + 0.015*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.540	0.519 + 0.011*SL	0.526 + 0.009*SL	0.529 + 0.009*SL
	t_{PHL}	0.538	0.515 + 0.011*SL	0.525 + 0.009*SL	0.532 + 0.009*SL
RN to QN	t_R	0.101	0.067 + 0.017*SL	0.059 + 0.019*SL	0.035 + 0.020*SL
	t_{PLH}	0.370	0.349 + 0.011*SL	0.356 + 0.009*SL	0.358 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD2CS/FD2CSD2

D Flip-Flop with Reset, Scan Clock, 1X/2X Drive

Logic Symbol



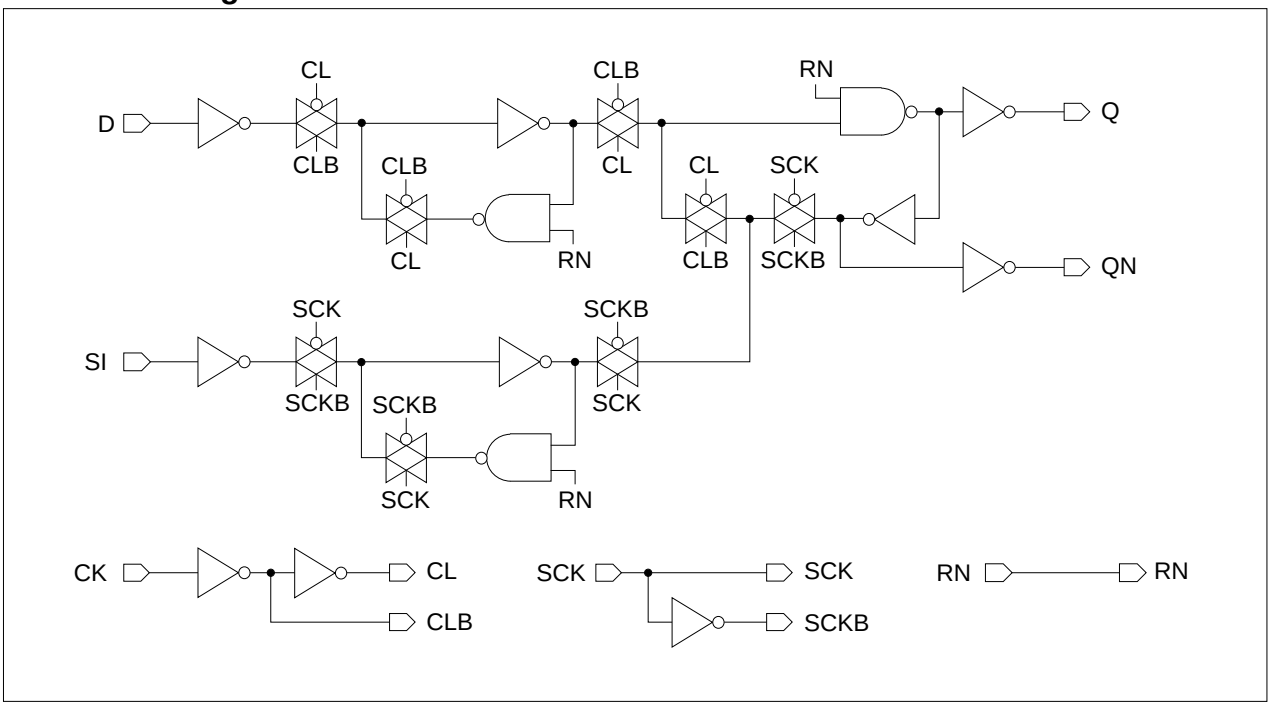
Truth Table

SI	SCK	D	CK	RN	Q (n+1)	QN (n+1)
x	0	0	↑	1	0	1
x	0	1	↑	1	1	0
0	↑	x	0	1	0	1
1	↑	x	0	1	1	0
x	x	x	x	0	0	1
x	↓	x	0	1	Q(n)	QN(n)
x	0	x	↓	1	Q(n)	QN(n)

Cell Data

Input Load (SL)										Gate Count	
FD2CS					*FD2CSD2*					*FD2CS*	*FD2CSD2*
SI	SCK	D	CK	RN	SI	SCK	D	CK	RN		
0.8	2.0	0.8	0.8	2.7	0.8	2.0	0.8	0.8	3.0	10.00	10.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2CS	FD2CSD2
Input Setup Time (D to CK)	t_{SU}	0.509	0.510
Input Hold Time (D to CK)	t_{HD}	0.024	0.025
Input Setup Time (SI to SCK)	t_{SU}	1.179	1.178
Input Hold Time (SI to SCK)	t_{HD}	0.000	0.000
Pulse Width High (CK)	t_{PWH}	0.453	0.478
Pulse Width Low (CK)	t_{PWL}	0.383	0.384
Pulse Width High (SCK)	t_{PWH}	0.459	0.494
Pulse Width Low (SCK)	t_{PWL}	0.385	0.387
Pulse Width Low (RN)	t_{PWL}	0.402	0.417
Removal Time (RN to CK)	t_{RM}	0.848	0.833
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to SCK)	t_{RM}	0.820	0.815
Recovery Time (RN to SCK)	t_{RC}	0.000	0.000

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD2CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.159	0.087 + 0.036*SL	0.081 + 0.038*SL	0.059 + 0.038*SL
	t_F	0.126	0.064 + 0.031*SL	0.058 + 0.032*SL	0.039 + 0.033*SL
	t_{PLH}	0.461	0.421 + 0.020*SL	0.432 + 0.017*SL	0.441 + 0.017*SL
	t_{PHL}	0.449	0.409 + 0.020*SL	0.419 + 0.017*SL	0.424 + 0.017*SL
SCK to Q	t_R	0.166	0.095 + 0.036*SL	0.088 + 0.037*SL	0.060 + 0.038*SL
	t_F	0.129	0.067 + 0.031*SL	0.062 + 0.032*SL	0.039 + 0.033*SL
	t_{PLH}	0.477	0.436 + 0.021*SL	0.449 + 0.017*SL	0.458 + 0.017*SL
	t_{PHL}	0.402	0.362 + 0.020*SL	0.372 + 0.017*SL	0.378 + 0.017*SL
RN to Q	t_F	0.127	0.066 + 0.031*SL	0.060 + 0.032*SL	0.041 + 0.033*SL
	t_{PHL}	0.223	0.183 + 0.020*SL	0.193 + 0.017*SL	0.200 + 0.017*SL
CK to QN	t_R	0.160	0.090 + 0.035*SL	0.081 + 0.037*SL	0.053 + 0.038*SL
	t_F	0.137	0.074 + 0.031*SL	0.071 + 0.032*SL	0.049 + 0.033*SL
	t_{PLH}	0.587	0.546 + 0.020*SL	0.558 + 0.017*SL	0.562 + 0.017*SL
	t_{PHL}	0.583	0.540 + 0.021*SL	0.554 + 0.018*SL	0.568 + 0.017*SL
SCK to QN	t_R	0.139	0.068 + 0.036*SL	0.058 + 0.038*SL	0.047 + 0.038*SL
	t_F	0.120	0.059 + 0.031*SL	0.052 + 0.032*SL	0.036 + 0.033*SL
	t_{PLH}	0.481	0.445 + 0.018*SL	0.448 + 0.017*SL	0.449 + 0.017*SL
	t_{PHL}	0.552	0.514 + 0.019*SL	0.521 + 0.017*SL	0.523 + 0.017*SL
RN to QN	t_R	0.187	0.111 + 0.038*SL	0.114 + 0.037*SL	0.080 + 0.038*SL
	t_{PLH}	0.400	0.353 + 0.023*SL	0.375 + 0.018*SL	0.399 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD2CSD2

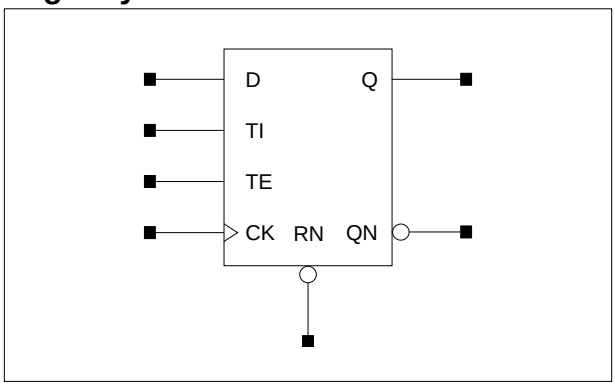
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.119	0.083 + 0.018*SL	0.079 + 0.019*SL	0.052 + 0.019*SL
	t_F	0.091	0.059 + 0.016*SL	0.059 + 0.016*SL	0.033 + 0.017*SL
	t_{PLH}	0.459	0.435 + 0.012*SL	0.447 + 0.009*SL	0.464 + 0.009*SL
	t_{PHL}	0.450	0.427 + 0.012*SL	0.439 + 0.009*SL	0.452 + 0.009*SL
SCK to Q	t_R	0.125	0.089 + 0.018*SL	0.087 + 0.019*SL	0.054 + 0.019*SL
	t_F	0.097	0.065 + 0.016*SL	0.064 + 0.016*SL	0.033 + 0.017*SL
	t_{PLH}	0.477	0.453 + 0.012*SL	0.466 + 0.009*SL	0.484 + 0.009*SL
	t_{PHL}	0.410	0.386 + 0.012*SL	0.398 + 0.009*SL	0.411 + 0.009*SL
RN to Q	t_F	0.092	0.060 + 0.016*SL	0.061 + 0.016*SL	0.034 + 0.016*SL
	t_{PHL}	0.213	0.189 + 0.012*SL	0.201 + 0.009*SL	0.215 + 0.009*SL
CK to QN	t_R	0.113	0.077 + 0.018*SL	0.073 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.098	0.066 + 0.016*SL	0.067 + 0.016*SL	0.040 + 0.016*SL
	t_{PLH}	0.586	0.563 + 0.011*SL	0.574 + 0.009*SL	0.582 + 0.009*SL
	t_{PHL}	0.594	0.569 + 0.012*SL	0.582 + 0.009*SL	0.602 + 0.009*SL
SCK to QN	t_R	0.096	0.061 + 0.018*SL	0.055 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.085	0.053 + 0.016*SL	0.053 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.506	0.486 + 0.010*SL	0.492 + 0.009*SL	0.494 + 0.009*SL
	t_{PHL}	0.579	0.557 + 0.011*SL	0.567 + 0.009*SL	0.574 + 0.009*SL
RN to QN	t_R	0.127	0.089 + 0.019*SL	0.090 + 0.019*SL	0.064 + 0.019*SL
	t_{PLH}	0.373	0.348 + 0.013*SL	0.362 + 0.009*SL	0.394 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD2S/FD2SD2

D Flip-Flop with Reset, Scan, 1X/2X Drive

Logic Symbol



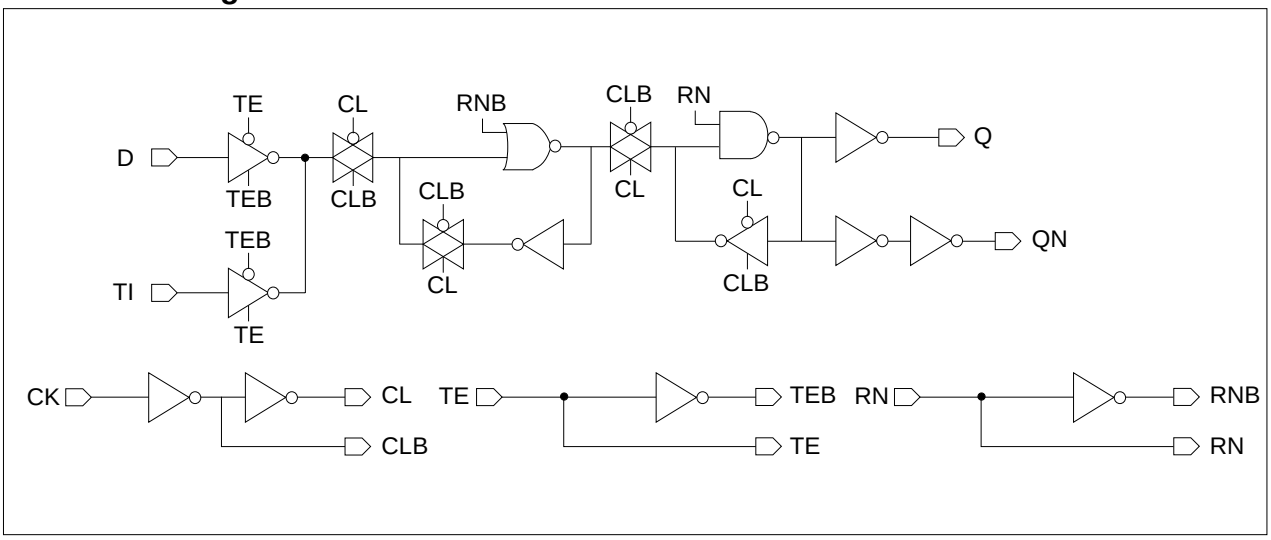
Truth Table

D	TI	TE	CK	RN	Q (n+1)	QN (n+1)
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	0	1
x	x	x	↓	1	Q(n)	QN(n)

Cell Data

Input Load (SL)										Gate Count	
FD2S					*FD2SD2*					*FD2S*	*FD2SD2*
D	TI	TE	CK	RN	D	TI	TE	CK	RN		
0.7	0.7	1.2	0.7	1.8	0.7	0.7	1.2	0.7	1.8	8.00	8.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2S	FD2SD2
Pulse Width Low (CK)	t_{PWL}	0.416	0.416
Pulse Width High (CK)	t_{PWH}	0.401	0.420
Pulse Width Low (RN)	t_{PWL}	0.352	0.381
Input Setup Time (D to CK)	t_{SU}	0.977	0.975
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (TI to CK)	t_{SU}	0.979	0.977
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	1.053	1.053
Input Hold Time (TE to CK)	t_{HD}	0.037	0.038
Recovery Time (RN)	t_{RC}	0.304	0.304
Removal Time (RN)	t_{RM}	0.096	0.096

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.158	0.085 + 0.036*SL	0.079 + 0.038*SL	0.056 + 0.039*SL
	t_F	0.132	0.068 + 0.032*SL	0.064 + 0.033*SL	0.041 + 0.034*SL
	t_{PLH}	0.425	0.384 + 0.020*SL	0.396 + 0.018*SL	0.403 + 0.017*SL
	t_{PHL}	0.424	0.382 + 0.021*SL	0.394 + 0.018*SL	0.401 + 0.018*SL
RN to Q	t_F	0.135	0.073 + 0.031*SL	0.066 + 0.033*SL	0.039 + 0.034*SL
	t_{PHL}	0.252	0.210 + 0.021*SL	0.223 + 0.018*SL	0.227 + 0.018*SL
CK to QN	t_R	0.134	0.061 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.115	0.051 + 0.032*SL	0.046 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.489	0.453 + 0.018*SL	0.456 + 0.017*SL	0.456 + 0.017*SL
	t_{PHL}	0.490	0.452 + 0.019*SL	0.458 + 0.018*SL	0.460 + 0.018*SL
RN to QN	t_R	0.135	0.063 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_{PLH}	0.318	0.282 + 0.018*SL	0.285 + 0.017*SL	0.285 + 0.017*SL

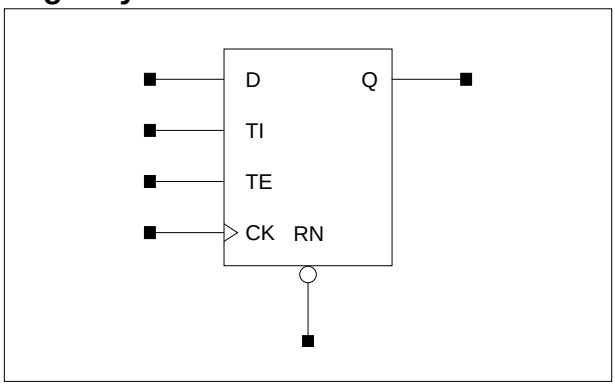
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.121	0.084 + 0.019*SL	0.082 + 0.019*SL	0.051 + 0.019*SL
	t_F	0.102	0.070 + 0.016*SL	0.070 + 0.016*SL	0.038 + 0.017*SL
	t_{PLH}	0.430	0.405 + 0.012*SL	0.418 + 0.009*SL	0.436 + 0.009*SL
	t_{PHL}	0.425	0.399 + 0.013*SL	0.414 + 0.009*SL	0.433 + 0.009*SL
RN to Q	t_F	0.107	0.074 + 0.016*SL	0.074 + 0.016*SL	0.031 + 0.017*SL
	t_{PHL}	0.252	0.226 + 0.013*SL	0.241 + 0.009*SL	0.254 + 0.009*SL
CK to QN	t_R	0.102	0.067 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.088	0.057 + 0.016*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.543	0.522 + 0.011*SL	0.529 + 0.009*SL	0.532 + 0.009*SL
	t_{PHL}	0.540	0.517 + 0.012*SL	0.527 + 0.009*SL	0.534 + 0.009*SL
RN to QN	t_R	0.101	0.067 + 0.017*SL	0.059 + 0.019*SL	0.035 + 0.020*SL
	t_{PLH}	0.370	0.349 + 0.011*SL	0.356 + 0.009*SL	0.358 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



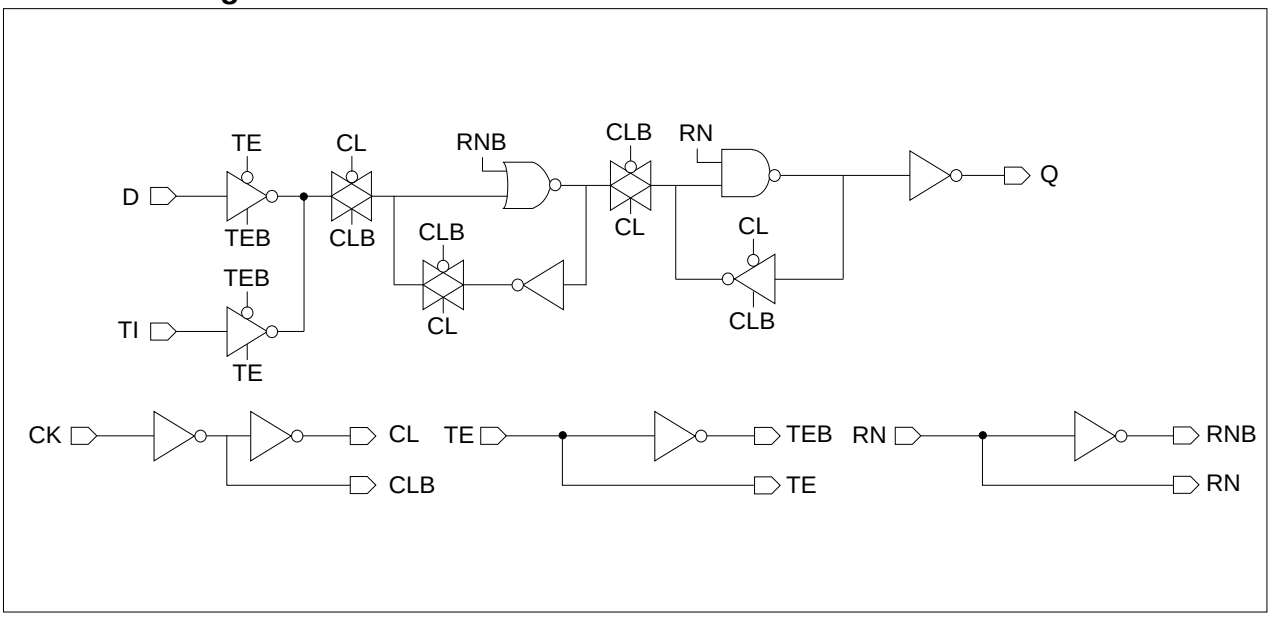
Truth Table

D	TI	TE	CK	RN	Q (n+1)
0	x	0	↑	1	0
1	x	0	↑	1	1
x	0	1	↑	1	0
x	1	1	↑	1	1
x	x	x	x	0	0
x	x	x	↓	1	Q(n)

Cell Data

Input Load (SL)										Gate Count	
FD2SQ					*FD2SQD2*					*FD2SQ*	*FD2SQD2*
D	TI	TE	CK	RN	D	TI	TE	CK	RN		
0.7	0.7	1.2	0.7	1.8	0.7	0.7	1.2	0.7	1.8	7.33	7.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2SQ	FD2SQD2
Pulse Width Low (CK)	t_{PWL}	0.416	0.416
Pulse Width High (CK)	t_{PWH}	0.388	0.403
Pulse Width Low (RN)	t_{PWL}	0.327	0.353
Input Setup Time (D to CK)	t_{SU}	0.973	0.973
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (TI to CK)	t_{SU}	0.975	0.973
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	1.040	1.049
Input Hold Time (TE to CK)	t_{HD}	0.044	0.044
Recovery Time (RN)	t_{RC}	0.300	0.299
Removal Time (RN)	t_{RM}	0.100	0.100

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD2SQ

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.148	0.077 + 0.036*SL	0.067 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.123	0.059 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.396	0.357 + 0.020*SL	0.365 + 0.018*SL	0.368 + 0.017*SL
	t_{PHL}	0.399	0.359 + 0.020*SL	0.368 + 0.018*SL	0.371 + 0.018*SL
RN to Q	t_F	0.126	0.063 + 0.031*SL	0.056 + 0.033*SL	0.036 + 0.034*SL
	t_{PHL}	0.225	0.185 + 0.020*SL	0.194 + 0.018*SL	0.197 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD2SQD2

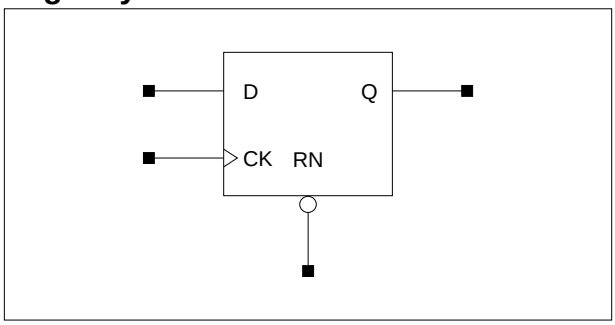
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.111	0.074 + 0.018*SL	0.071 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.090	0.055 + 0.017*SL	0.058 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.400	0.377 + 0.012*SL	0.388 + 0.009*SL	0.398 + 0.009*SL
	t_{PHL}	0.399	0.375 + 0.012*SL	0.387 + 0.009*SL	0.398 + 0.009*SL
RN to Q	t_F	0.094	0.062 + 0.016*SL	0.061 + 0.016*SL	0.027 + 0.017*SL
	t_{PHL}	0.224	0.200 + 0.012*SL	0.212 + 0.009*SL	0.222 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD2Q/FD2QD2

D Flip-Flop with Reset, Q Output Only, 1X/2X Drive

Logic Symbol



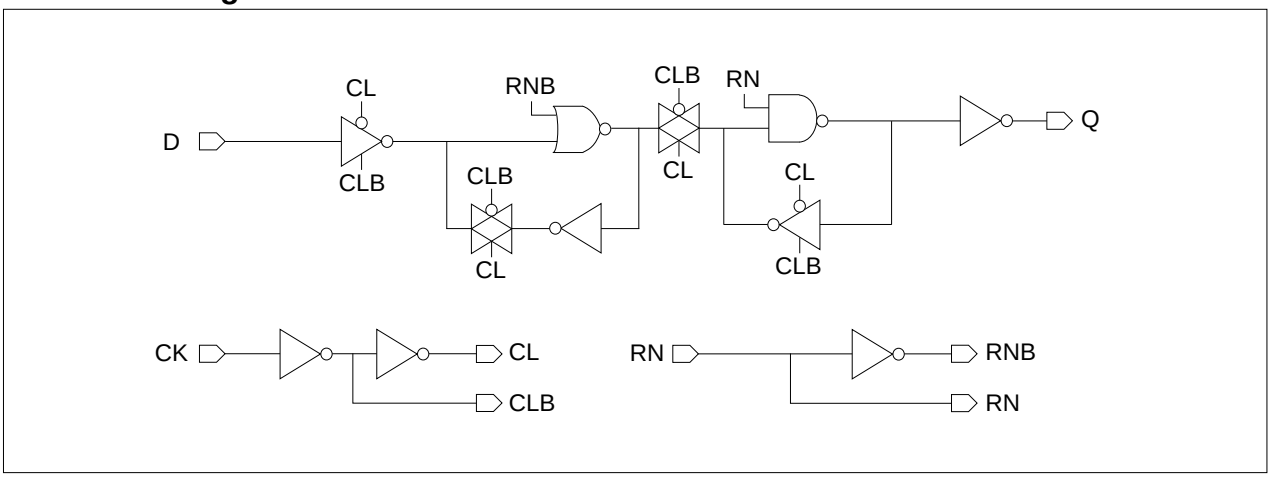
Truth Table

D	CK	RN	Q (n+1)
0	↑	1	0
1	↑	1	1
x	x	0	0
x	↓	x	Q (n)

Cell Data

Input Load (SL)						Gate Count	
FD2Q			*FD2QD2*			*FD2Q*	*FD2QD2*
D	CK	RN	D	CK	RN		
0.7	0.7	1.9	0.7	0.7	1.8	5.67	5.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2Q	FD2QD2
Pulse Width Low (CK)	t_{PWL}	0.429	0.429
Pulse Width High (CK)	t_{PWH}	0.387	0.403
Pulse Width Low (RN)	t_{PWL}	0.327	0.353
Input Setup Time (D to CK)	t_{SU}	0.729	0.727
Input Hold Time (D to CK)	t_{HD}	0.057	0.058
Recovery Time (RN)	t_{RC}	0.301	0.300
Removal Time (RN)	t_{RM}	0.099	0.100

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD2Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.147	0.075 + 0.036*SL	0.067 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.123	0.059 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.393	0.354 + 0.020*SL	0.362 + 0.018*SL	0.365 + 0.017*SL
	t_{PHL}	0.396	0.356 + 0.020*SL	0.365 + 0.018*SL	0.368 + 0.018*SL
RN to Q	t_F	0.126	0.064 + 0.031*SL	0.057 + 0.033*SL	0.036 + 0.034*SL
	t_{PHL}	0.225	0.185 + 0.020*SL	0.194 + 0.018*SL	0.197 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD2QD2

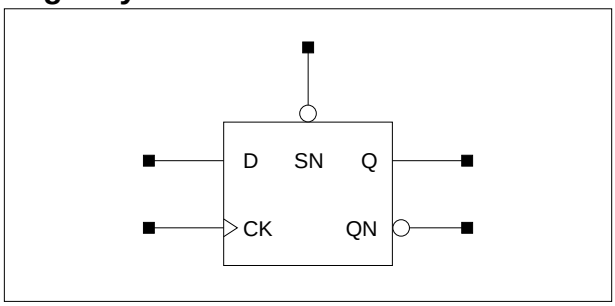
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.110	0.074 + 0.018*SL	0.071 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.089	0.055 + 0.017*SL	0.057 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.398	0.375 + 0.012*SL	0.386 + 0.009*SL	0.396 + 0.009*SL
	t_{PHL}	0.396	0.372 + 0.012*SL	0.385 + 0.009*SL	0.396 + 0.009*SL
RN to Q	t_F	0.094	0.062 + 0.016*SL	0.061 + 0.016*SL	0.027 + 0.017*SL
	t_{PHL}	0.224	0.199 + 0.012*SL	0.212 + 0.009*SL	0.221 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD3/FD3D2

D Flip-Flop with Set, 1X/2X Drive

Logic Symbol



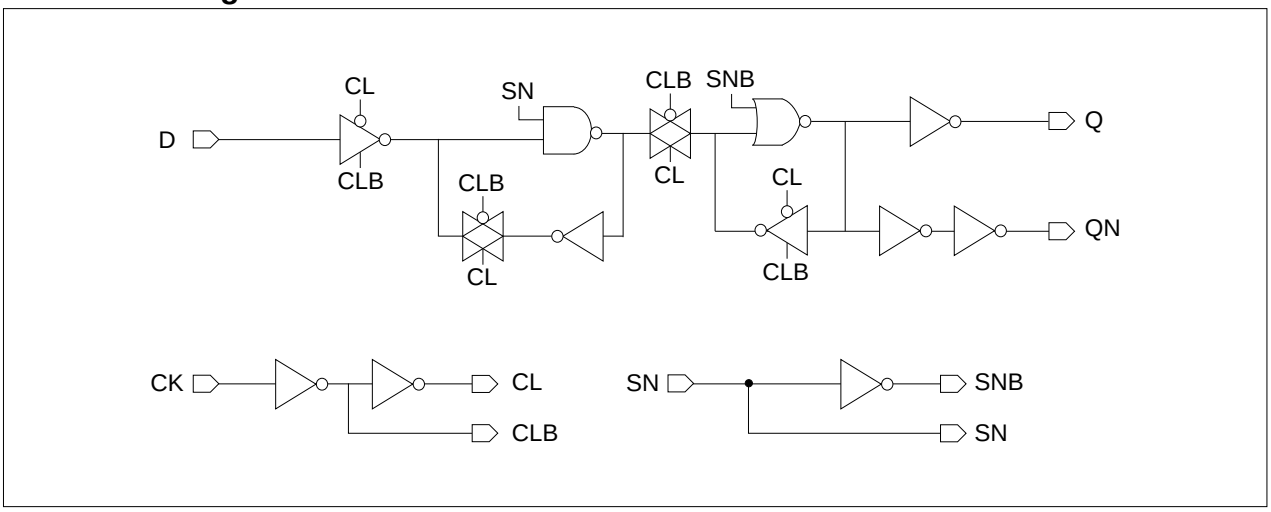
Truth Table

D	CK	SN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FD3			*FD3D2*			*FD3*	*FD3D2*
D	CK	SN	D	CK	SN		
0.7	0.7	2.0	0.7	0.7	2.0	7.00	7.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3	FD3D2
Pulse Width Low (CK)	t_{PWL}	0.455	0.455
Pulse Width High (CK)	t_{PWH}	0.397	0.411
Pulse Width Low (SN)	t_{PWL}	0.404	0.425
Input Setup Time (D to CK)	t_{SU}	0.763	0.763
Input Hold Time (D to CK)	t_{HD}	0.058	0.058
Recovery Time (SN)	t_{RC}	0.010	0.010
Removal Time (SN)	t_{HD}	0.389	0.389

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.149	0.078 + 0.035*SL	0.067 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.157	0.090 + 0.034*SL	0.095 + 0.032*SL	0.061 + 0.033*SL
	t_{PLH}	0.426	0.388 + 0.019*SL	0.395 + 0.017*SL	0.397 + 0.017*SL
	t_{PHL}	0.511	0.463 + 0.024*SL	0.485 + 0.018*SL	0.508 + 0.018*SL
SN to Q	t_R	0.140	0.067 + 0.036*SL	0.060 + 0.038*SL	0.047 + 0.039*SL
	t_{PLH}	0.270	0.232 + 0.019*SL	0.238 + 0.018*SL	0.241 + 0.017*SL
CK to QN	t_R	0.139	0.068 + 0.035*SL	0.056 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.115	0.053 + 0.031*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.584	0.547 + 0.018*SL	0.551 + 0.017*SL	0.550 + 0.017*SL
	t_{PHL}	0.494	0.455 + 0.019*SL	0.461 + 0.018*SL	0.463 + 0.018*SL
SN to QN	t_F	0.114	0.052 + 0.031*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PHL}	0.337	0.299 + 0.019*SL	0.305 + 0.018*SL	0.306 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD3D2

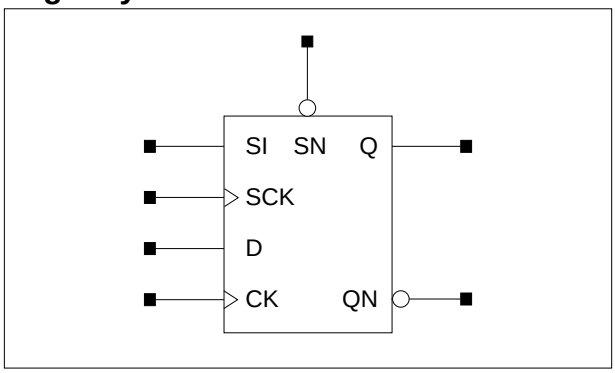
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.113	0.077 + 0.018*SL	0.072 + 0.019*SL	0.039 + 0.019*SL
	t_F	0.136	0.101 + 0.017*SL	0.106 + 0.016*SL	0.071 + 0.017*SL
	t_{PLH}	0.429	0.406 + 0.011*SL	0.417 + 0.009*SL	0.425 + 0.009*SL
	t_{PHL}	0.525	0.495 + 0.015*SL	0.517 + 0.010*SL	0.563 + 0.009*SL
SN to Q	t_R	0.103	0.067 + 0.018*SL	0.062 + 0.019*SL	0.037 + 0.019*SL
	t_{PLH}	0.269	0.246 + 0.011*SL	0.256 + 0.009*SL	0.264 + 0.009*SL
CK to QN	t_R	0.108	0.074 + 0.017*SL	0.066 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.085	0.054 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.661	0.640 + 0.011*SL	0.648 + 0.009*SL	0.651 + 0.009*SL
	t_{PHL}	0.535	0.512 + 0.011*SL	0.522 + 0.009*SL	0.529 + 0.009*SL
SN to QN	t_F	0.083	0.050 + 0.017*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PHL}	0.373	0.350 + 0.011*SL	0.360 + 0.009*SL	0.367 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD3CS/FD3CSD2

D Flip-Flop with Set, Scan Clock, 1X/2X Drive

Logic Symbol



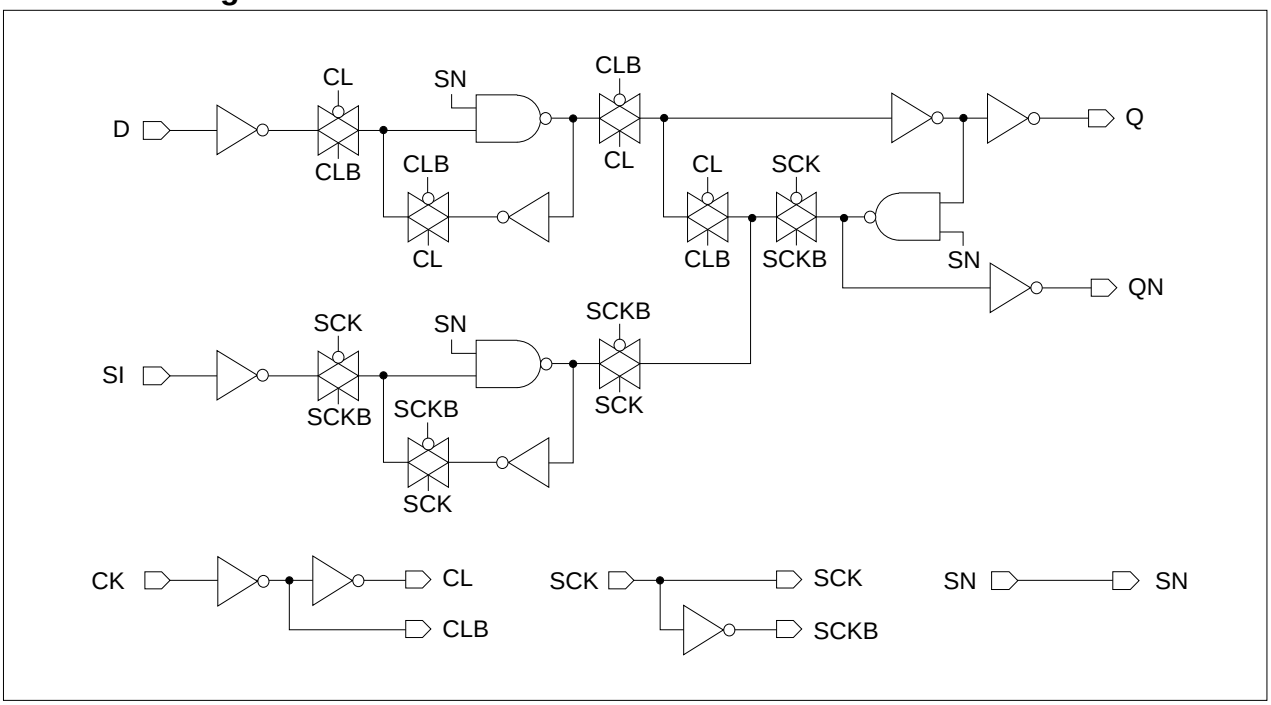
Truth Table

SI	SCK	D	CK	SN	Q (n+1)	QN (n+1)
x	0	0	↑	1	0	1
x	0	1	↑	1	1	0
0	↑	x	0	1	0	1
1	↑	x	0	1	1	0
x	x	x	x	0	1	0
x	0	x	↓	1	Q(n)	QN(n)
x	↓	x	0	1	Q(n)	QN(n)

Cell Data

Input Load (SL)										Gate Count	
FD3CS					*FD3CSD2*					*FD3CS*	*FD3CSD2*
SI	SCK	D	CK	SN	SI	SCK	D	CK	SN		
0.8	1.9	0.8	0.8	2.7	0.8	1.9	0.8	0.8	2.9	10.33	10.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3CS	FD3CSD2
Pulse Width Low (CK)	t_{PWL}	0.407	0.409
Pulse Width High (CK)	t_{PWH}	0.444	0.467
Pulse Width Low (SCK)	t_{PWL}	0.398	0.399
Pulse Width High (SCK)	t_{PWH}	0.465	0.506
Pulse Width Low (SN)	t_{PWL}	0.442	0.459
Input Setup Time (D to CK)	t_{SU}	0.569	0.571
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (SI to SCK)	t_{SU}	1.257	1.255
Input Hold Time (SI to SCK)	t_{HD}	0.000	0.000
Recovery Time (SN to CK)	t_{RC}	0.099	0.103
Removal Time (SN to CK)	t_{RM}	0.299	0.296
Recovery Time (SN to SCK)	t_{RC}	0.332	0.334
Removal Time (SN to SCK)	t_{RM}	0.068	0.067

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD3CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.147	0.076 + 0.035*SL	0.065 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.126	0.064 + 0.031*SL	0.057 + 0.033*SL	0.040 + 0.034*SL
	t_{PLH}	0.436	0.397 + 0.019*SL	0.404 + 0.018*SL	0.407 + 0.017*SL
	t_{PHL}	0.462	0.421 + 0.020*SL	0.431 + 0.018*SL	0.437 + 0.018*SL
SCK to Q	t_R	0.155	0.086 + 0.035*SL	0.073 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.131	0.069 + 0.031*SL	0.062 + 0.033*SL	0.041 + 0.034*SL
	t_{PLH}	0.452	0.413 + 0.019*SL	0.421 + 0.018*SL	0.424 + 0.017*SL
	t_{PHL}	0.426	0.385 + 0.020*SL	0.396 + 0.018*SL	0.402 + 0.018*SL
SN to Q	t_R	0.156	0.088 + 0.034*SL	0.072 + 0.038*SL	0.048 + 0.039*SL
	t_{PLH}	0.511	0.472 + 0.020*SL	0.481 + 0.017*SL	0.481 + 0.017*SL
CK to QN	t_R	0.182	0.108 + 0.037*SL	0.106 + 0.037*SL	0.068 + 0.038*SL
	t_F	0.139	0.074 + 0.033*SL	0.074 + 0.033*SL	0.051 + 0.033*SL
	t_{PLH}	0.656	0.611 + 0.023*SL	0.630 + 0.018*SL	0.646 + 0.017*SL
	t_{PHL}	0.570	0.525 + 0.022*SL	0.541 + 0.018*SL	0.557 + 0.018*SL
SCK to QN	t_R	0.152	0.080 + 0.036*SL	0.072 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.123	0.060 + 0.031*SL	0.054 + 0.033*SL	0.035 + 0.034*SL
	t_{PLH}	0.549	0.508 + 0.020*SL	0.519 + 0.018*SL	0.522 + 0.017*SL
	t_{PHL}	0.545	0.504 + 0.020*SL	0.514 + 0.018*SL	0.517 + 0.018*SL
SN to QN	t_F	0.155	0.087 + 0.034*SL	0.094 + 0.033*SL	0.069 + 0.033*SL
	t_{PHL}	0.279	0.231 + 0.024*SL	0.253 + 0.019*SL	0.283 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 36, *Group3 : 36 < SL

Switching Characteristics

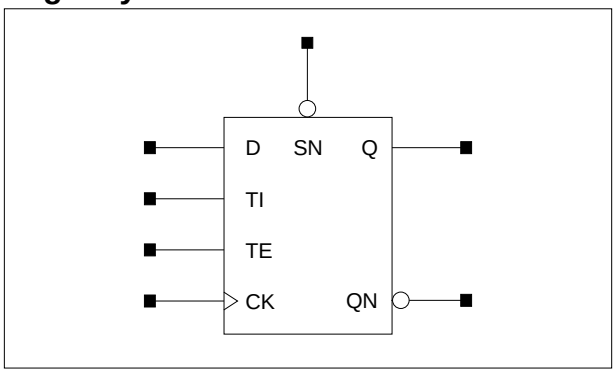
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD3CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.105	0.071 + 0.017*SL	0.064 + 0.019*SL	0.039 + 0.019*SL
	t_F	0.092	0.059 + 0.017*SL	0.059 + 0.016*SL	0.032 + 0.017*SL
	t_{PLH}	0.432	0.410 + 0.011*SL	0.419 + 0.009*SL	0.426 + 0.009*SL
	t_{PHL}	0.465	0.441 + 0.012*SL	0.453 + 0.009*SL	0.466 + 0.009*SL
SCK to Q	t_R	0.114	0.079 + 0.018*SL	0.073 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.098	0.067 + 0.016*SL	0.064 + 0.016*SL	0.034 + 0.017*SL
	t_{PLH}	0.451	0.428 + 0.011*SL	0.439 + 0.009*SL	0.446 + 0.009*SL
	t_{PHL}	0.435	0.411 + 0.012*SL	0.423 + 0.009*SL	0.438 + 0.009*SL
SN to Q	t_R	0.115	0.081 + 0.017*SL	0.073 + 0.019*SL	0.037 + 0.019*SL
	t_{PLH}	0.512	0.489 + 0.011*SL	0.500 + 0.009*SL	0.504 + 0.009*SL
CK to QN	t_R	0.132	0.095 + 0.019*SL	0.094 + 0.019*SL	0.055 + 0.019*SL
	t_F	0.098	0.064 + 0.017*SL	0.067 + 0.016*SL	0.040 + 0.017*SL
	t_{PLH}	0.653	0.627 + 0.013*SL	0.643 + 0.009*SL	0.667 + 0.009*SL
	t_{PHL}	0.574	0.549 + 0.013*SL	0.563 + 0.009*SL	0.587 + 0.009*SL
SCK to QN	t_R	0.109	0.072 + 0.018*SL	0.070 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.088	0.056 + 0.016*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.575	0.552 + 0.012*SL	0.563 + 0.009*SL	0.573 + 0.009*SL
	t_{PHL}	0.564	0.541 + 0.012*SL	0.552 + 0.009*SL	0.562 + 0.009*SL
SN to QN	t_F	0.111	0.076 + 0.018*SL	0.081 + 0.016*SL	0.060 + 0.017*SL
	t_{PHL}	0.249	0.221 + 0.014*SL	0.240 + 0.009*SL	0.281 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



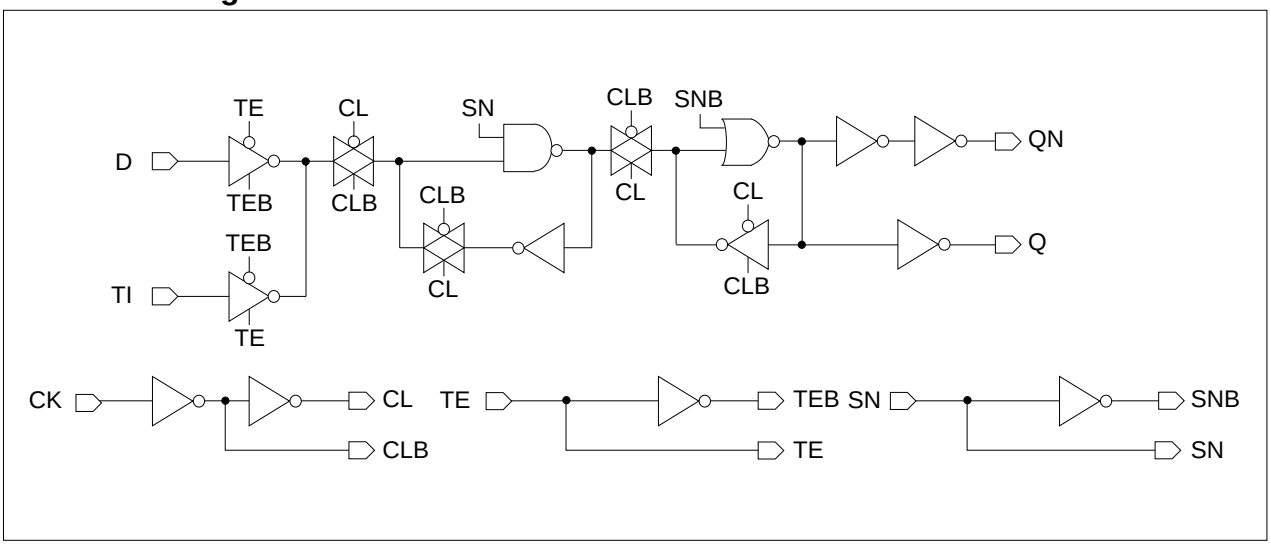
Truth Table

D	TI	TE	CK	SN	Q (n+1)	QN (n+1)
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	1	0
x	x	x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
FD3S					*FD3SD2*					*FD3S*	*FD3SD2*
D	TI	TE	CK	SN	D	TI	TE	CK	SN		
0.7	0.7	1.2	0.7	2.0	0.7	0.7	1.2	0.7	2.0	8.67	8.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3S	FD3SD2
Pulse Width Low (CK)	t_{PWL}	0.434	0.434
Pulse Width High (CK)	t_{PWH}	0.399	0.411
Pulse Width Low (SN)	t_{PWL}	0.405	0.423
Input Setup Time (D to CK)	t_{SU}	1.006	1.007
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (TI to CK)	t_{SU}	1.008	1.009
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	1.075	1.084
Input Hold Time (TE to CK)	t_{HD}	0.025	0.024
Recovery Time (SN)	t_{RC}	0.010	0.012
Removal Time (SN)	t_{RM}	0.390	0.388

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD3S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.148	0.078 + 0.035*SL	0.067 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.157	0.091 + 0.033*SL	0.095 + 0.032*SL	0.061 + 0.033*SL
	t_{PLH}	0.429	0.391 + 0.019*SL	0.398 + 0.017*SL	0.400 + 0.017*SL
	t_{PHL}	0.512	0.465 + 0.024*SL	0.487 + 0.018*SL	0.509 + 0.018*SL
SN to Q	t_R	0.142	0.069 + 0.036*SL	0.062 + 0.038*SL	0.047 + 0.039*SL
	t_{PLH}	0.268	0.230 + 0.019*SL	0.236 + 0.018*SL	0.239 + 0.017*SL
CK to QN	t_R	0.139	0.068 + 0.035*SL	0.056 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.115	0.053 + 0.031*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.585	0.548 + 0.018*SL	0.551 + 0.017*SL	0.551 + 0.017*SL
	t_{PHL}	0.496	0.457 + 0.019*SL	0.464 + 0.018*SL	0.465 + 0.018*SL
SN to QN	t_F	0.116	0.054 + 0.031*SL	0.046 + 0.033*SL	0.033 + 0.034*SL
	t_{PHL}	0.332	0.293 + 0.019*SL	0.299 + 0.018*SL	0.301 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD3SD2

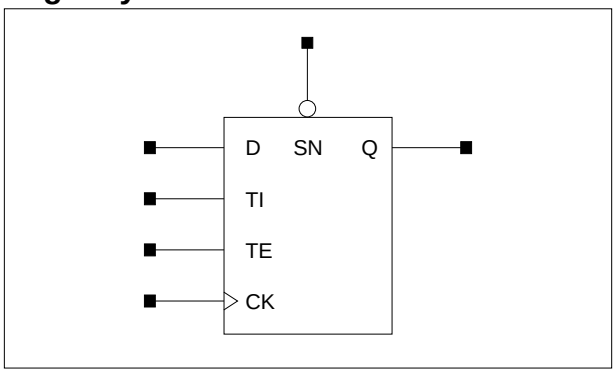
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.112	0.077 + 0.018*SL	0.072 + 0.019*SL	0.039 + 0.019*SL
	t_F	0.135	0.099 + 0.018*SL	0.105 + 0.016*SL	0.069 + 0.017*SL
	t_{PLH}	0.429	0.406 + 0.011*SL	0.416 + 0.009*SL	0.424 + 0.009*SL
	t_{PHL}	0.524	0.494 + 0.015*SL	0.516 + 0.010*SL	0.562 + 0.009*SL
SN to Q	t_R	0.108	0.076 + 0.016*SL	0.065 + 0.019*SL	0.036 + 0.019*SL
	t_{PLH}	0.266	0.244 + 0.011*SL	0.253 + 0.009*SL	0.260 + 0.009*SL
CK to QN	t_R	0.108	0.075 + 0.017*SL	0.066 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.086	0.055 + 0.016*SL	0.051 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.661	0.639 + 0.011*SL	0.647 + 0.009*SL	0.650 + 0.009*SL
	t_{PHL}	0.535	0.512 + 0.011*SL	0.522 + 0.009*SL	0.528 + 0.009*SL
SN to QN	t_F	0.086	0.054 + 0.016*SL	0.051 + 0.017*SL	0.027 + 0.017*SL
	t_{PHL}	0.371	0.348 + 0.011*SL	0.358 + 0.009*SL	0.361 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD3SQ/FD3SQD2

D Flip-Flop with Set, Scan, Q Output Only, 1X/2X Drive

Logic Symbol



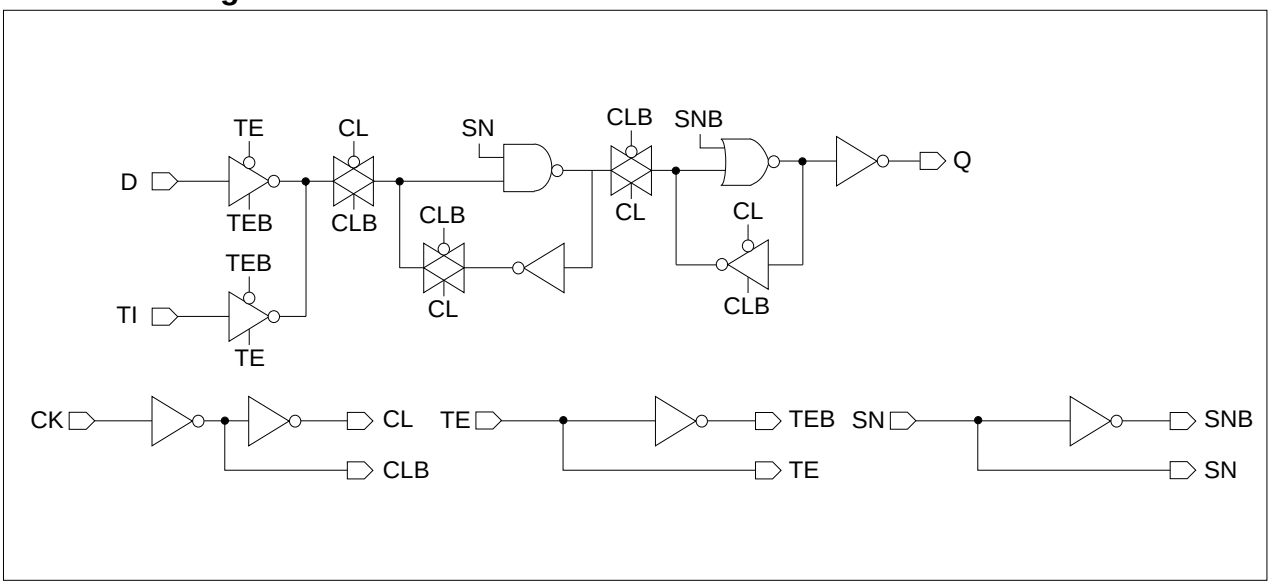
Truth Table

D	TI	TE	CK	SN	Q (n+1)
0	x	0	↑	1	0
1	x	0	↑	1	1
x	0	1	↑	1	0
x	1	1	↑	1	1
x	x	x	x	0	1
x	x	x	↓	1	Q (n)

Cell Data

Input Load (SL)										Gate Count	
FD3SQ					*FD3SQD2*					*FD3SQ*	*FD3SQD2*
D	TI	TE	CK	SN	D	TI	TE	CK	SN		
0.7	0.7	1.2	0.7	2.0	0.7	0.7	1.2	0.7	2.0	7.67	8.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3SQ	FD3SQD2
Pulse Width Low (CK)	t_{PWL}	0.434	0.434
Pulse Width High (CK)	t_{PWH}	0.388	0.400
Pulse Width Low (SN)	t_{PWL}	0.397	0.408
Input Setup Time (D to CK)	t_{SU}	1.004	1.004
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (TI to CK)	t_{SU}	1.006	1.006
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	1.082	1.075
Input Hold Time (TE to CK)	t_{HD}	0.026	0.025
Recovery Time (SN)	t_{RC}	0.010	0.010
Removal Time (SN)	t_{RM}	0.391	0.391

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD3SQ

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.142	0.071 + 0.035*SL	0.059 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.142	0.077 + 0.033*SL	0.077 + 0.033*SL	0.049 + 0.033*SL
	t_{PLH}	0.407	0.369 + 0.019*SL	0.374 + 0.017*SL	0.374 + 0.017*SL
	t_{PHL}	0.473	0.428 + 0.022*SL	0.446 + 0.018*SL	0.460 + 0.018*SL
SN to Q	t_R	0.134	0.062 + 0.036*SL	0.053 + 0.038*SL	0.045 + 0.039*SL
	t_{PLH}	0.249	0.213 + 0.018*SL	0.216 + 0.017*SL	0.218 + 0.017*SL

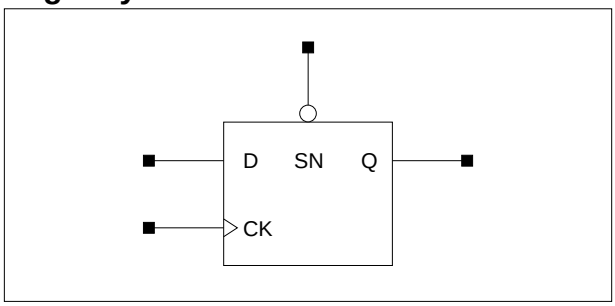
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD3SQD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.105	0.071 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.118	0.084 + 0.017*SL	0.087 + 0.016*SL	0.053 + 0.017*SL
	t_{PLH}	0.408	0.386 + 0.011*SL	0.394 + 0.009*SL	0.398 + 0.009*SL
	t_{PHL}	0.487	0.459 + 0.014*SL	0.477 + 0.009*SL	0.509 + 0.009*SL
SN to Q	t_R	0.095	0.061 + 0.017*SL	0.053 + 0.019*SL	0.033 + 0.019*SL
	t_{PLH}	0.248	0.227 + 0.011*SL	0.234 + 0.009*SL	0.238 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



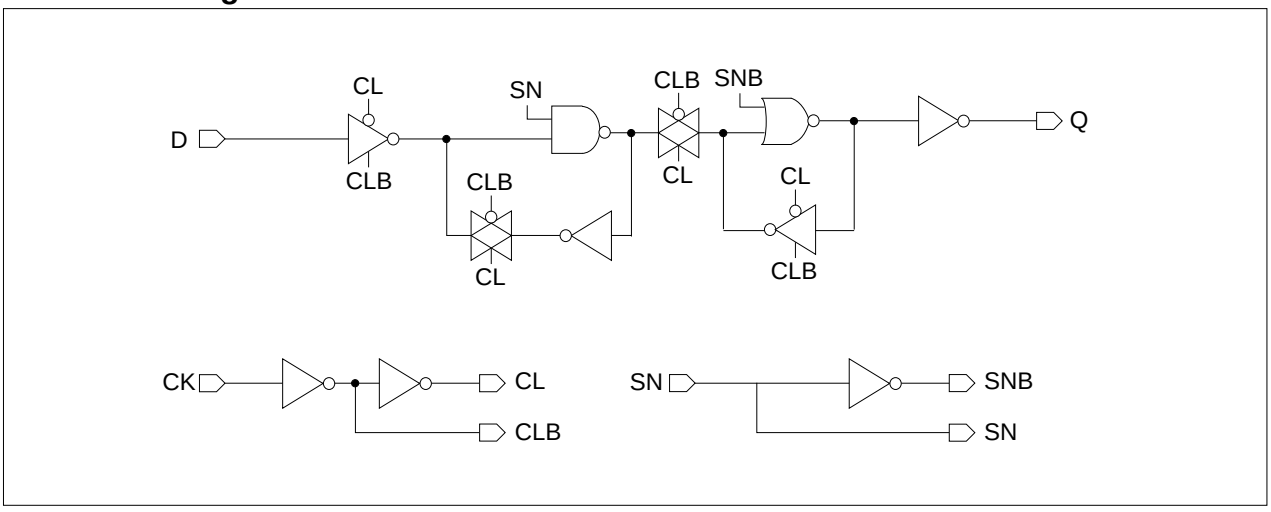
Truth Table

D	CK	SN	Q (n+1)
0	↑	1	0
1	↑	1	1
x	x	0	1
x	↓	x	Q (n)

Cell Data

Input Load (SL)						Gate Count	
FD3Q			*FD3QD2*			*FD3Q*	*FD3QD2*
D	CK	SN	D	CK	SN		
0.7	0.7	2.0	0.7	0.7	2.0	6.00	6.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3Q	FD3QD2
Pulse Width Low (CK)	t_{PWL}	0.455	0.455
Pulse Width High (CK)	t_{PWH}	0.388	0.400
Pulse Width Low (SN)	t_{PWL}	0.397	0.407
Input Setup Time (D to CK)	t_{SU}	0.762	0.762
Input Hold Time (D to CK)	t_{HD}	0.058	0.058
Recovery Time (SN to CK)	t_{RC}	0.010	0.009
Removal Time (SN to CK)	t_{RM}	0.390	0.390

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD3Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.141	0.070 + 0.036*SL	0.059 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.143	0.078 + 0.033*SL	0.077 + 0.033*SL	0.049 + 0.033*SL
	t_{PLH}	0.406	0.368 + 0.019*SL	0.373 + 0.017*SL	0.373 + 0.017*SL
	t_{PHL}	0.473	0.428 + 0.023*SL	0.446 + 0.018*SL	0.459 + 0.018*SL
SN to Q	t_R	0.134	0.061 + 0.036*SL	0.053 + 0.038*SL	0.045 + 0.039*SL
	t_{PLH}	0.250	0.213 + 0.018*SL	0.217 + 0.017*SL	0.218 + 0.017*SL

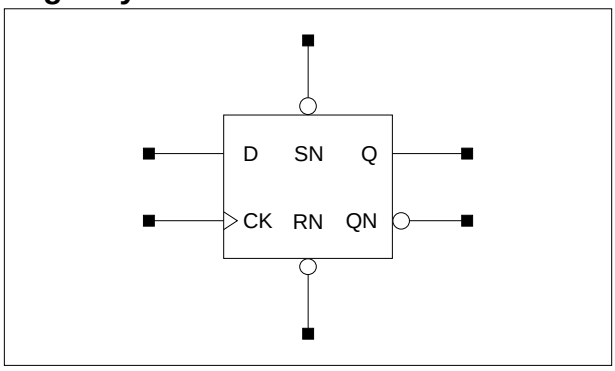
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD3QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.105	0.071 + 0.017*SL	0.063 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.118	0.084 + 0.017*SL	0.087 + 0.016*SL	0.053 + 0.017*SL
	t_{PLH}	0.407	0.385 + 0.011*SL	0.393 + 0.009*SL	0.397 + 0.009*SL
	t_{PHL}	0.486	0.458 + 0.014*SL	0.477 + 0.009*SL	0.509 + 0.009*SL
SN to Q	t_R	0.095	0.059 + 0.018*SL	0.054 + 0.019*SL	0.033 + 0.019*SL
	t_{PLH}	0.248	0.227 + 0.011*SL	0.234 + 0.009*SL	0.239 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



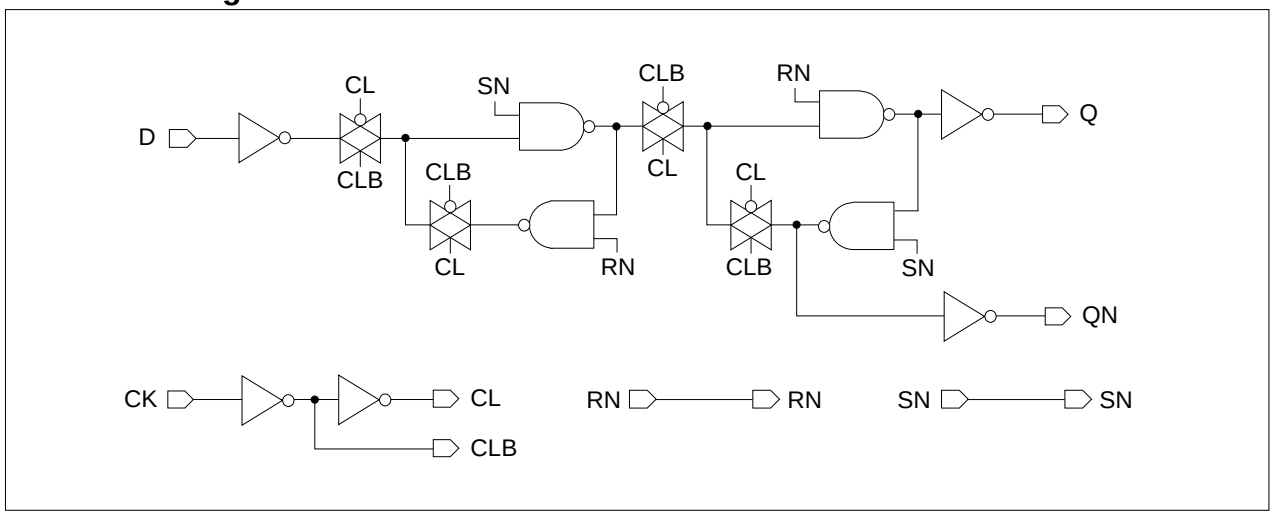
Truth Table

D	CK	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
FD4				*FD4D2*				*FD4*	*FD4D2*
D	CK	RN	SN	D	CK	RN	SN		
0.7	0.7	2.1	2.0	0.7	0.7	2.1	2.0	7.00	7.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4	FD4D2
Pulse Width Low (CK)	t_{PWL}	0.402	0.403
Pulse Width High (CK)	t_{PWH}	0.428	0.452
Pulse Width Low (RN)	t_{PWL}	0.366	0.400
Pulse Width Low (SN)	t_{PWL}	0.375	0.409
Input Setup Time (D to CK)	t_{SU}	0.810	0.812
Input Hold Time (D to CK)	t_{HD}	0.023	0.023
Recovery Time (RN)	t_{RC}	0.000	0.000
Removal Time (RN)	t_{RM}	0.855	0.860
Recovery Time (SN)	t_{RC}	0.264	0.266
Removal Time (SN)	t_{RM}	0.176	0.174

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.157	0.083 + 0.037*SL	0.078 + 0.038*SL	0.056 + 0.039*SL
	t_F	0.125	0.060 + 0.032*SL	0.058 + 0.033*SL	0.039 + 0.034*SL
	t_{PLH}	0.441	0.400 + 0.021*SL	0.411 + 0.018*SL	0.420 + 0.017*SL
	t_{PHL}	0.442	0.401 + 0.021*SL	0.412 + 0.018*SL	0.419 + 0.018*SL
RN to Q	t_R	0.153	0.080 + 0.036*SL	0.073 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.126	0.063 + 0.032*SL	0.058 + 0.033*SL	0.040 + 0.034*SL
	t_{PLH}	0.192	0.151 + 0.020*SL	0.162 + 0.018*SL	0.167 + 0.017*SL
	t_{PHL}	0.222	0.181 + 0.020*SL	0.191 + 0.018*SL	0.198 + 0.018*SL
SN to Q	t_R	0.155	0.083 + 0.036*SL	0.075 + 0.038*SL	0.051 + 0.039*SL
	t_{PLH}	0.412	0.371 + 0.020*SL	0.382 + 0.018*SL	0.387 + 0.017*SL
CK to QN	t_R	0.146	0.074 + 0.036*SL	0.065 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.121	0.058 + 0.031*SL	0.052 + 0.033*SL	0.035 + 0.034*SL
	t_{PLH}	0.544	0.504 + 0.020*SL	0.513 + 0.018*SL	0.516 + 0.017*SL
	t_{PHL}	0.528	0.487 + 0.020*SL	0.497 + 0.018*SL	0.500 + 0.018*SL
RN to QN	t_R	0.172	0.098 + 0.037*SL	0.095 + 0.038*SL	0.061 + 0.038*SL
	t_{PLH}	0.389	0.344 + 0.022*SL	0.362 + 0.018*SL	0.375 + 0.017*SL
SN to QN	t_R	0.171	0.098 + 0.037*SL	0.095 + 0.038*SL	0.061 + 0.038*SL
	t_F	0.138	0.073 + 0.032*SL	0.072 + 0.033*SL	0.046 + 0.033*SL
	t_{PLH}	0.233	0.189 + 0.022*SL	0.207 + 0.018*SL	0.220 + 0.017*SL
	t_{PHL}	0.245	0.201 + 0.022*SL	0.217 + 0.018*SL	0.230 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

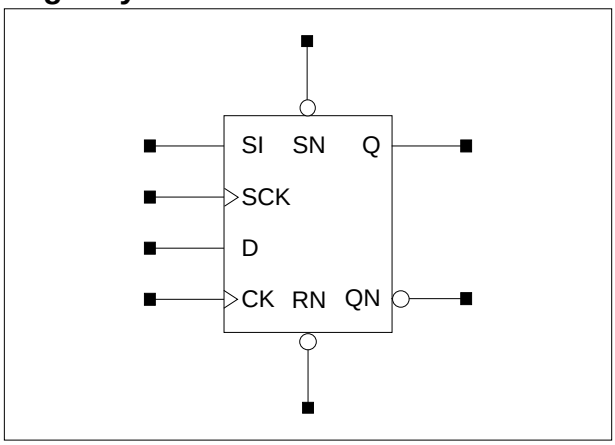
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.117	0.079 + 0.019*SL	0.079 + 0.019*SL	0.051 + 0.019*SL
	t_F	0.092	0.060 + 0.016*SL	0.058 + 0.017*SL	0.033 + 0.017*SL
	t_{PLH}	0.440	0.415 + 0.012*SL	0.428 + 0.009*SL	0.447 + 0.009*SL
	t_{PHL}	0.437	0.412 + 0.012*SL	0.425 + 0.009*SL	0.440 + 0.009*SL
RN to Q	t_R	0.113	0.076 + 0.019*SL	0.075 + 0.019*SL	0.043 + 0.019*SL
	t_F	0.092	0.058 + 0.017*SL	0.059 + 0.016*SL	0.032 + 0.017*SL
	t_{PLH}	0.189	0.165 + 0.012*SL	0.178 + 0.009*SL	0.191 + 0.009*SL
	t_{PHL}	0.213	0.189 + 0.012*SL	0.201 + 0.009*SL	0.216 + 0.009*SL
SN to Q	t_R	0.117	0.081 + 0.018*SL	0.078 + 0.019*SL	0.044 + 0.019*SL
	t_{PLH}	0.439	0.415 + 0.012*SL	0.427 + 0.009*SL	0.441 + 0.009*SL
CK to QN	t_R	0.108	0.070 + 0.019*SL	0.069 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.088	0.054 + 0.017*SL	0.056 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.575	0.551 + 0.012*SL	0.562 + 0.009*SL	0.573 + 0.009*SL
	t_{PHL}	0.559	0.535 + 0.012*SL	0.547 + 0.009*SL	0.558 + 0.009*SL
RN to QN	t_R	0.134	0.096 + 0.019*SL	0.096 + 0.019*SL	0.057 + 0.019*SL
	t_{PLH}	0.413	0.386 + 0.013*SL	0.403 + 0.009*SL	0.429 + 0.009*SL
SN to QN	t_R	0.132	0.094 + 0.019*SL	0.095 + 0.019*SL	0.057 + 0.019*SL
	t_F	0.104	0.070 + 0.017*SL	0.072 + 0.016*SL	0.040 + 0.017*SL
	t_{PLH}	0.229	0.202 + 0.013*SL	0.219 + 0.009*SL	0.246 + 0.009*SL
	t_{PHL}	0.235	0.209 + 0.013*SL	0.225 + 0.009*SL	0.250 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



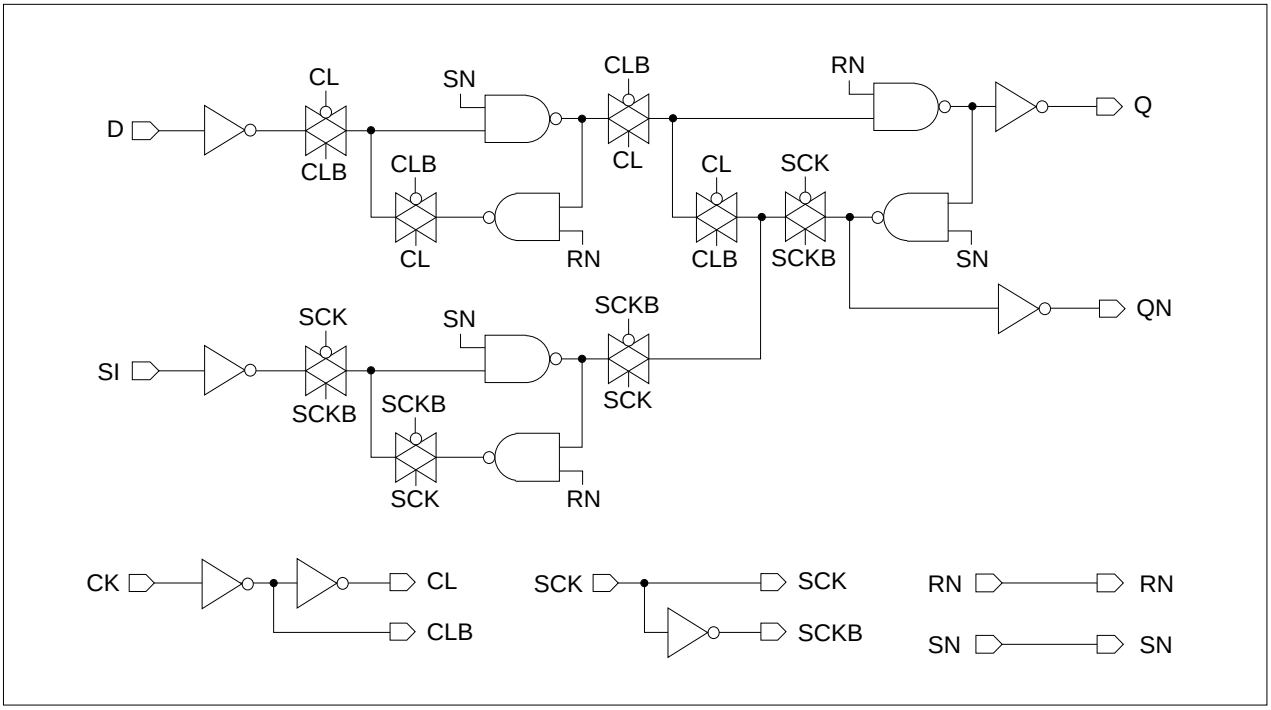
Truth Table

SI	SCK	D	CK	RN	SN	Q (n+1)	QN (n+1)
x	0	0	↑	1	1	0	1
x	0	1	↑	1	1	1	0
0	↑	x	0	1	1	0	1
1	↑	x	0	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	0	x	↓	1	1	Q(n)	QN(n)
x	↓	x	0	1	1	Q(n)	QN(n)

Cell Data

Input Load (SL)												Gate Count	
FD4CS						*FD4CSD2*						*FD4CS*	*FD4CSD2*
SI	SCK	D	CK	RN	SN	SI	SCK	D	CK	RN	SN		
0.8	2.0	0.8	0.8	2.8	2.8	0.8	1.9	0.8	0.8	3.1	3.0	11.33	11.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4CS	FD4CSD2
Pulse Width Low (CK)	t_{PWL}	0.413	0.415
Pulse Width High (CK)	t_{PWH}	0.464	0.488
Pulse Width Low (SCK)	t_{PWL}	0.416	0.416
Pulse Width High (SCK)	t_{PWH}	0.473	0.514
Pulse Width Low (RN)	t_{PWL}	0.449	0.457
Pulse Width Low (SN)	t_{PWL}	0.460	0.478
Input Setup Time (D to CK)	t_{SU}	0.575	0.577
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (SI to SCK)	t_{SU}	1.243	1.243
Input Hold Time (SI to SCK)	t_{HD}	0.000	0.000
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.866	0.853
Recovery Time (RN to SCK)	t_{RC}	0.000	0.000
Input Hold Time (RN to SCK)	t_{HD}	0.818	0.814
Recovery Time (SN to CK)	t_{RC}	0.109	0.114
Removal Time (SN to CK)	t_{RM}	0.289	0.285
Recovery Time (SN to SCK)	t_{RC}	0.292	0.294
Input Hold Time (SN to SCK)	t_{HD}	0.108	0.106

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD4CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.160	0.088 + 0.036*SL	0.082 + 0.038*SL	0.059 + 0.039*SL
	t_F	0.128	0.065 + 0.032*SL	0.060 + 0.033*SL	0.041 + 0.034*SL
	t_{PLH}	0.470	0.428 + 0.021*SL	0.440 + 0.018*SL	0.450 + 0.017*SL
	t_{PHL}	0.475	0.434 + 0.020*SL	0.445 + 0.018*SL	0.451 + 0.018*SL
SCK to Q	t_R	0.168	0.096 + 0.036*SL	0.089 + 0.038*SL	0.062 + 0.039*SL
	t_F	0.134	0.071 + 0.031*SL	0.065 + 0.033*SL	0.042 + 0.034*SL
	t_{PLH}	0.487	0.445 + 0.021*SL	0.458 + 0.018*SL	0.468 + 0.017*SL
	t_{PHL}	0.440	0.398 + 0.021*SL	0.410 + 0.018*SL	0.417 + 0.018*SL
SN to Q	t_R	0.167	0.097 + 0.035*SL	0.087 + 0.038*SL	0.056 + 0.039*SL
	t_{PLH}	0.547	0.505 + 0.021*SL	0.518 + 0.018*SL	0.524 + 0.017*SL
RN to Q	t_R	0.157	0.085 + 0.036*SL	0.078 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.128	0.065 + 0.031*SL	0.058 + 0.033*SL	0.041 + 0.034*SL
	t_{PLH}	0.206	0.165 + 0.021*SL	0.177 + 0.018*SL	0.182 + 0.017*SL
	t_{PHL}	0.223	0.182 + 0.020*SL	0.192 + 0.018*SL	0.199 + 0.018*SL
CK to QN	t_R	0.182	0.109 + 0.037*SL	0.106 + 0.037*SL	0.069 + 0.038*SL
	t_F	0.142	0.076 + 0.033*SL	0.076 + 0.033*SL	0.052 + 0.033*SL
	t_{PLH}	0.671	0.626 + 0.023*SL	0.645 + 0.018*SL	0.661 + 0.017*SL
	t_{PHL}	0.610	0.565 + 0.022*SL	0.582 + 0.018*SL	0.598 + 0.018*SL
SCK to QN	t_R	0.153	0.081 + 0.036*SL	0.072 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.125	0.062 + 0.031*SL	0.056 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.563	0.523 + 0.020*SL	0.533 + 0.018*SL	0.537 + 0.017*SL
	t_{PHL}	0.581	0.540 + 0.020*SL	0.550 + 0.018*SL	0.554 + 0.018*SL
SN to QN	t_R	0.220	0.143 + 0.039*SL	0.150 + 0.037*SL	0.114 + 0.038*SL
	t_F	0.156	0.088 + 0.034*SL	0.094 + 0.033*SL	0.072 + 0.033*SL
	t_{PLH}	0.317	0.263 + 0.027*SL	0.295 + 0.019*SL	0.344 + 0.017*SL
	t_{PHL}	0.279	0.231 + 0.024*SL	0.253 + 0.019*SL	0.286 + 0.018*SL
RN to QN	t_R	0.224	0.147 + 0.038*SL	0.152 + 0.037*SL	0.115 + 0.038*SL
	t_{PLH}	0.477	0.424 + 0.027*SL	0.456 + 0.019*SL	0.504 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

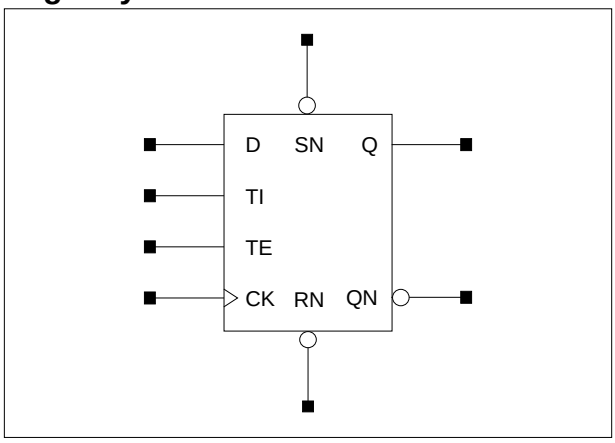
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD4CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.118	0.082 + 0.018*SL	0.079 + 0.019*SL	0.050 + 0.019*SL
	t_F	0.095	0.061 + 0.017*SL	0.062 + 0.016*SL	0.033 + 0.017*SL
	t_{PLH}	0.464	0.439 + 0.012*SL	0.452 + 0.009*SL	0.470 + 0.009*SL
	t_{PHL}	0.477	0.453 + 0.012*SL	0.466 + 0.009*SL	0.480 + 0.009*SL
SCK to Q	t_R	0.125	0.090 + 0.018*SL	0.086 + 0.019*SL	0.053 + 0.019*SL
	t_F	0.100	0.068 + 0.016*SL	0.067 + 0.016*SL	0.035 + 0.017*SL
	t_{PLH}	0.485	0.460 + 0.012*SL	0.473 + 0.009*SL	0.492 + 0.009*SL
	t_{PHL}	0.448	0.423 + 0.012*SL	0.436 + 0.009*SL	0.452 + 0.009*SL
SN to Q	t_R	0.125	0.088 + 0.018*SL	0.085 + 0.019*SL	0.047 + 0.019*SL
	t_{PLH}	0.546	0.522 + 0.012*SL	0.535 + 0.009*SL	0.549 + 0.009*SL
RN to Q	t_R	0.114	0.078 + 0.018*SL	0.075 + 0.019*SL	0.044 + 0.019*SL
	t_F	0.092	0.058 + 0.017*SL	0.059 + 0.017*SL	0.033 + 0.017*SL
	t_{PLH}	0.187	0.163 + 0.012*SL	0.175 + 0.009*SL	0.189 + 0.009*SL
	t_{PHL}	0.211	0.187 + 0.012*SL	0.199 + 0.009*SL	0.214 + 0.009*SL
CK to QN	t_R	0.132	0.095 + 0.019*SL	0.094 + 0.019*SL	0.055 + 0.019*SL
	t_F	0.102	0.068 + 0.017*SL	0.070 + 0.016*SL	0.042 + 0.017*SL
	t_{PLH}	0.668	0.641 + 0.013*SL	0.658 + 0.009*SL	0.682 + 0.009*SL
	t_{PHL}	0.616	0.590 + 0.013*SL	0.605 + 0.009*SL	0.629 + 0.009*SL
SCK to QN	t_R	0.110	0.074 + 0.018*SL	0.071 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.090	0.059 + 0.016*SL	0.056 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.589	0.566 + 0.012*SL	0.577 + 0.009*SL	0.588 + 0.009*SL
	t_{PHL}	0.604	0.580 + 0.012*SL	0.592 + 0.009*SL	0.602 + 0.009*SL
SN to QN	t_R	0.156	0.116 + 0.020*SL	0.120 + 0.019*SL	0.096 + 0.019*SL
	t_F	0.113	0.078 + 0.018*SL	0.083 + 0.016*SL	0.062 + 0.017*SL
	t_{PLH}	0.256	0.226 + 0.015*SL	0.249 + 0.010*SL	0.307 + 0.009*SL
	t_{PHL}	0.251	0.222 + 0.014*SL	0.241 + 0.009*SL	0.283 + 0.009*SL
RN to QN	t_R	0.159	0.120 + 0.020*SL	0.124 + 0.019*SL	0.097 + 0.019*SL
	t_{PLH}	0.439	0.408 + 0.016*SL	0.432 + 0.010*SL	0.491 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



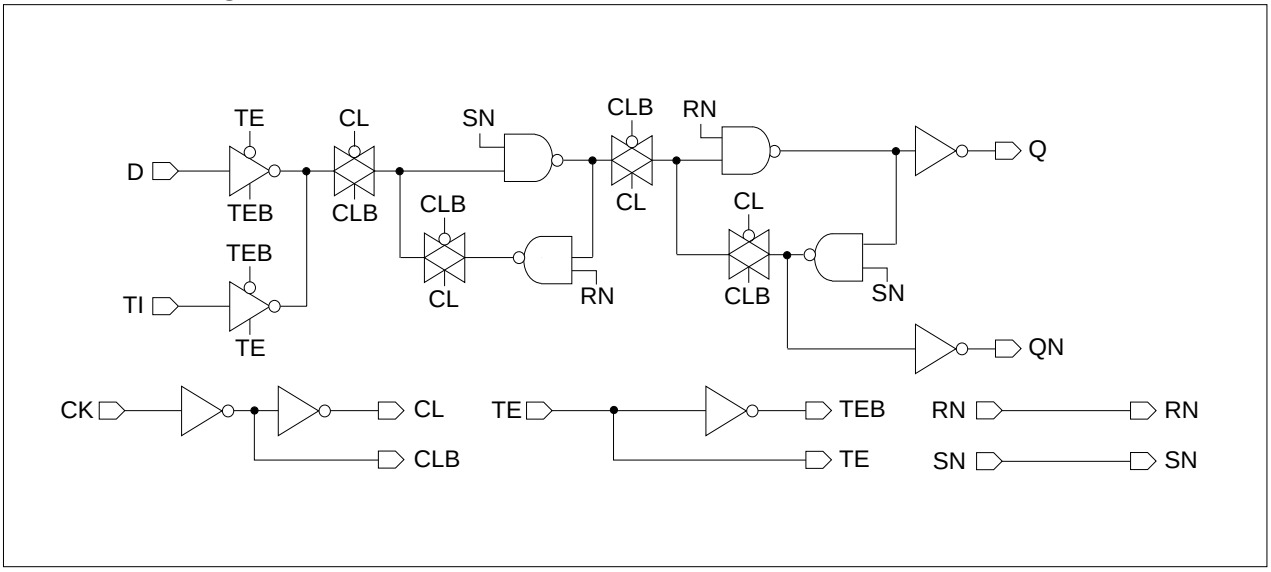
Truth Table

D	TI	TE	CK	RN	SN	Q (n+1)	QN (n+1)
0	x	0	↑	1	1	0	1
1	x	0	↑	1	1	1	0
x	0	1	↑	1	1	0	1
x	1	1	↑	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	x	x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)												Gate Count	
FD4S						*FD4SD2*						*FD4S*	*FD4SD2*
D	TI	TE	CK	RN	SN	D	TI	TE	CK	RN	SN		
0.7	0.7	1.2	0.7	2.1	2.0	0.7	0.7	1.2	0.7	2.1	2.0	9.00	9.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4S	FD4SD2
Pulse Width Low (CK)	t_{PWL}	0.457	0.457
Pulse Width High (CK)	t_{PWH}	0.437	0.462
Pulse Width Low (RN)	t_{PWL}	0.368	0.403
Pulse Width Low (SN)	t_{PWL}	0.384	0.418
Input Setup Time (D to CK)	t_{SU}	0.978	0.978
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (TI to CK)	t_{SU}	0.992	0.992
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	1.062	1.062
Input Hold Time (TE to CK)	t_{HD}	0.071	0.071
Recovery Time (RN)	t_{RC}	0.242	0.243
Removal Time (RN)	t_{RM}	0.158	0.157
Recovery Time (SN)	t_{RC}	0.069	0.069
Removal Time (SN)	t_{RM}	0.331	0.330

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD4S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.158	0.084 + 0.037*SL	0.080 + 0.038*SL	0.057 + 0.039*SL
	t_F	0.127	0.063 + 0.032*SL	0.059 + 0.033*SL	0.040 + 0.034*SL
	t_{PLH}	0.456	0.415 + 0.021*SL	0.427 + 0.018*SL	0.435 + 0.017*SL
	t_{PHL}	0.468	0.428 + 0.020*SL	0.438 + 0.018*SL	0.444 + 0.018*SL
RN to Q	t_R	0.153	0.081 + 0.036*SL	0.073 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.126	0.063 + 0.032*SL	0.058 + 0.033*SL	0.042 + 0.034*SL
	t_{PLH}	0.192	0.152 + 0.020*SL	0.163 + 0.018*SL	0.166 + 0.017*SL
	t_{PHL}	0.220	0.180 + 0.020*SL	0.189 + 0.018*SL	0.197 + 0.018*SL
SN to Q	t_R	0.155	0.083 + 0.036*SL	0.076 + 0.038*SL	0.052 + 0.039*SL
	t_{PLH}	0.421	0.380 + 0.020*SL	0.391 + 0.018*SL	0.396 + 0.017*SL
CK to QN	t_R	0.149	0.077 + 0.036*SL	0.069 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.124	0.061 + 0.031*SL	0.055 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.577	0.537 + 0.020*SL	0.546 + 0.018*SL	0.550 + 0.017*SL
	t_{PHL}	0.549	0.508 + 0.020*SL	0.518 + 0.018*SL	0.522 + 0.018*SL
RN to QN	t_R	0.177	0.103 + 0.037*SL	0.102 + 0.037*SL	0.066 + 0.038*SL
	t_{PLH}	0.398	0.352 + 0.023*SL	0.372 + 0.018*SL	0.387 + 0.017*SL
SN to QN	t_R	0.177	0.102 + 0.037*SL	0.102 + 0.037*SL	0.066 + 0.038*SL
	t_F	0.142	0.077 + 0.033*SL	0.077 + 0.033*SL	0.050 + 0.033*SL
	t_{PLH}	0.245	0.200 + 0.023*SL	0.219 + 0.018*SL	0.234 + 0.017*SL
	t_{PHL}	0.253	0.209 + 0.022*SL	0.226 + 0.018*SL	0.240 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

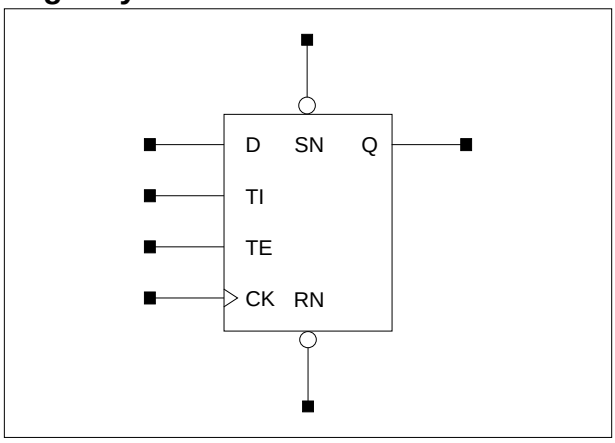
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD4SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.119	0.081 + 0.019*SL	0.081 + 0.019*SL	0.052 + 0.019*SL
	t_F	0.093	0.060 + 0.016*SL	0.059 + 0.016*SL	0.033 + 0.017*SL
	t_{PLH}	0.458	0.433 + 0.012*SL	0.446 + 0.009*SL	0.465 + 0.009*SL
	t_{PHL}	0.464	0.440 + 0.012*SL	0.452 + 0.009*SL	0.466 + 0.009*SL
RN to Q	t_R	0.115	0.079 + 0.018*SL	0.075 + 0.019*SL	0.044 + 0.019*SL
	t_F	0.091	0.058 + 0.017*SL	0.059 + 0.017*SL	0.033 + 0.017*SL
	t_{PLH}	0.191	0.167 + 0.012*SL	0.179 + 0.009*SL	0.192 + 0.009*SL
	t_{PHL}	0.213	0.189 + 0.012*SL	0.201 + 0.009*SL	0.215 + 0.009*SL
SN to Q	t_R	0.119	0.082 + 0.018*SL	0.079 + 0.019*SL	0.046 + 0.019*SL
	t_{PLH}	0.450	0.426 + 0.012*SL	0.438 + 0.009*SL	0.452 + 0.009*SL
CK to QN	t_R	0.112	0.075 + 0.018*SL	0.073 + 0.019*SL	0.042 + 0.019*SL
	t_F	0.091	0.058 + 0.016*SL	0.058 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.607	0.583 + 0.012*SL	0.595 + 0.009*SL	0.606 + 0.009*SL
	t_{PHL}	0.582	0.558 + 0.012*SL	0.570 + 0.009*SL	0.581 + 0.009*SL
RN to QN	t_R	0.138	0.101 + 0.019*SL	0.101 + 0.019*SL	0.062 + 0.019*SL
	t_{PLH}	0.421	0.394 + 0.014*SL	0.412 + 0.009*SL	0.441 + 0.009*SL
SN to QN	t_R	0.138	0.100 + 0.019*SL	0.100 + 0.019*SL	0.062 + 0.019*SL
	t_F	0.107	0.073 + 0.017*SL	0.075 + 0.016*SL	0.043 + 0.017*SL
	t_{PLH}	0.239	0.212 + 0.014*SL	0.229 + 0.009*SL	0.259 + 0.009*SL
	t_{PHL}	0.242	0.215 + 0.013*SL	0.232 + 0.009*SL	0.259 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



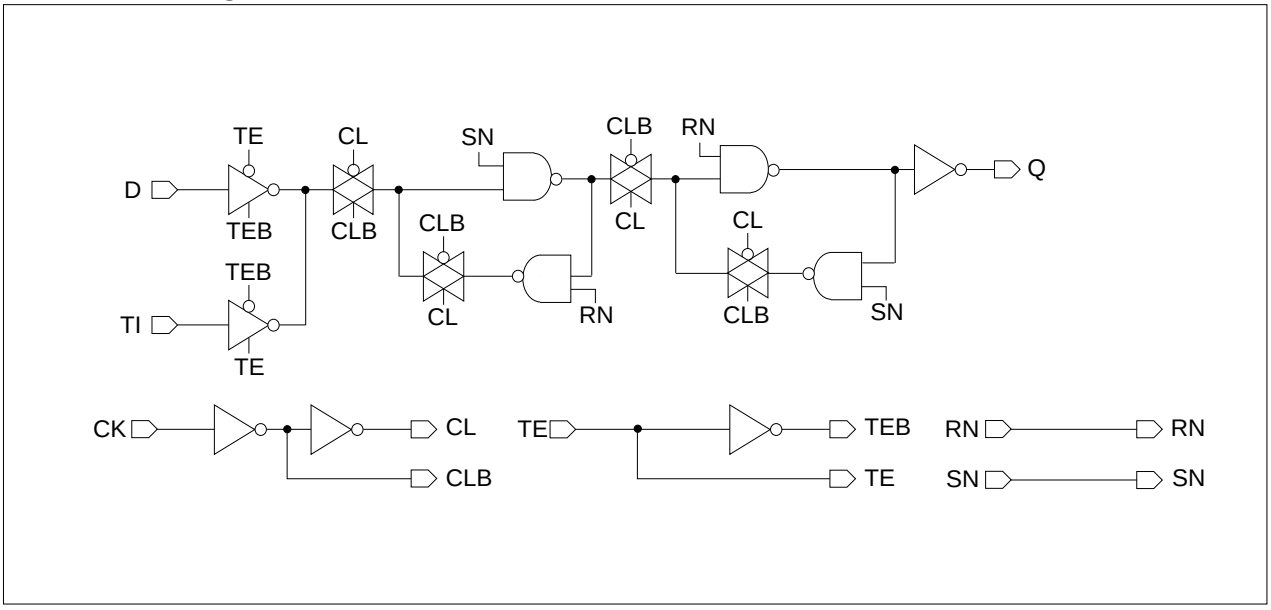
Truth Table

D	TI	TE	CK	RN	SN	Q (n+1)
0	x	0	↑	1	1	0
1	x	0	↑	1	1	1
x	0	1	↑	1	1	0
x	1	1	↑	1	1	1
x	x	x	x	1	0	1
x	x	x	x	0	1	0
x	x	x	x	0	0	0
x	x	x	↓	1	1	Q (n)

Cell Data

Input Load (SL)												Gate Count	
FD4SQ						*FD4SQD2*						*FD4SQ*	*FD4SQD2*
D	TI	TE	CK	RN	SN	D	TI	TE	CK	RN	SN		
0.7	0.7	1.2	0.7	2.1	2.0	0.7	0.7	1.2	0.7	2.1	2.0	8.33	8.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4SQ	FD4SQD2
Pulse Width Low (CK)	t_{PWL}	0.457	0.457
Pulse Width High (CK)	t_{PWH}	0.437	0.462
Pulse Width Low (RN)	t_{PWL}	0.368	0.403
Pulse Width Low (SN)	t_{PWL}	0.384	0.418
Input Setup Time (D to CK)	t_{SU}	0.978	0.978
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (TI to CK)	t_{SU}	0.992	0.992
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	1.062	1.062
Input Hold Time (TE to CK)	t_{HD}	0.071	0.071
Recovery Time (RN)	t_{RC}	0.242	0.243
Removal Time (RN)	t_{RM}	0.158	0.157
Recovery Time (SN)	t_{RC}	0.069	0.069
Removal Time (SN)	t_{RM}	0.331	0.330

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD4SQ

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.158	0.085 + 0.036*SL	0.079 + 0.038*SL	0.054 + 0.039*SL
	t_F	0.127	0.063 + 0.032*SL	0.058 + 0.033*SL	0.038 + 0.034*SL
	t_{PLH}	0.455	0.414 + 0.021*SL	0.427 + 0.018*SL	0.434 + 0.017*SL
	t_{PHL}	0.467	0.426 + 0.021*SL	0.437 + 0.018*SL	0.442 + 0.018*SL
RN to Q	t_R	0.152	0.080 + 0.036*SL	0.073 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.126	0.062 + 0.032*SL	0.057 + 0.033*SL	0.039 + 0.034*SL
	t_{PLH}	0.192	0.151 + 0.020*SL	0.162 + 0.018*SL	0.166 + 0.017*SL
	t_{PHL}	0.220	0.180 + 0.020*SL	0.189 + 0.018*SL	0.196 + 0.018*SL
SN to Q	t_R	0.154	0.082 + 0.036*SL	0.074 + 0.038*SL	0.051 + 0.039*SL
	t_{PLH}	0.389	0.349 + 0.020*SL	0.360 + 0.018*SL	0.364 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD4SQD2

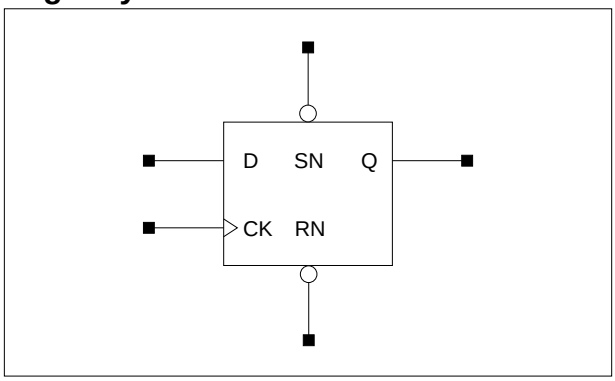
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.120	0.084 + 0.018*SL	0.081 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.093	0.060 + 0.016*SL	0.060 + 0.016*SL	0.031 + 0.017*SL
	t_{PLH}	0.456	0.431 + 0.012*SL	0.444 + 0.009*SL	0.462 + 0.009*SL
	t_{PHL}	0.462	0.437 + 0.012*SL	0.450 + 0.009*SL	0.463 + 0.009*SL
RN to Q	t_R	0.117	0.084 + 0.017*SL	0.074 + 0.019*SL	0.043 + 0.019*SL
	t_F	0.091	0.057 + 0.017*SL	0.060 + 0.016*SL	0.031 + 0.017*SL
	t_{PLH}	0.190	0.166 + 0.012*SL	0.179 + 0.009*SL	0.192 + 0.009*SL
	t_{PHL}	0.213	0.189 + 0.012*SL	0.201 + 0.009*SL	0.214 + 0.009*SL
SN to Q	t_R	0.116	0.079 + 0.018*SL	0.076 + 0.019*SL	0.044 + 0.019*SL
	t_{PLH}	0.391	0.367 + 0.012*SL	0.379 + 0.009*SL	0.393 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD4Q/FD4QD2

D Flip-Flop with Reset, Set, Q Output Only, 1X/2X Drive

Logic Symbol



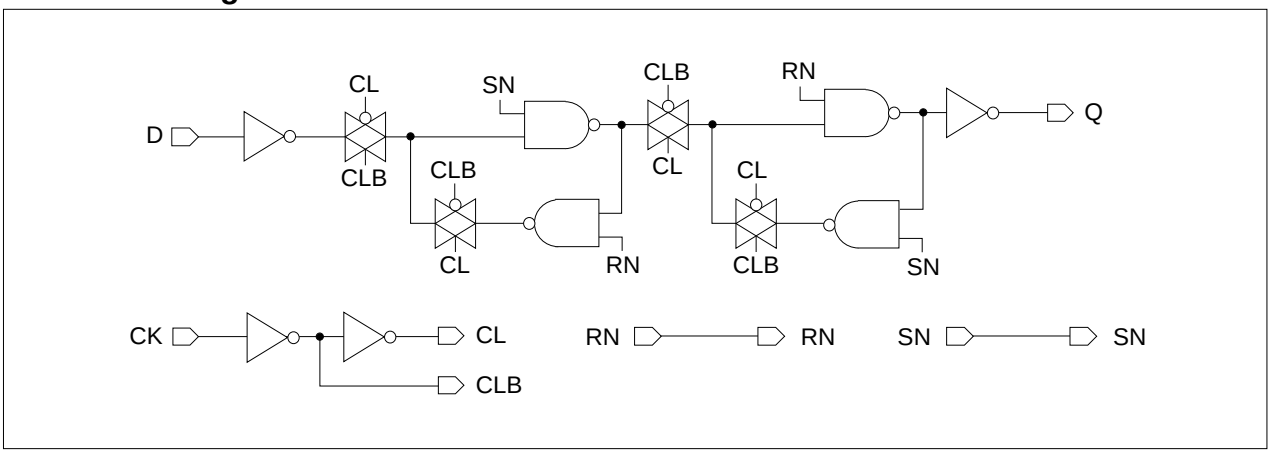
Truth Table

D	CK	RN	SN	Q (n+1)
0	↑	1	1	0
1	↑	1	1	1
x	x	1	0	1
x	x	0	1	0
x	x	0	0	0
x	↓	1	1	Q (n)

Cell Data

Input Load (SL)								Gate Count	
FD4Q				*FD4QD2*				*FD4Q*	*FD4QD2*
D	CK	RN	SN	D	CK	RN	SN		
0.7	0.7	2.1	2.1	0.7	0.7	2.1	2.1	6.33	6.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4Q	FD4QD2
Pulse Width Low (CK)	t_{PWL}	0.402	0.402
Pulse Width High (CK)	t_{PWH}	0.418	0.433
Pulse Width Low (RN)	t_{PWL}	0.347	0.371
Pulse Width Low (SN)	t_{PWL}	0.350	0.362
Input Setup Time (D to CK)	t_{SU}	0.810	0.810
Input Hold Time (D to CK)	t_{HD}	0.022	0.022
Recovery Time (RN)	t_{RC}	0.000	0.000
Removal Time (RN)	t_{RM}	0.856	0.855
Recovery Time (SN)	t_{RC}	0.071	0.071
Removal Time (SN)	t_{RM}	0.328	0.330

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD4Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.156	0.084 + 0.036*SL	0.078 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.126	0.062 + 0.032*SL	0.058 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.440	0.398 + 0.021*SL	0.411 + 0.018*SL	0.418 + 0.017*SL
	t_{PHL}	0.441	0.400 + 0.021*SL	0.411 + 0.018*SL	0.417 + 0.018*SL
RN to Q	t_R	0.152	0.079 + 0.036*SL	0.072 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.125	0.061 + 0.032*SL	0.057 + 0.033*SL	0.038 + 0.034*SL
	t_{PLH}	0.189	0.149 + 0.020*SL	0.160 + 0.018*SL	0.163 + 0.017*SL
	t_{PHL}	0.219	0.179 + 0.020*SL	0.189 + 0.018*SL	0.195 + 0.018*SL
SN to Q	t_R	0.153	0.080 + 0.036*SL	0.073 + 0.038*SL	0.050 + 0.039*SL
	t_{PLH}	0.378	0.338 + 0.020*SL	0.349 + 0.018*SL	0.353 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD4QD2

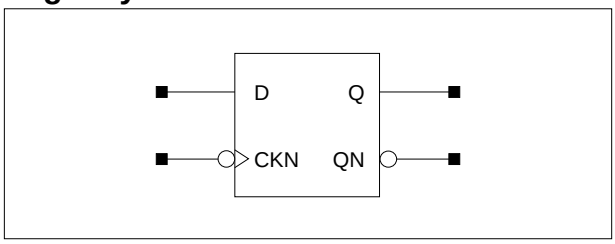
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.118	0.079 + 0.019*SL	0.080 + 0.019*SL	0.047 + 0.019*SL
	t_F	0.092	0.060 + 0.016*SL	0.059 + 0.016*SL	0.030 + 0.017*SL
	t_{PLH}	0.441	0.416 + 0.012*SL	0.429 + 0.009*SL	0.447 + 0.009*SL
	t_{PHL}	0.436	0.412 + 0.012*SL	0.425 + 0.009*SL	0.438 + 0.009*SL
RN to Q	t_R	0.113	0.076 + 0.019*SL	0.075 + 0.019*SL	0.043 + 0.019*SL
	t_F	0.091	0.058 + 0.017*SL	0.059 + 0.016*SL	0.030 + 0.017*SL
	t_{PLH}	0.188	0.164 + 0.012*SL	0.176 + 0.009*SL	0.190 + 0.009*SL
	t_{PHL}	0.212	0.188 + 0.012*SL	0.200 + 0.009*SL	0.214 + 0.009*SL
SN to Q	t_R	0.115	0.078 + 0.019*SL	0.076 + 0.019*SL	0.044 + 0.019*SL
	t_{PLH}	0.379	0.355 + 0.012*SL	0.368 + 0.009*SL	0.382 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD5/FD5D2

D Flip-Flop with Negative Edge Trigger, 1X/2X Drive

Logic Symbol



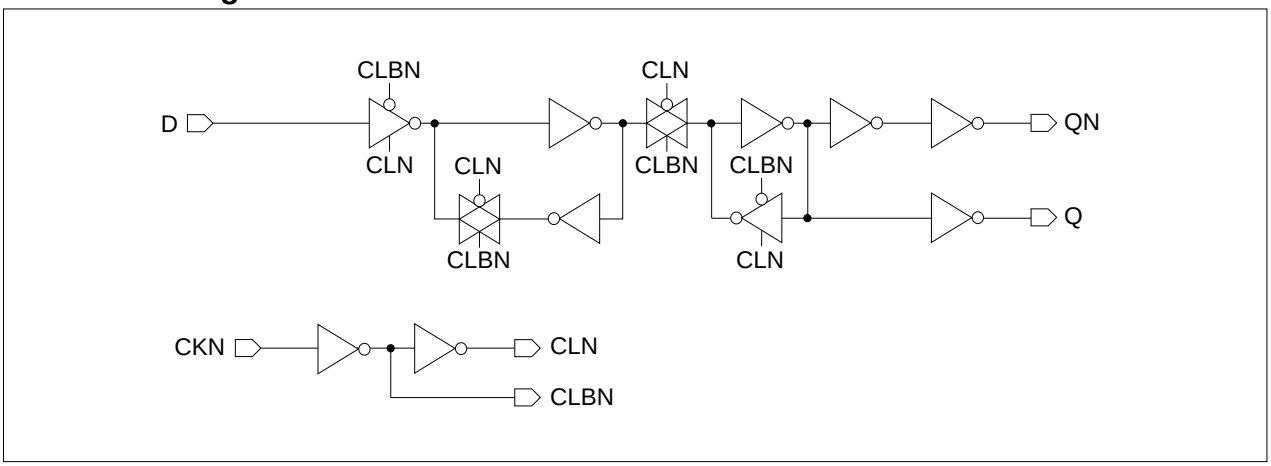
Truth Table

D	CKN	Q (n+1)	QN (n+1)
0	↓	0	1
1	↓	1	0
x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
FD5		*FD5D2*		*FD5*	*FD5D2*
D	CKN	D	CKN		
0.7	0.7	0.7	0.7	5.33	6.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD5	FD5D2
Pulse Width Low (CKN)	t_{PWL}	0.488	0.488
Pulse Width High (CKN)	t_{PWH}	0.488	0.488
Input Setup Time (D to CKN)	t_{SU}	0.208	0.208
Input Hold Time (D to CKN)	t_{HD}	0.200	0.200

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.146	0.075 + 0.036*SL	0.065 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.124	0.061 + 0.032*SL	0.056 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.461	0.422 + 0.019*SL	0.429 + 0.017*SL	0.431 + 0.017*SL
	t_{PHL}	0.409	0.369 + 0.020*SL	0.379 + 0.018*SL	0.383 + 0.018*SL
CKN to QN	t_R	0.133	0.060 + 0.037*SL	0.052 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.114	0.052 + 0.031*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.475	0.439 + 0.018*SL	0.442 + 0.017*SL	0.442 + 0.017*SL
	t_{PHL}	0.527	0.488 + 0.019*SL	0.494 + 0.018*SL	0.496 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD5D2

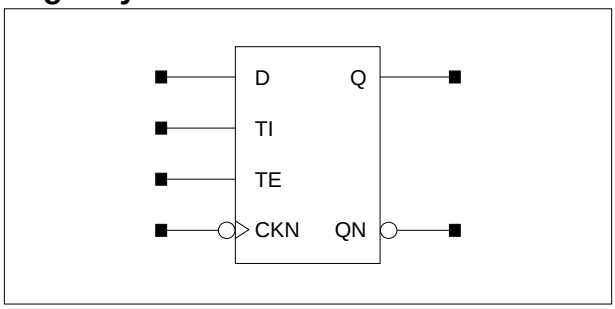
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.106	0.071 + 0.018*SL	0.066 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.088	0.056 + 0.016*SL	0.054 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.457	0.435 + 0.011*SL	0.444 + 0.009*SL	0.451 + 0.009*SL
	t_{PHL}	0.401	0.377 + 0.012*SL	0.389 + 0.009*SL	0.401 + 0.009*SL
CKN to QN	t_R	0.100	0.064 + 0.018*SL	0.058 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.085	0.054 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.514	0.493 + 0.011*SL	0.500 + 0.009*SL	0.503 + 0.009*SL
	t_{PHL}	0.562	0.539 + 0.011*SL	0.549 + 0.009*SL	0.556 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD5S/FD5SD2

D Flip-Flop with Negative Edge Trigger, Scan, 1X/2X Drive

Logic Symbol



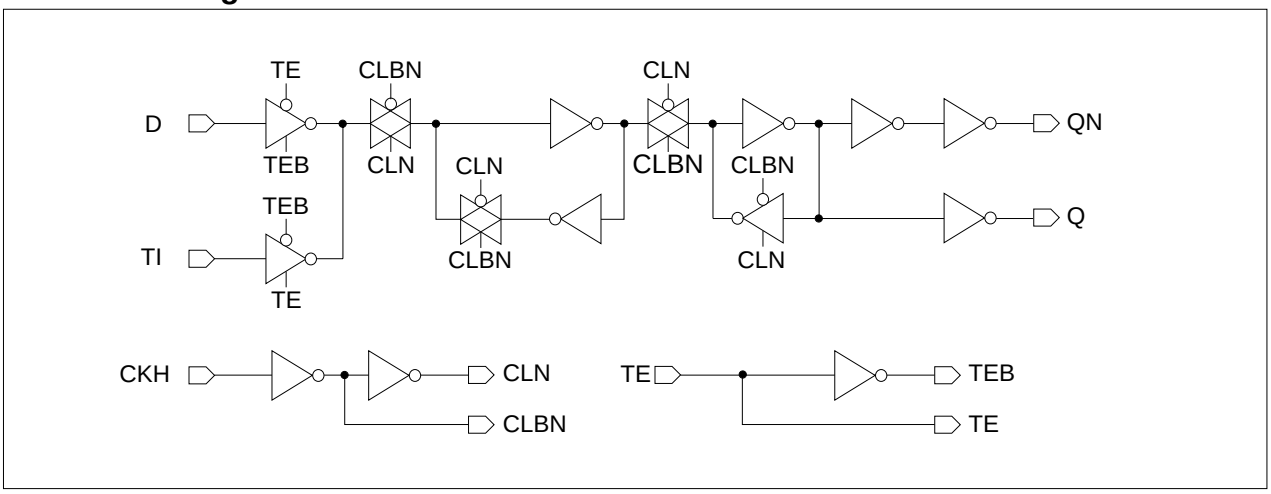
Truth Table

D	TI	TE	CKN	Q (n+1)	QN (n+1)
0	x	0	↓	0	1
1	x	0	↓	1	0
x	0	1	↓	0	1
x	1	1	↓	1	0
x	x	x	↑	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
FD5S				*FD5SD2*				*FD5S*	*FD5SD2*
D	TI	TE	CKN	D	TI	TE	CKN		
0.7	0.7	1.3	0.7	0.7	0.7	1.3	0.7	7.00	7.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD5S	FD5SD2
Pulse Width Low (CKN)	t_{PWL}	0.384	0.391
Pulse Width High (CKN)	t_{PWH}	0.384	0.391
Input Setup Time (D to CKN)	t_{SU}	0.513	0.514
Input Hold Time (D to CKN)	t_{HD}	0.668	0.670
Input Setup Time (TI to CKN)	t_{SU}	0.514	0.514
Input Hold Time (TI to CKN)	t_{HD}	0.668	0.669
Input Setup Time (TE to CKN)	t_{SU}	0.585	0.585
Input Hold Time (TE to CKN)	t_{HD}	0.664	0.666

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD5S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.154	0.083 + 0.035*SL	0.073 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.129	0.065 + 0.032*SL	0.061 + 0.033*SL	0.040 + 0.034*SL
	t_{PLH}	0.478	0.439 + 0.020*SL	0.448 + 0.018*SL	0.451 + 0.017*SL
	t_{PHL}	0.412	0.370 + 0.021*SL	0.382 + 0.018*SL	0.387 + 0.018*SL
CKN to QN	t_R	0.134	0.062 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.116	0.053 + 0.031*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.478	0.442 + 0.018*SL	0.445 + 0.017*SL	0.445 + 0.017*SL
	t_{PHL}	0.545	0.506 + 0.019*SL	0.512 + 0.018*SL	0.514 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD5SD2

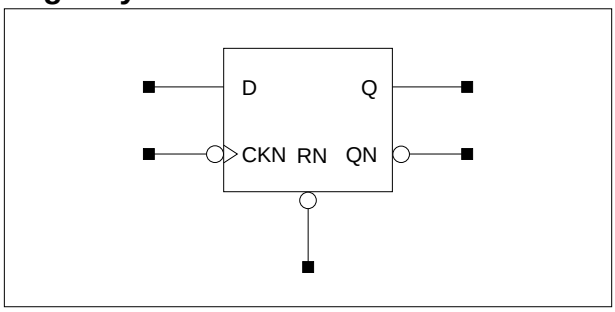
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.106	0.071 + 0.017*SL	0.065 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.088	0.056 + 0.016*SL	0.055 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.457	0.434 + 0.011*SL	0.444 + 0.009*SL	0.451 + 0.009*SL
	t_{PHL}	0.400	0.376 + 0.012*SL	0.388 + 0.009*SL	0.400 + 0.009*SL
CKN to QN	t_R	0.100	0.064 + 0.018*SL	0.058 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.085	0.052 + 0.016*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.513	0.492 + 0.011*SL	0.500 + 0.009*SL	0.502 + 0.009*SL
	t_{PHL}	0.561	0.539 + 0.011*SL	0.549 + 0.009*SL	0.556 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD6/FD6D2

D Flip-Flop with Negative Edge Trigger, Reset, 1X/2X Drive

Logic Symbol



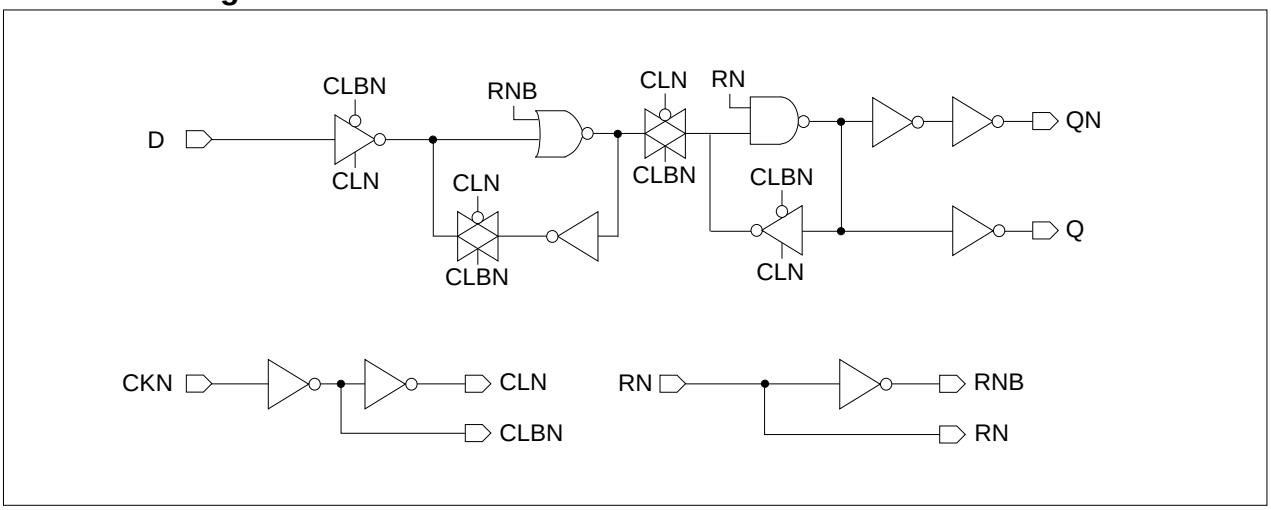
Truth Table

D	CKN	RN	Q (n+1)	QN (n+1)
0	↓	1	0	1
1	↓	1	1	0
x	x	0	0	1
x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FD6			*FD6D2*			*FD6*	*FD6D2*
D	CKN	RN	D	CKN	RN		
0.7	0.7	1.9	0.7	0.7	1.9	6.33	7.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD6	FD6D2
Pulse Width Low (CKN)	t_{PWL}	0.393	0.406
Pulse Width High (CKN)	t_{PWH}	0.393	0.406
Pulse Width Low (RN)	t_{PWL}	0.356	0.355
Input Setup Time (D to CKN)	t_{SU}	0.483	0.483
Input Hold Time (D to CKN)	t_{HD}	0.918	0.918
Recovery Time (RN)	t_{RC}	0.000	0.000
Removal Time (RN)	t_{RM}	0.569	0.569

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.158	0.085 + 0.036*SL	0.080 + 0.038*SL	0.055 + 0.039*SL
	t_F	0.132	0.068 + 0.032*SL	0.064 + 0.033*SL	0.041 + 0.034*SL
	t_{PLH}	0.483	0.442 + 0.021*SL	0.454 + 0.018*SL	0.461 + 0.017*SL
	t_{PHL}	0.421	0.379 + 0.021*SL	0.392 + 0.018*SL	0.399 + 0.018*SL
RN to Q	t_F	0.134	0.072 + 0.031*SL	0.066 + 0.033*SL	0.038 + 0.034*SL
	t_{PHL}	0.251	0.209 + 0.021*SL	0.222 + 0.018*SL	0.226 + 0.018*SL
CKN to QN	t_R	0.135	0.062 + 0.036*SL	0.053 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.115	0.051 + 0.032*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.488	0.452 + 0.018*SL	0.454 + 0.017*SL	0.455 + 0.017*SL
	t_{PHL}	0.549	0.511 + 0.019*SL	0.517 + 0.018*SL	0.519 + 0.018*SL
RN to QN	t_R	0.135	0.063 + 0.036*SL	0.053 + 0.038*SL	0.045 + 0.039*SL
	t_{PLH}	0.318	0.282 + 0.018*SL	0.285 + 0.017*SL	0.285 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD6D2

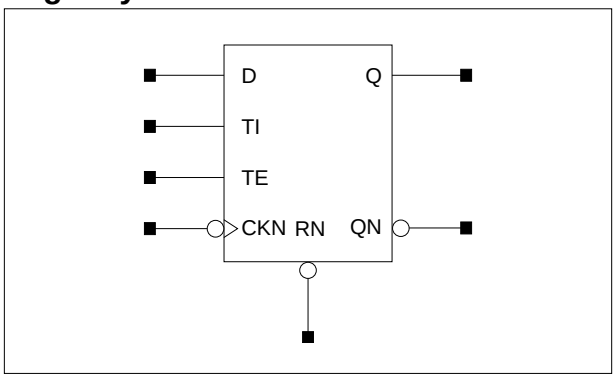
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.121	0.084 + 0.018*SL	0.082 + 0.019*SL	0.050 + 0.019*SL
	t_F	0.100	0.067 + 0.017*SL	0.067 + 0.016*SL	0.036 + 0.017*SL
	t_{PLH}	0.485	0.461 + 0.012*SL	0.474 + 0.009*SL	0.492 + 0.009*SL
	t_{PHL}	0.420	0.394 + 0.013*SL	0.409 + 0.009*SL	0.428 + 0.009*SL
RN to Q	t_F	0.104	0.072 + 0.016*SL	0.071 + 0.016*SL	0.029 + 0.017*SL
	t_{PHL}	0.247	0.222 + 0.013*SL	0.237 + 0.009*SL	0.250 + 0.009*SL
CKN to QN	t_R	0.102	0.068 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.088	0.057 + 0.016*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.539	0.517 + 0.011*SL	0.525 + 0.009*SL	0.528 + 0.009*SL
	t_{PHL}	0.596	0.573 + 0.012*SL	0.584 + 0.009*SL	0.591 + 0.009*SL
RN to QN	t_R	0.102	0.067 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_{PLH}	0.366	0.345 + 0.011*SL	0.352 + 0.009*SL	0.355 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD6S/FD6SD2

D Flip-Flop with Negative Edge Trigger, Reset, Scan, 1X/2X Drive

Logic Symbol



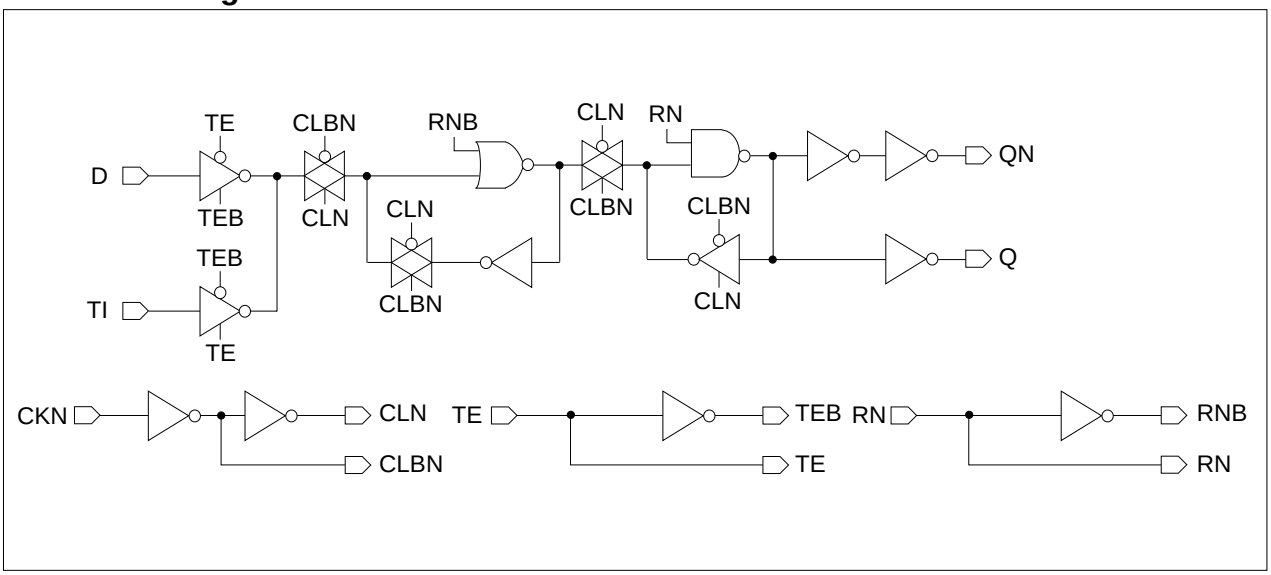
Truth Table

D	TI	TE	CKN	RN	Q (n+1)	QN (n+1)
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	0	1
x	x	x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
FD6S					*FD6SD2*					*FD6S*	*FD6SD2*
D	TI	TE	CKN	RN	D	TI	TE	CKN	RN		
0.7	0.7	1.3	0.7	1.8	0.7	0.7	1.3	0.7	1.8	8.00	8.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD6S	FD6SD2
Pulse Width Low (CKN)	t_{PWL}	0.415	0.407
Pulse Width High (CKN)	t_{PWH}	0.415	0.407
Pulse Width Low (RN)	t_{PWL}	0.355	0.356
Input Setup Time (D to CKN)	t_{SU}	0.519	0.519
Input Hold Time (D to CKN)	t_{HD}	0.608	0.609
Input Setup Time (TI to CKN)	t_{SU}	0.520	0.520
Input Hold Time (TI to CKN)	t_{HD}	0.607	0.608
Input Setup Time (TE to CKN)	t_{SU}	0.596	0.596
Input Hold Time (TE to CKN)	t_{HD}	0.592	0.593
Recovery Time (RN)	t_{RC}	0.000	0.000
Removal Time (RN)	t_{RM}	0.556	0.556

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD6S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.170	0.098 + 0.036*SL	0.092 + 0.038*SL	0.062 + 0.038*SL
	t_F	0.128	0.064 + 0.032*SL	0.060 + 0.033*SL	0.040 + 0.034*SL
	t_{PLH}	0.526	0.483 + 0.021*SL	0.498 + 0.018*SL	0.509 + 0.017*SL
	t_{PHL}	0.407	0.365 + 0.021*SL	0.377 + 0.018*SL	0.383 + 0.018*SL
RN to Q	t_F	0.131	0.068 + 0.031*SL	0.062 + 0.033*SL	0.037 + 0.034*SL
	t_{PHL}	0.234	0.193 + 0.021*SL	0.204 + 0.018*SL	0.208 + 0.018*SL
CKN to QN	t_R	0.135	0.063 + 0.036*SL	0.053 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.473	0.437 + 0.018*SL	0.440 + 0.017*SL	0.440 + 0.017*SL
	t_{PHL}	0.592	0.554 + 0.019*SL	0.560 + 0.018*SL	0.562 + 0.018*SL
RN to QN	t_R	0.134	0.062 + 0.036*SL	0.053 + 0.038*SL	0.045 + 0.039*SL
	t_{PLH}	0.301	0.265 + 0.018*SL	0.268 + 0.017*SL	0.268 + 0.017*SL

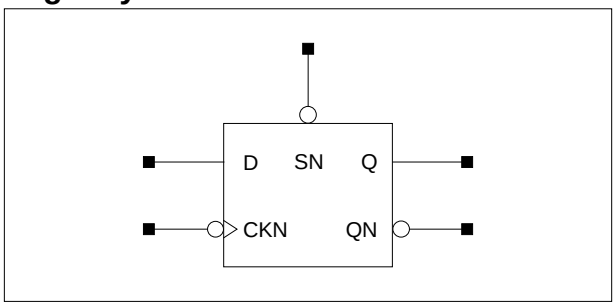
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD6SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.121	0.084 + 0.018*SL	0.081 + 0.019*SL	0.050 + 0.019*SL
	t_F	0.099	0.066 + 0.017*SL	0.067 + 0.016*SL	0.036 + 0.017*SL
	t_{PLH}	0.485	0.461 + 0.012*SL	0.474 + 0.009*SL	0.491 + 0.009*SL
	t_{PHL}	0.419	0.393 + 0.013*SL	0.408 + 0.009*SL	0.426 + 0.009*SL
RN to Q	t_F	0.104	0.072 + 0.016*SL	0.071 + 0.016*SL	0.030 + 0.017*SL
	t_{PHL}	0.247	0.221 + 0.013*SL	0.237 + 0.009*SL	0.249 + 0.009*SL
CKN to QN	t_R	0.102	0.067 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.089	0.057 + 0.016*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.538	0.516 + 0.011*SL	0.524 + 0.009*SL	0.527 + 0.009*SL
	t_{PHL}	0.596	0.573 + 0.012*SL	0.583 + 0.009*SL	0.591 + 0.009*SL
RN to QN	t_R	0.101	0.066 + 0.018*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_{PLH}	0.366	0.345 + 0.011*SL	0.352 + 0.009*SL	0.354 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



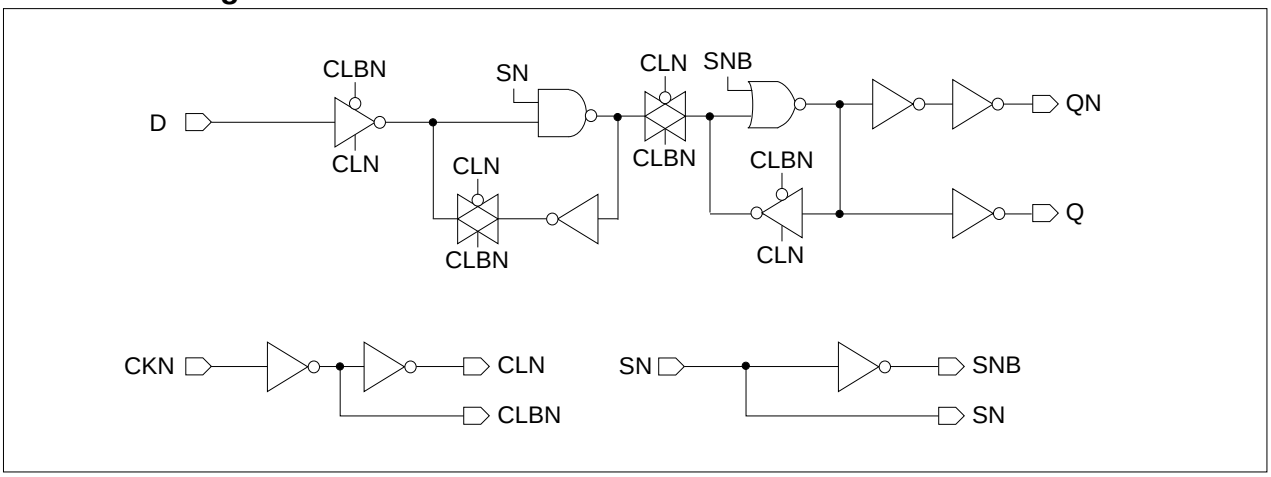
Truth Table

D	CKN	SN	Q (n+1)	QN (n+1)
0	↓	1	0	1
1	↓	1	1	0
x	x	0	1	0
x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FD7			*FD7D2*			*FD7*	*FD7D2*
D	CKN	SN	D	CKN	SN		
0.7	0.7	2.0	0.7	0.7	2.0	7.00	7.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD7	FD7D2
Pulse Width Low (CKN)	t_{PWL}	0.391	0.404
Pulse Width High (CKN)	t_{PWH}	0.391	0.404
Pulse Width Low (SN)	t_{PWL}	0.367	0.366
Input Setup Time (D to CKN)	t_{SU}	0.511	0.511
Input Hold Time (D to CKN)	t_{HD}	0.930	0.930
Recovery Time (SN)	t_{RC}	0.000	0.000
Removal Time (SN)	t_{RM}	0.956	0.956

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.146	0.074 + 0.036*SL	0.064 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.158	0.091 + 0.033*SL	0.096 + 0.032*SL	0.062 + 0.033*SL
	t_{PLH}	0.465	0.427 + 0.019*SL	0.434 + 0.017*SL	0.436 + 0.017*SL
	t_{PHL}	0.503	0.456 + 0.024*SL	0.478 + 0.018*SL	0.501 + 0.018*SL
SN to Q	t_R	0.145	0.074 + 0.036*SL	0.064 + 0.038*SL	0.048 + 0.039*SL
	t_{PLH}	0.291	0.253 + 0.019*SL	0.260 + 0.018*SL	0.263 + 0.017*SL
CKN to QN	t_R	0.138	0.067 + 0.036*SL	0.056 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.113	0.049 + 0.032*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.575	0.539 + 0.018*SL	0.542 + 0.017*SL	0.542 + 0.017*SL
	t_{PHL}	0.532	0.493 + 0.019*SL	0.499 + 0.018*SL	0.501 + 0.018*SL
SN to QN	t_F	0.114	0.052 + 0.031*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PHL}	0.358	0.319 + 0.019*SL	0.325 + 0.018*SL	0.327 + 0.018*SL

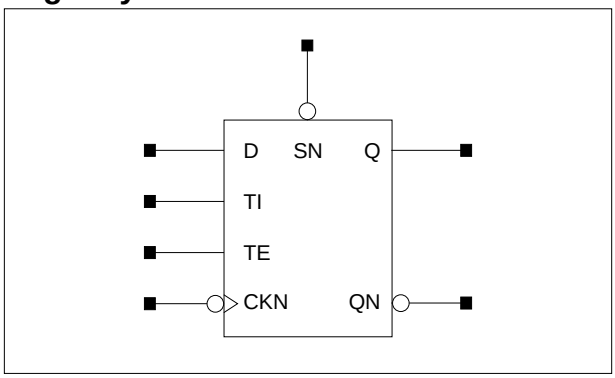
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD7D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.107	0.072 + 0.018*SL	0.066 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.134	0.099 + 0.017*SL	0.104 + 0.016*SL	0.070 + 0.017*SL
	t_{PLH}	0.464	0.442 + 0.011*SL	0.452 + 0.009*SL	0.459 + 0.009*SL
	t_{PHL}	0.513	0.483 + 0.015*SL	0.505 + 0.009*SL	0.550 + 0.009*SL
SN to Q	t_R	0.107	0.071 + 0.018*SL	0.067 + 0.019*SL	0.038 + 0.019*SL
	t_{PLH}	0.287	0.265 + 0.011*SL	0.275 + 0.009*SL	0.283 + 0.009*SL
CKN to QN	t_R	0.108	0.074 + 0.017*SL	0.066 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.085	0.054 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.649	0.627 + 0.011*SL	0.635 + 0.009*SL	0.638 + 0.009*SL
	t_{PHL}	0.569	0.546 + 0.011*SL	0.556 + 0.009*SL	0.563 + 0.009*SL
SN to QN	t_F	0.084	0.052 + 0.016*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PHL}	0.392	0.369 + 0.011*SL	0.379 + 0.009*SL	0.386 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



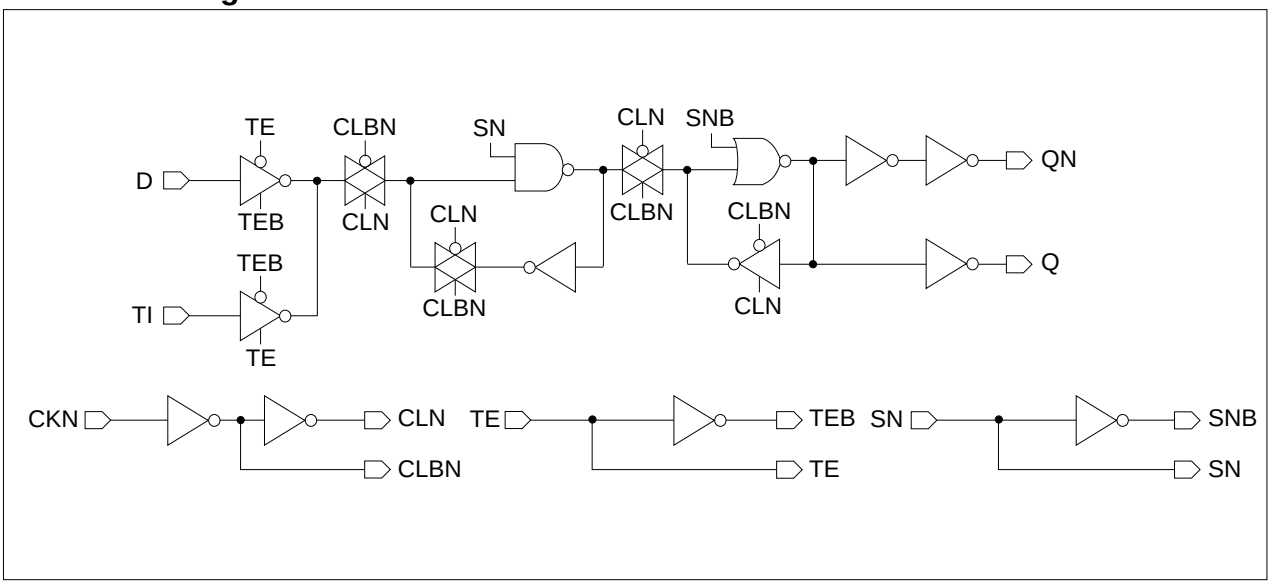
Truth Table

D	TI	TE	CKN	SN	Q (n+1)	QN (n+1)
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	1	0
x	x	x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
FD7S					*FD7SD2*					*FD7S*	*FD7SD2*
D	TI	TE	CKN	SN	D	TI	TE	CKN	SN		
0.7	0.7	1.3	0.7	1.8	0.7	0.7	1.3	0.7	1.8	8.33	9.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD7S	FD7SD2
Pulse Width Low (CKN)	t_{PWL}	0.410	0.426
Pulse Width High (CKN)	t_{PWH}	0.410	0.426
Pulse Width Low (SN)	t_{PWL}	0.340	0.342
Input Setup Time (D to CKN)	t_{SU}	0.630	0.630
Input Hold Time (D to CKN)	t_{HD}	0.673	0.674
Input Setup Time (TI to CKN)	t_{SU}	0.630	0.630
Input Hold Time (TI to CKN)	t_{HD}	0.673	0.673
Input Setup Time (TE to CKN)	t_{SU}	0.309	0.309
Input Hold Time (TE to CKN)	t_{HD}	0.668	0.669
Recovery Time (SN)	t_{RC}	0.000	0.000
Removal Time (SN)	t_{RM}	0.755	0.753

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD7S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.149	0.078 + 0.036*SL	0.068 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.164	0.097 + 0.034*SL	0.102 + 0.032*SL	0.067 + 0.033*SL
	t_{PLH}	0.479	0.440 + 0.020*SL	0.449 + 0.018*SL	0.451 + 0.017*SL
	t_{PHL}	0.534	0.485 + 0.024*SL	0.509 + 0.018*SL	0.534 + 0.018*SL
SN to Q	t_R	0.149	0.078 + 0.036*SL	0.068 + 0.038*SL	0.048 + 0.039*SL
	t_{PLH}	0.302	0.262 + 0.020*SL	0.271 + 0.018*SL	0.274 + 0.017*SL
CKN to QN	t_R	0.139	0.068 + 0.036*SL	0.057 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.115	0.053 + 0.031*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.608	0.571 + 0.018*SL	0.575 + 0.017*SL	0.575 + 0.017*SL
	t_{PHL}	0.547	0.509 + 0.019*SL	0.515 + 0.018*SL	0.516 + 0.018*SL
SN to QN	t_F	0.115	0.053 + 0.031*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PHL}	0.369	0.330 + 0.019*SL	0.336 + 0.018*SL	0.338 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FD7SD2

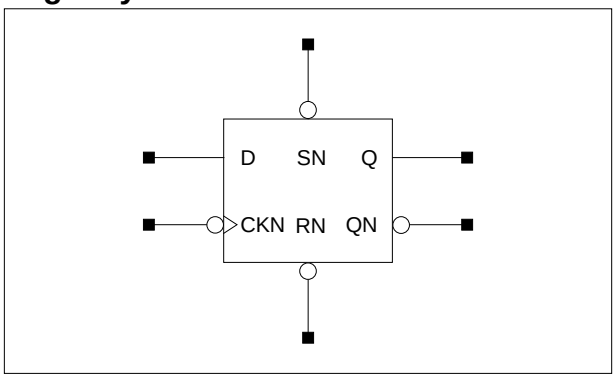
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.108	0.072 + 0.018*SL	0.066 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.135	0.101 + 0.017*SL	0.105 + 0.016*SL	0.071 + 0.017*SL
	t_{PLH}	0.468	0.445 + 0.011*SL	0.455 + 0.009*SL	0.462 + 0.009*SL
	t_{PHL}	0.539	0.509 + 0.015*SL	0.531 + 0.009*SL	0.576 + 0.009*SL
SN to Q	t_R	0.107	0.071 + 0.018*SL	0.066 + 0.019*SL	0.038 + 0.019*SL
	t_{PLH}	0.287	0.264 + 0.011*SL	0.274 + 0.009*SL	0.282 + 0.009*SL
CKN to QN	t_R	0.108	0.074 + 0.017*SL	0.066 + 0.019*SL	0.036 + 0.019*SL
	t_F	0.084	0.050 + 0.017*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.675	0.654 + 0.011*SL	0.662 + 0.009*SL	0.664 + 0.009*SL
	t_{PHL}	0.573	0.550 + 0.011*SL	0.560 + 0.009*SL	0.567 + 0.009*SL
SN to QN	t_F	0.084	0.050 + 0.017*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PHL}	0.392	0.369 + 0.012*SL	0.379 + 0.009*SL	0.386 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD8/FD8D2

D Flip-Flop with Negative Edge Trigger, Reset, Set, 1X/2X Drive

Logic Symbol



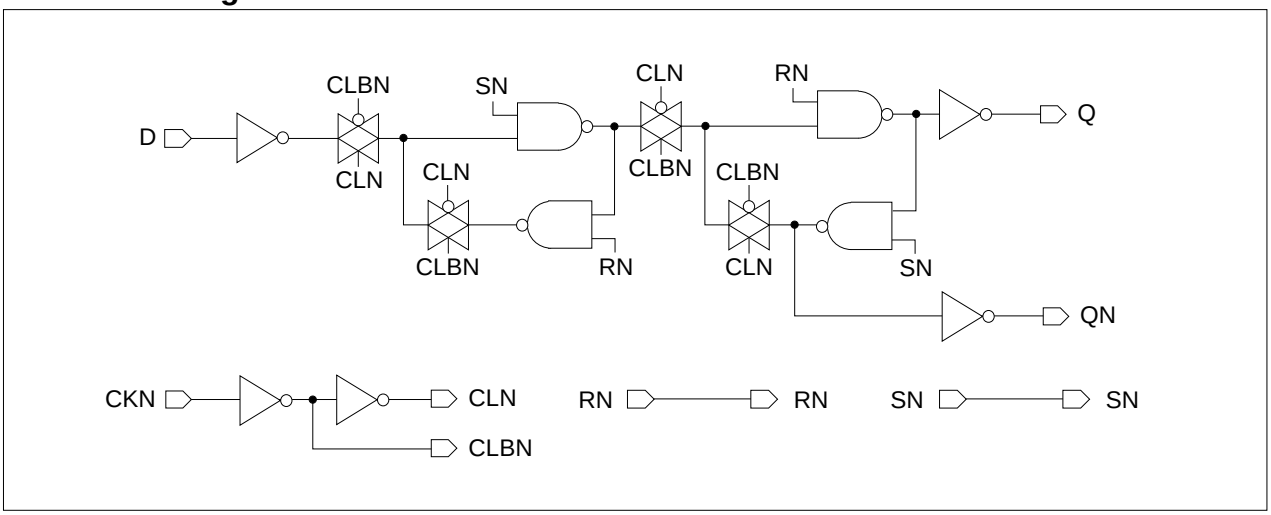
Truth Table

D	CKN	RN	SN	Q (n+1)	QN (n+1)
0	↓	1	1	0	1
1	↓	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↑	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
FD8				*FD8D2*				*FD8*	*FD8D2*
D	CKN	RN	SN	D	CKN	RN	SN		
0.7	0.7	2.1	2.0	0.7	0.7	2.1	2.0	7.00	7.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD8	FD8D2
Pulse Width Low (CKN)	t_{PWL}	0.422	0.448
Pulse Width High (CKN)	t_{PWH}	0.422	0.448
Pulse Width Low (RN)	t_{PWL}	0.399	0.400
Pulse Width Low (SN)	t_{PWL}	0.413	0.414
Input Setup Time (D to CKN)	t_{SU}	0.381	0.382
Input Hold Time (D to CKN)	t_{HD}	0.714	0.713
Recovery Time (RN)	t_{RC}	0.000	0.000
Removal Time (RN)	t_{RM}	1.389	1.388
Recovery Time (SN)	t_{RC}	0.000	0.000
Removal Time (SN)	t_{RM}	0.952	0.952

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.157	0.084 + 0.037*SL	0.079 + 0.038*SL	0.056 + 0.039*SL
	t_F	0.125	0.060 + 0.033*SL	0.058 + 0.033*SL	0.039 + 0.034*SL
	t_{PLH}	0.497	0.456 + 0.021*SL	0.468 + 0.018*SL	0.477 + 0.017*SL
	t_{PHL}	0.441	0.400 + 0.021*SL	0.411 + 0.018*SL	0.418 + 0.018*SL
RN to Q	t_R	0.153	0.080 + 0.036*SL	0.073 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.126	0.063 + 0.032*SL	0.058 + 0.033*SL	0.040 + 0.034*SL
	t_{PLH}	0.192	0.151 + 0.020*SL	0.162 + 0.018*SL	0.167 + 0.017*SL
	t_{PHL}	0.222	0.181 + 0.020*SL	0.191 + 0.018*SL	0.198 + 0.018*SL
SN to Q	t_R	0.155	0.083 + 0.036*SL	0.075 + 0.038*SL	0.051 + 0.039*SL
	t_{PLH}	0.412	0.371 + 0.020*SL	0.382 + 0.018*SL	0.387 + 0.017*SL
CKN to QN	t_R	0.146	0.074 + 0.036*SL	0.065 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.121	0.058 + 0.031*SL	0.052 + 0.033*SL	0.035 + 0.034*SL
	t_{PLH}	0.543	0.503 + 0.020*SL	0.512 + 0.018*SL	0.515 + 0.017*SL
	t_{PHL}	0.584	0.544 + 0.020*SL	0.553 + 0.018*SL	0.556 + 0.018*SL
RN to QN	t_R	0.172	0.098 + 0.037*SL	0.095 + 0.038*SL	0.061 + 0.038*SL
	t_{PLH}	0.389	0.344 + 0.022*SL	0.362 + 0.018*SL	0.375 + 0.017*SL
SN to QN	t_R	0.171	0.098 + 0.037*SL	0.095 + 0.038*SL	0.061 + 0.038*SL
	t_F	0.138	0.073 + 0.032*SL	0.072 + 0.033*SL	0.046 + 0.033*SL
	t_{PLH}	0.233	0.189 + 0.022*SL	0.207 + 0.018*SL	0.220 + 0.017*SL
	t_{PHL}	0.245	0.201 + 0.022*SL	0.217 + 0.018*SL	0.230 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD8D2

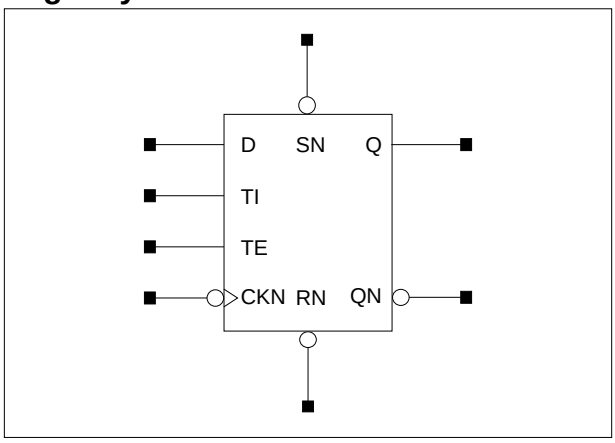
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.119	0.081 + 0.019*SL	0.080 + 0.019*SL	0.051 + 0.019*SL
	t_F	0.091	0.057 + 0.017*SL	0.058 + 0.016*SL	0.033 + 0.017*SL
	t_{PLH}	0.498	0.473 + 0.012*SL	0.486 + 0.009*SL	0.506 + 0.009*SL
	t_{PHL}	0.436	0.411 + 0.012*SL	0.424 + 0.009*SL	0.439 + 0.009*SL
RN to Q	t_R	0.113	0.076 + 0.019*SL	0.075 + 0.019*SL	0.043 + 0.019*SL
	t_F	0.092	0.058 + 0.017*SL	0.059 + 0.016*SL	0.032 + 0.017*SL
	t_{PLH}	0.189	0.165 + 0.012*SL	0.178 + 0.009*SL	0.191 + 0.009*SL
	t_{PHL}	0.213	0.189 + 0.012*SL	0.201 + 0.009*SL	0.216 + 0.009*SL
SN to Q	t_R	0.117	0.081 + 0.018*SL	0.078 + 0.019*SL	0.044 + 0.019*SL
	t_{PLH}	0.439	0.415 + 0.012*SL	0.427 + 0.009*SL	0.441 + 0.009*SL
CKN to QN	t_R	0.109	0.072 + 0.018*SL	0.069 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.089	0.057 + 0.016*SL	0.056 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.574	0.550 + 0.012*SL	0.561 + 0.009*SL	0.572 + 0.009*SL
	t_{PHL}	0.618	0.594 + 0.012*SL	0.605 + 0.009*SL	0.616 + 0.009*SL
RN to QN	t_R	0.134	0.096 + 0.019*SL	0.096 + 0.019*SL	0.057 + 0.019*SL
	t_{PLH}	0.413	0.386 + 0.013*SL	0.403 + 0.009*SL	0.430 + 0.009*SL
SN to QN	t_R	0.132	0.094 + 0.019*SL	0.095 + 0.019*SL	0.057 + 0.019*SL
	t_F	0.104	0.070 + 0.017*SL	0.072 + 0.016*SL	0.040 + 0.017*SL
	t_{PLH}	0.229	0.202 + 0.013*SL	0.219 + 0.009*SL	0.246 + 0.009*SL
	t_{PHL}	0.235	0.209 + 0.013*SL	0.225 + 0.009*SL	0.250 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FD8S/FD8SD2

D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 1X/2X Drive

Logic Symbol



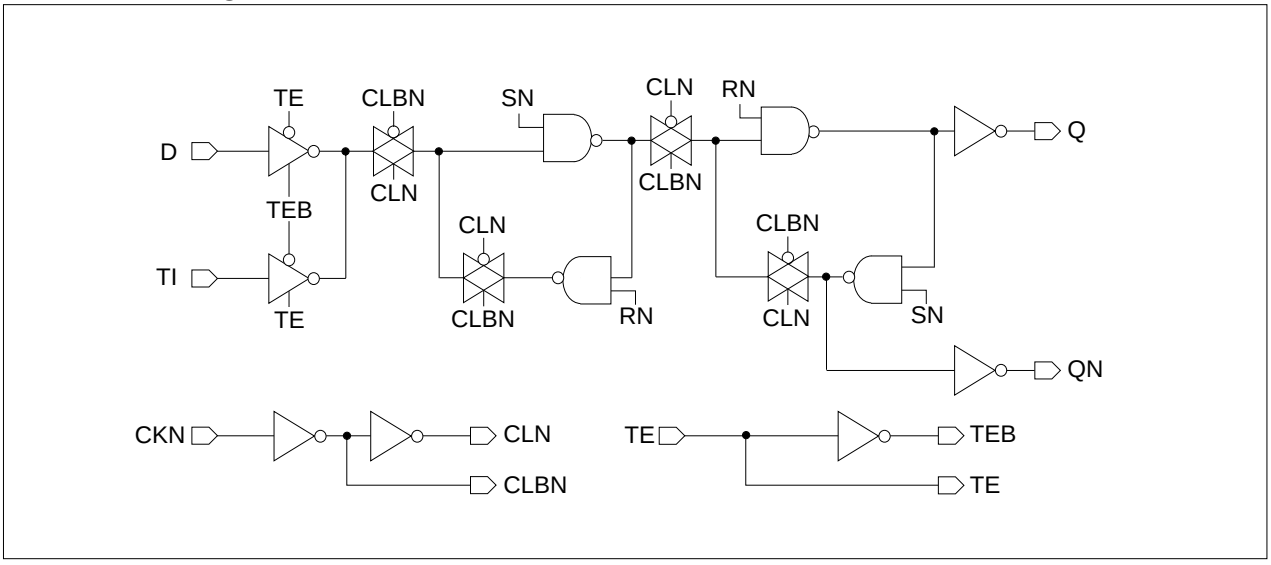
Truth Table

D	TI	TE	CKN	RN	SN	Q (n+1)	QN (n+1)
0	x	0	↓	1	1	0	1
1	x	0	↓	1	1	1	0
x	0	1	↓	1	1	0	1
x	1	1	↓	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	x	x	↑	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)												Gate Count	
FD8S						*FD8SD2*						*FD8S*	*FD8SD2*
D	TI	TE	CKN	RN	SN	D	TI	TE	CKN	RN	SN		
0.7	0.7	1.3	0.7	1.8	1.8	0.7	0.7	1.3	0.7	2.1	2.0	8.67	8.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD8S	FD8SD2
Pulse Width Low (CKN)	t_{PWL}	0.422	0.446
Pulse Width High (CKN)	t_{PWH}	0.422	0.446
Pulse Width Low (RN)	t_{PWL}	0.397	0.400
Pulse Width Low (SN)	t_{PWL}	0.407	0.413
Input Setup Time (D to CKN)	t_{SU}	0.556	0.554
Input Hold Time (D to CKN)	t_{HD}	0.637	0.638
Input Setup Time (TI to CKN)	t_{SU}	0.557	0.554
Input Hold Time (TI to CKN)	t_{HD}	0.636	0.638
Input Setup Time (TE to CKN)	t_{SU}	0.629	0.626
Input Hold Time (TE to CKN)	t_{HD}	0.626	0.628
Recovery Time (RN)	t_{RC}	0.000	0.000
Removal Time(RN)	t_{RM}	1.386	1.370
Recovery Time (SN)	t_{RC}	0.000	0.000
Removal Time (SN)	t_{RM}	0.953	0.950

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD8S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.162	0.089 + 0.036*SL	0.084 + 0.038*SL	0.060 + 0.039*SL
	t_F	0.126	0.062 + 0.032*SL	0.059 + 0.033*SL	0.040 + 0.034*SL
	t_{PLH}	0.506	0.464 + 0.021*SL	0.478 + 0.018*SL	0.488 + 0.017*SL
	t_{PHL}	0.436	0.395 + 0.021*SL	0.406 + 0.018*SL	0.413 + 0.018*SL
RN to Q	t_R	0.158	0.087 + 0.036*SL	0.079 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.128	0.065 + 0.032*SL	0.060 + 0.033*SL	0.041 + 0.034*SL
	t_{PLH}	0.211	0.170 + 0.021*SL	0.182 + 0.018*SL	0.188 + 0.017*SL
	t_{PHL}	0.227	0.186 + 0.020*SL	0.196 + 0.018*SL	0.203 + 0.018*SL
SN to Q	t_R	0.161	0.088 + 0.036*SL	0.082 + 0.038*SL	0.054 + 0.039*SL
	t_{PLH}	0.441	0.400 + 0.021*SL	0.412 + 0.018*SL	0.418 + 0.017*SL
CKN to QN	t_R	0.152	0.080 + 0.036*SL	0.072 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.125	0.063 + 0.031*SL	0.056 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.558	0.517 + 0.020*SL	0.528 + 0.018*SL	0.531 + 0.017*SL
	t_{PHL}	0.602	0.561 + 0.020*SL	0.571 + 0.018*SL	0.575 + 0.018*SL
RN to QN	t_R	0.182	0.110 + 0.036*SL	0.105 + 0.037*SL	0.068 + 0.038*SL
	t_{PLH}	0.429	0.383 + 0.023*SL	0.403 + 0.018*SL	0.419 + 0.017*SL
SN to QN	t_R	0.182	0.109 + 0.037*SL	0.106 + 0.037*SL	0.068 + 0.038*SL
	t_F	0.143	0.078 + 0.032*SL	0.077 + 0.033*SL	0.048 + 0.033*SL
	t_{PLH}	0.268	0.222 + 0.023*SL	0.242 + 0.018*SL	0.258 + 0.017*SL
	t_{PHL}	0.257	0.212 + 0.022*SL	0.229 + 0.018*SL	0.243 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FD8SD2

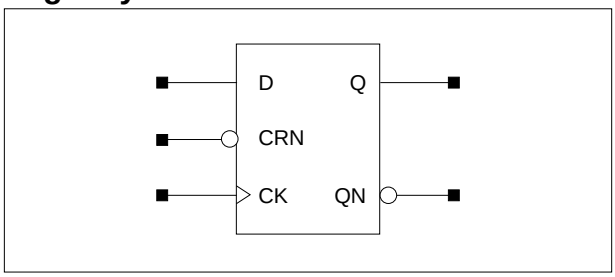
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.119	0.082 + 0.019*SL	0.081 + 0.019*SL	0.053 + 0.019*SL
	t_F	0.092	0.059 + 0.017*SL	0.060 + 0.017*SL	0.034 + 0.017*SL
	t_{PLH}	0.496	0.472 + 0.012*SL	0.485 + 0.009*SL	0.503 + 0.009*SL
	t_{PHL}	0.435	0.411 + 0.012*SL	0.423 + 0.009*SL	0.438 + 0.009*SL
RN to Q	t_R	0.116	0.080 + 0.018*SL	0.077 + 0.019*SL	0.045 + 0.019*SL
	t_F	0.093	0.060 + 0.017*SL	0.060 + 0.016*SL	0.034 + 0.017*SL
	t_{PLH}	0.189	0.165 + 0.012*SL	0.177 + 0.009*SL	0.190 + 0.009*SL
	t_{PHL}	0.213	0.189 + 0.012*SL	0.201 + 0.009*SL	0.215 + 0.009*SL
SN to Q	t_R	0.119	0.083 + 0.018*SL	0.079 + 0.019*SL	0.046 + 0.019*SL
	t_{PLH}	0.439	0.415 + 0.012*SL	0.427 + 0.009*SL	0.440 + 0.009*SL
CKN to QN	t_R	0.110	0.073 + 0.018*SL	0.070 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.090	0.058 + 0.016*SL	0.055 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.573	0.550 + 0.012*SL	0.561 + 0.009*SL	0.572 + 0.009*SL
	t_{PHL}	0.615	0.591 + 0.012*SL	0.603 + 0.009*SL	0.613 + 0.009*SL
RN to QN	t_R	0.134	0.097 + 0.019*SL	0.097 + 0.019*SL	0.058 + 0.019*SL
	t_{PLH}	0.412	0.385 + 0.013*SL	0.403 + 0.009*SL	0.429 + 0.009*SL
SN to QN	t_R	0.133	0.094 + 0.019*SL	0.096 + 0.019*SL	0.058 + 0.019*SL
	t_F	0.104	0.070 + 0.017*SL	0.073 + 0.016*SL	0.040 + 0.017*SL
	t_{PLH}	0.232	0.205 + 0.013*SL	0.222 + 0.009*SL	0.249 + 0.009*SL
	t_{PHL}	0.236	0.210 + 0.013*SL	0.226 + 0.009*SL	0.250 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FDS2/FDS2D2

D Flip-Flop with Synchronous Clear, 1X/2X Drive

Logic Symbol



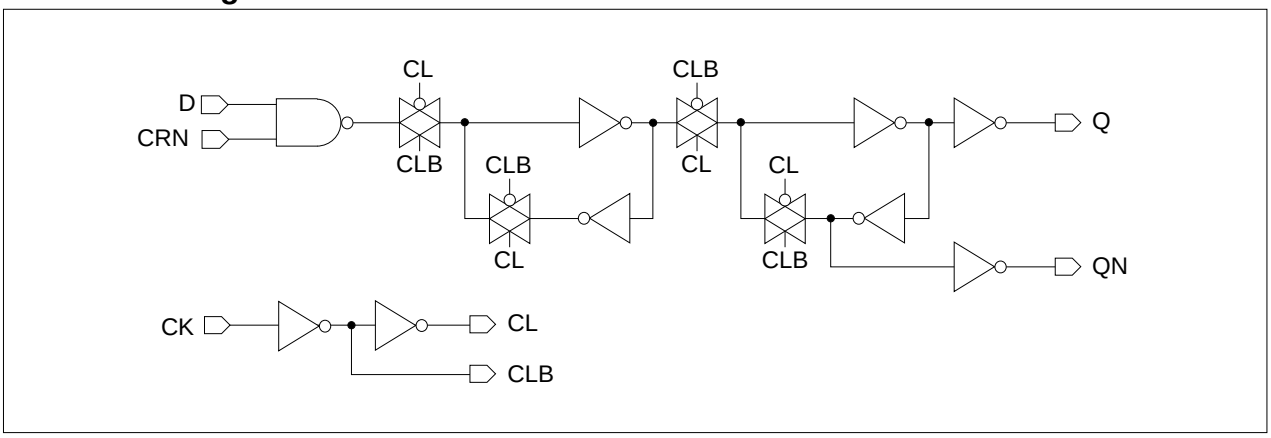
Truth Table

D	CRN	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	0	1
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FDS2			*FDS2D2*			*FDS2*	*FDS2D2*
D	CRN	CK	D	CRN	CK		
1.0	1.0	0.7	1.0	1.0	0.7	6.33	6.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS2	FDS2D2
Pulse Width Low (CK)	t_{PWL}	0.371	0.371
Pulse Width High (CK)	t_{PWH}	0.394	0.406
Input Setup Time (D to CK)	t_{SU}	0.423	0.423
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (CRN to CK)	t_{SU}	0.900	0.900
Input Hold Time (CRN to CK)	t_{HD}	0.112	0.111

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FDS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.146	0.074 + 0.036*SL	0.065 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.124	0.061 + 0.032*SL	0.056 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.404	0.366 + 0.019*SL	0.373 + 0.017*SL	0.375 + 0.017*SL
	t_{PHL}	0.403	0.363 + 0.020*SL	0.373 + 0.018*SL	0.377 + 0.018*SL
CK to QN	t_R	0.133	0.060 + 0.037*SL	0.052 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.114	0.051 + 0.032*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.469	0.433 + 0.018*SL	0.436 + 0.017*SL	0.436 + 0.017*SL
	t_{PHL}	0.470	0.432 + 0.019*SL	0.438 + 0.018*SL	0.440 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FDS2D2

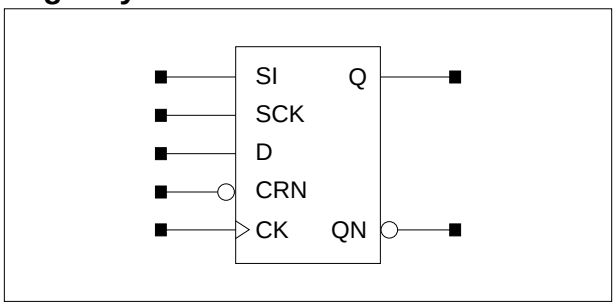
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.106	0.071 + 0.018*SL	0.065 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.088	0.056 + 0.016*SL	0.054 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.401	0.379 + 0.011*SL	0.388 + 0.009*SL	0.395 + 0.009*SL
	t_{PHL}	0.395	0.371 + 0.012*SL	0.383 + 0.009*SL	0.395 + 0.009*SL
CK to QN	t_R	0.099	0.064 + 0.018*SL	0.058 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.085	0.054 + 0.015*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.508	0.487 + 0.011*SL	0.494 + 0.009*SL	0.497 + 0.009*SL
	t_{PHL}	0.506	0.483 + 0.011*SL	0.493 + 0.009*SL	0.500 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FDS2CS/FDS2CSD2

D Flip-Flop with Synchronous Clear, Scan Clock, 1X/2X Drive

Logic Symbol



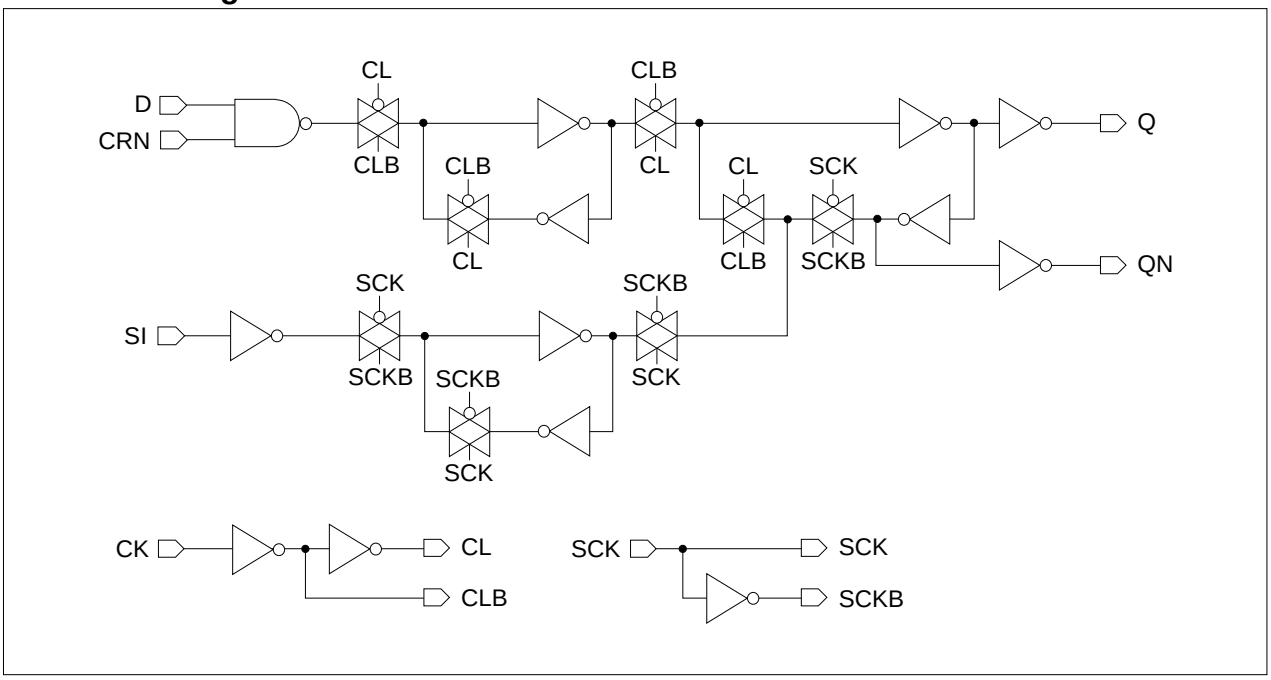
Truth Table

SI	SCK	D	CRN	CK	Q (n+1)	QN (n+1)
x	0	0	1	↑	0	1
x	0	1	1	↑	1	0
0	↑	x	x	0	0	1
1	↑	x	x	0	1	0
x	0	x	0	↑	0	1
x	0	x	x	↓	Q(n)	QN(n)
x	↓	x	x	0	Q(n)	QN(n)

Cell Data

Input Load (SL)										Gate Count	
FDS2CS					*FDS2CSD2*					*FDS2CS*	*FDS2CSD2*
SI	SCK	D	CRN	CK	SI	SCK	D	CRN	CK		
0.8	2.0	1.1	1.1	0.8	0.8	1.9	1.1	1.1	0.8	8.67	9.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C,3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS2CS	FDS2CSD2
Pulse Width Low (CK)	t_{PWL}	0.383	0.384
Pulse Width High (CK)	t_{PWH}	0.430	0.452
Pulse Width Low (SCK)	t_{PWL}	0.374	0.376
Pulse Width High (SCK)	t_{PWH}	0.427	0.457
Input Setup Time (D to CK)	t_{SU}	0.531	0.532
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (SI to SCK)	t_{SU}	1.209	1.215
Input Hold Time (SI to SCK)	t_{HD}	0.000	0.000
Input Setup Time (CRN to CK)	t_{SU}	0.309	0.309
Input Hold Time (CRN to CK)	t_{HD}	0.107	0.108

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FDS2CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.144	0.071 + 0.036*SL	0.064 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.123	0.059 + 0.032*SL	0.054 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.422	0.384 + 0.019*SL	0.390 + 0.018*SL	0.393 + 0.017*SL
	t_{PHL}	0.437	0.396 + 0.020*SL	0.406 + 0.018*SL	0.410 + 0.018*SL
SCK to Q	t_R	0.153	0.082 + 0.035*SL	0.071 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.127	0.063 + 0.032*SL	0.058 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.435	0.396 + 0.019*SL	0.404 + 0.017*SL	0.406 + 0.017*SL
	t_{PHL}	0.373	0.333 + 0.020*SL	0.343 + 0.018*SL	0.348 + 0.018*SL
CK to QN	t_R	0.157	0.087 + 0.035*SL	0.076 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.132	0.067 + 0.033*SL	0.066 + 0.033*SL	0.045 + 0.033*SL
	t_{PLH}	0.568	0.527 + 0.020*SL	0.539 + 0.018*SL	0.542 + 0.017*SL
	t_{PHL}	0.537	0.494 + 0.021*SL	0.508 + 0.018*SL	0.520 + 0.018*SL
SCK to QN	t_R	0.137	0.065 + 0.036*SL	0.055 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.117	0.055 + 0.031*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.453	0.416 + 0.018*SL	0.420 + 0.017*SL	0.420 + 0.017*SL
	t_{PHL}	0.512	0.473 + 0.020*SL	0.480 + 0.018*SL	0.482 + 0.018*SL

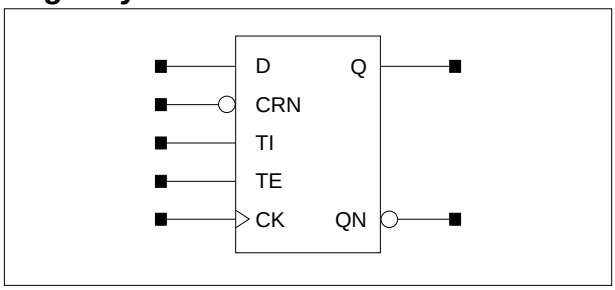
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FDS2CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.103	0.068 + 0.017*SL	0.061 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.087	0.054 + 0.017*SL	0.054 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.418	0.397 + 0.011*SL	0.405 + 0.009*SL	0.412 + 0.009*SL
	t_{PHL}	0.435	0.411 + 0.012*SL	0.423 + 0.009*SL	0.434 + 0.009*SL
SCK to Q	t_R	0.111	0.077 + 0.017*SL	0.069 + 0.019*SL	0.039 + 0.019*SL
	t_F	0.093	0.060 + 0.016*SL	0.060 + 0.016*SL	0.030 + 0.017*SL
	t_{PLH}	0.432	0.409 + 0.011*SL	0.419 + 0.009*SL	0.426 + 0.009*SL
	t_{PHL}	0.377	0.353 + 0.012*SL	0.365 + 0.009*SL	0.377 + 0.009*SL
CK to QN	t_R	0.110	0.074 + 0.018*SL	0.069 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.092	0.058 + 0.017*SL	0.060 + 0.016*SL	0.035 + 0.017*SL
	t_{PLH}	0.568	0.545 + 0.011*SL	0.556 + 0.009*SL	0.563 + 0.009*SL
	t_{PHL}	0.543	0.519 + 0.012*SL	0.532 + 0.009*SL	0.549 + 0.009*SL
SCK to QN	t_R	0.095	0.060 + 0.017*SL	0.053 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.083	0.052 + 0.016*SL	0.048 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.475	0.454 + 0.010*SL	0.460 + 0.009*SL	0.462 + 0.009*SL
	t_{PHL}	0.530	0.508 + 0.011*SL	0.517 + 0.009*SL	0.524 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



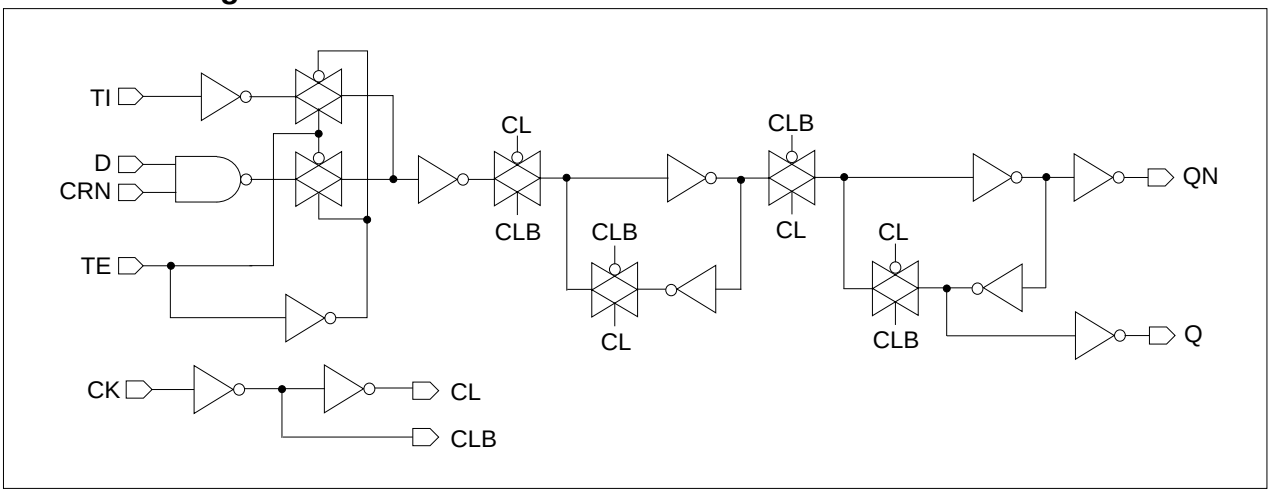
Truth Table

D	CRN	TI	TE	CK	Q (n+1)	QN (n+1)
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	0	x	0	↑	0	1
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0
x	x	x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
FDS2S					*FDS2SD2*					*FDS2S*	*FDS2SD2*
D	CRN	TI	TE	CK	D	CRN	TI	TE	CK		
1.0	1.0	0.7	1.2	0.7	1.0	1.0	0.7	1.2	0.7	8.00	8.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS2S	FDS2SD2
Pulse Width Low (CK)	t_{PWL}	0.423	0.423
Pulse Width High (CK)	t_{PWH}	0.394	0.407
Input Setup Time (D to CK)	t_{SU}	0.989	0.989
Input Hold Time (D to CK)	t_{HD}	0.031	0.031
Input Setup Time (TI to CK)	t_{SU}	0.979	0.979
Input Hold Time (TI to CK)	t_{HD}	0.066	0.066
Input Setup Time (TE to CK)	t_{SU}	0.830	0.830
Input Hold Time (TE to CK)	t_{HD}	0.158	0.158
Input Setup Time (CRN to CK)	t_{SU}	1.093	1.093
Input Hold Time (CRN to CK)	t_{HD}	0.153	0.153

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FDS2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.134	0.061 + 0.036*SL	0.052 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.113	0.049 + 0.032*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.467	0.431 + 0.018*SL	0.434 + 0.017*SL	0.434 + 0.017*SL
	t_{PHL}	0.469	0.430 + 0.019*SL	0.436 + 0.018*SL	0.438 + 0.018*SL
CK to QN	t_R	0.144	0.073 + 0.036*SL	0.063 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.123	0.059 + 0.032*SL	0.055 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.401	0.363 + 0.019*SL	0.370 + 0.017*SL	0.372 + 0.017*SL
	t_{PHL}	0.400	0.360 + 0.020*SL	0.370 + 0.018*SL	0.374 + 0.018*SL

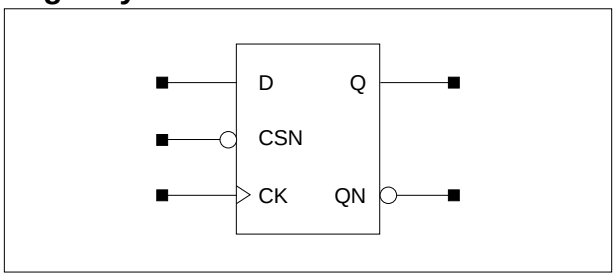
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FDS2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.100	0.065 + 0.017*SL	0.058 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.085	0.054 + 0.016*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.506	0.485 + 0.011*SL	0.493 + 0.009*SL	0.495 + 0.009*SL
	t_{PHL}	0.504	0.481 + 0.011*SL	0.491 + 0.009*SL	0.498 + 0.009*SL
CK to QN	t_R	0.106	0.070 + 0.018*SL	0.065 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.088	0.054 + 0.017*SL	0.056 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.400	0.377 + 0.011*SL	0.387 + 0.009*SL	0.394 + 0.009*SL
	t_{PHL}	0.393	0.369 + 0.012*SL	0.381 + 0.009*SL	0.394 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



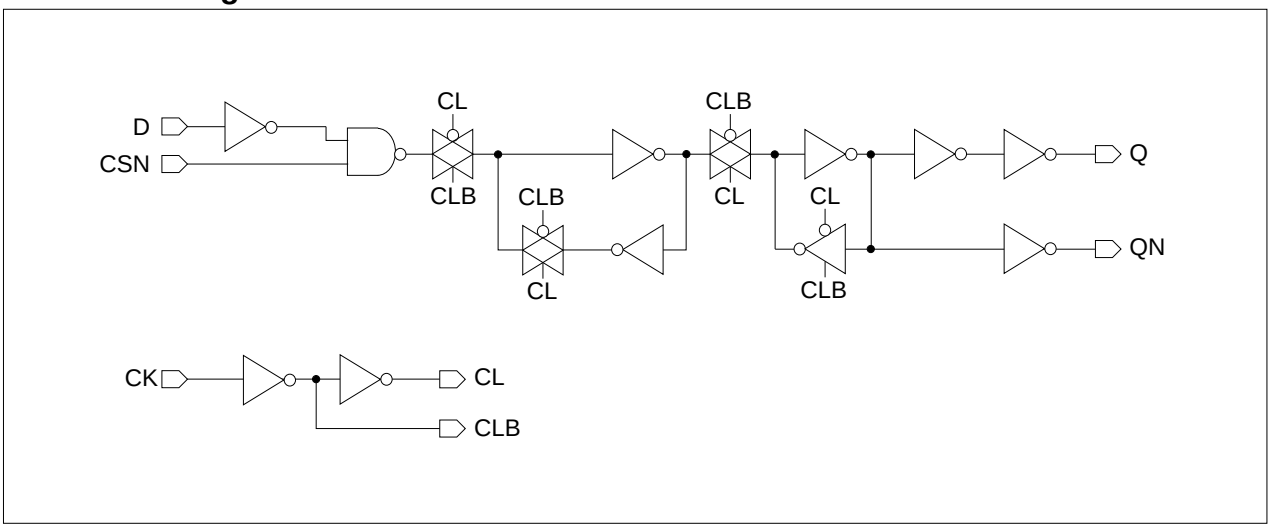
Truth Table

D	CSN	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	1	0
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FDS3			*FDS3D2*			*FDS3*	*FDS3D2*
D	CSN	CK	D	CSN	CK		
0.7	1.0	0.7	0.7	1.0	0.7	6.67	7.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS3	FDS3D2
Pulse Width Low (CK)	t_{PWL}	0.375	0.375
Pulse Width High (CK)	t_{PWH}	0.395	0.408
Input Setup Time (D to CK)	t_{SU}	0.923	0.923
Input Hold Time (D to CK)	t_{HD}	0.135	0.135
Input Setup Time (CSN to CK)	t_{SU}	0.898	0.898
Input Hold Time (CSN to CK)	t_{HD}	0.113	0.113

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FDS3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.133	0.061 + 0.036*SL	0.052 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.115	0.051 + 0.032*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.473	0.437 + 0.018*SL	0.440 + 0.017*SL	0.440 + 0.017*SL
	t_{PHL}	0.474	0.436 + 0.019*SL	0.442 + 0.018*SL	0.443 + 0.018*SL
CK to QN	t_R	0.146	0.074 + 0.036*SL	0.065 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.124	0.060 + 0.032*SL	0.056 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.408	0.370 + 0.019*SL	0.376 + 0.017*SL	0.378 + 0.017*SL
	t_{PHL}	0.407	0.367 + 0.020*SL	0.377 + 0.018*SL	0.381 + 0.018*SL

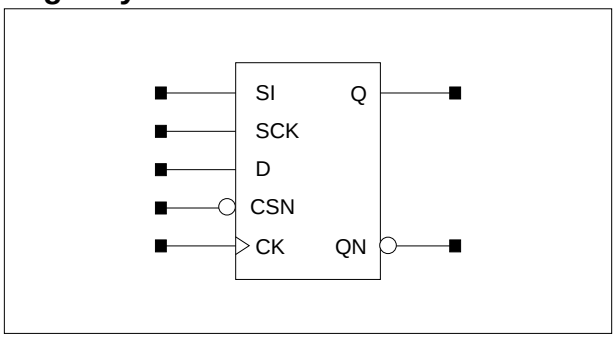
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FDS3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.099	0.064 + 0.018*SL	0.058 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.085	0.054 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.512	0.491 + 0.011*SL	0.498 + 0.009*SL	0.501 + 0.009*SL
	t_{PHL}	0.510	0.487 + 0.011*SL	0.497 + 0.009*SL	0.504 + 0.009*SL
CK to QN	t_R	0.106	0.070 + 0.018*SL	0.065 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.088	0.056 + 0.016*SL	0.054 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.405	0.382 + 0.011*SL	0.392 + 0.009*SL	0.399 + 0.009*SL
	t_{PHL}	0.399	0.375 + 0.012*SL	0.387 + 0.009*SL	0.399 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



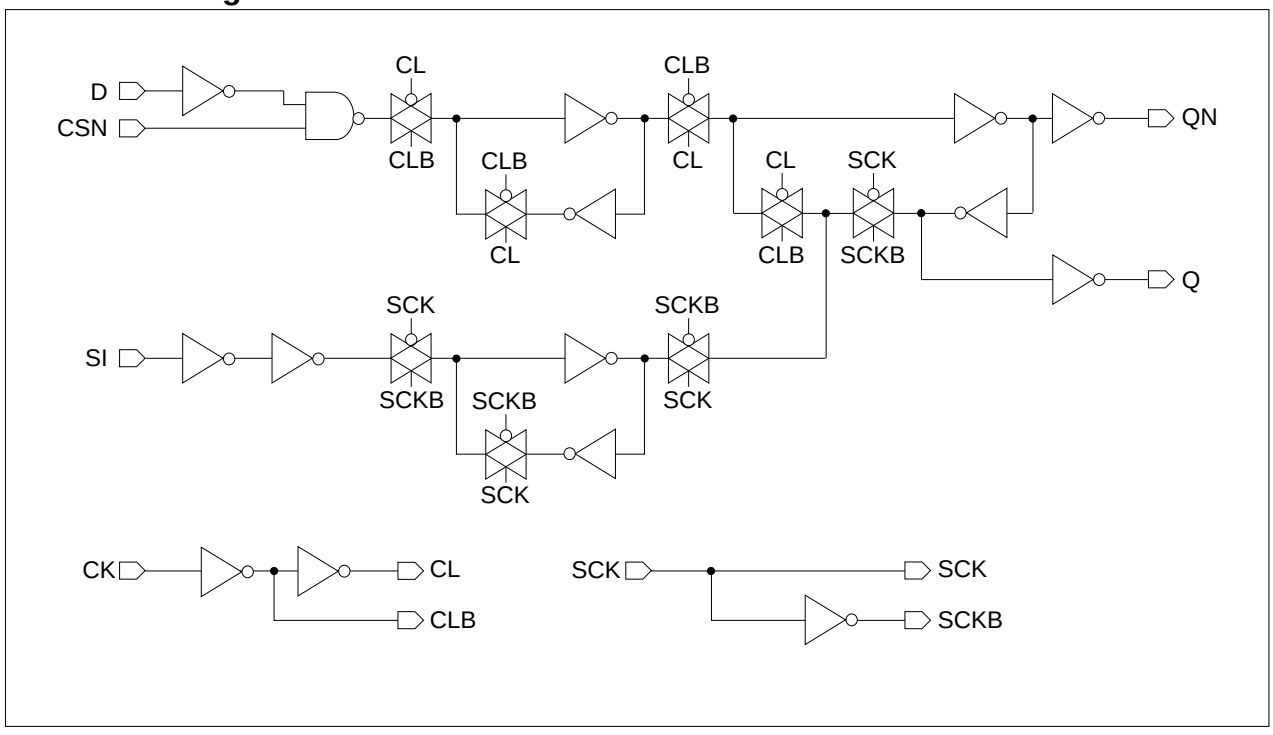
Truth Table

SI	SCK	D	CRN	CK	Q (n+1)	QN (n+1)
x	0	0	1	↑	0	1
x	0	1	1	↑	1	0
0	↑	x	x	0	0	1
1	↑	x	x	0	1	0
x	0	x	0	↑	1	0
x	0	x	x	↓	Q(n)	QN(n)
x	↓	x	x	0	Q(n)	QN(n)

Cell Data

Input Load (SL)										Gate Count	
FDS3CS					*FDS3CSD2*					*FDS3CS*	*FDS3CSD2*
CK	CSN	D	SCK	SI	CK	CSN	D	SCK	SI		
0.8	1.0	0.7	2.1	0.7	0.8	1.0	0.7	2.2	0.7	9.67	10.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS3CS	FDS3CSD2
Pulse Width Low (CK)	t_{PWL}	0.388	0.390
Pulse Width High (CK)	t_{PWH}	0.432	0.453
Pulse Width Low (SCK)	t_{PWL}	0.375	0.376
Pulse Width High (SCK)	t_{PWH}	0.430	0.457
Input Setup Time (D to CK)	t_{SU}	0.795	0.796
Input Hold Time (D to CK)	t_{HD}	0.257	0.258
Input Setup Time (SI to CK)	t_{SU}	0.853	0.854
Input Hold Time (SI to CK)	t_{HD}	0.000	0.000
Input Setup Time (CSN to CK)	t_{SU}	0.781	0.783
Input Hold Time (CSN to CK)	t_{HD}	0.253	0.253

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FDS3CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.157	0.087 + 0.035*SL	0.076 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.133	0.068 + 0.033*SL	0.066 + 0.033*SL	0.045 + 0.033*SL
	t_{PLH}	0.571	0.530 + 0.020*SL	0.542 + 0.018*SL	0.545 + 0.017*SL
	t_{PHL}	0.541	0.498 + 0.021*SL	0.512 + 0.018*SL	0.524 + 0.018*SL
SCK to Q	t_R	0.137	0.065 + 0.036*SL	0.055 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.119	0.056 + 0.031*SL	0.048 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.454	0.417 + 0.018*SL	0.421 + 0.017*SL	0.421 + 0.017*SL
	t_{PHL}	0.515	0.476 + 0.020*SL	0.484 + 0.018*SL	0.485 + 0.018*SL
CK to QN	t_R	0.145	0.074 + 0.036*SL	0.064 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.124	0.061 + 0.031*SL	0.054 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.425	0.387 + 0.019*SL	0.393 + 0.018*SL	0.396 + 0.017*SL
	t_{PHL}	0.439	0.399 + 0.020*SL	0.408 + 0.018*SL	0.413 + 0.018*SL
SCK to QN	t_R	0.152	0.081 + 0.036*SL	0.071 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.126	0.063 + 0.032*SL	0.058 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.438	0.399 + 0.019*SL	0.407 + 0.017*SL	0.409 + 0.017*SL
	t_{PHL}	0.375	0.334 + 0.020*SL	0.344 + 0.018*SL	0.349 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FDS3CSD2

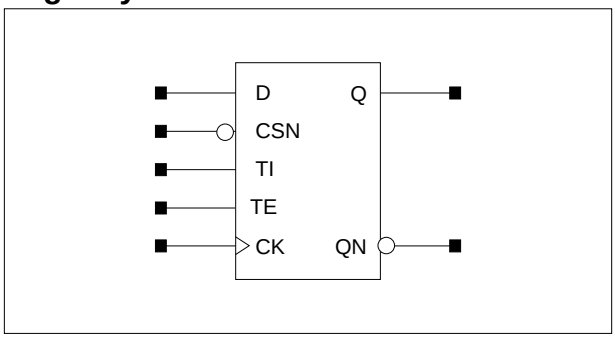
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.109	0.073 + 0.018*SL	0.068 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.092	0.059 + 0.017*SL	0.060 + 0.016*SL	0.035 + 0.017*SL
	t_{PLH}	0.570	0.547 + 0.011*SL	0.557 + 0.009*SL	0.565 + 0.009*SL
	t_{PHL}	0.545	0.520 + 0.012*SL	0.533 + 0.009*SL	0.551 + 0.009*SL
SCK to Q	t_R	0.095	0.060 + 0.017*SL	0.053 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.083	0.051 + 0.016*SL	0.048 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.474	0.454 + 0.010*SL	0.460 + 0.009*SL	0.462 + 0.009*SL
	t_{PHL}	0.532	0.509 + 0.011*SL	0.518 + 0.009*SL	0.525 + 0.009*SL
CK to QN	t_R	0.102	0.067 + 0.018*SL	0.061 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.088	0.057 + 0.016*SL	0.054 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.420	0.399 + 0.011*SL	0.407 + 0.009*SL	0.414 + 0.009*SL
	t_{PHL}	0.437	0.413 + 0.012*SL	0.425 + 0.009*SL	0.436 + 0.009*SL
SCK to QN	t_R	0.112	0.078 + 0.017*SL	0.070 + 0.019*SL	0.039 + 0.019*SL
	t_F	0.092	0.061 + 0.016*SL	0.058 + 0.016*SL	0.030 + 0.017*SL
	t_{PLH}	0.434	0.411 + 0.011*SL	0.421 + 0.009*SL	0.428 + 0.009*SL
	t_{PHL}	0.378	0.354 + 0.012*SL	0.366 + 0.009*SL	0.378 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FDS3S/FDS3SD2

Flip-Flop with Synchronous Set, Scan, 1X/2X Drive

Logic Symbol



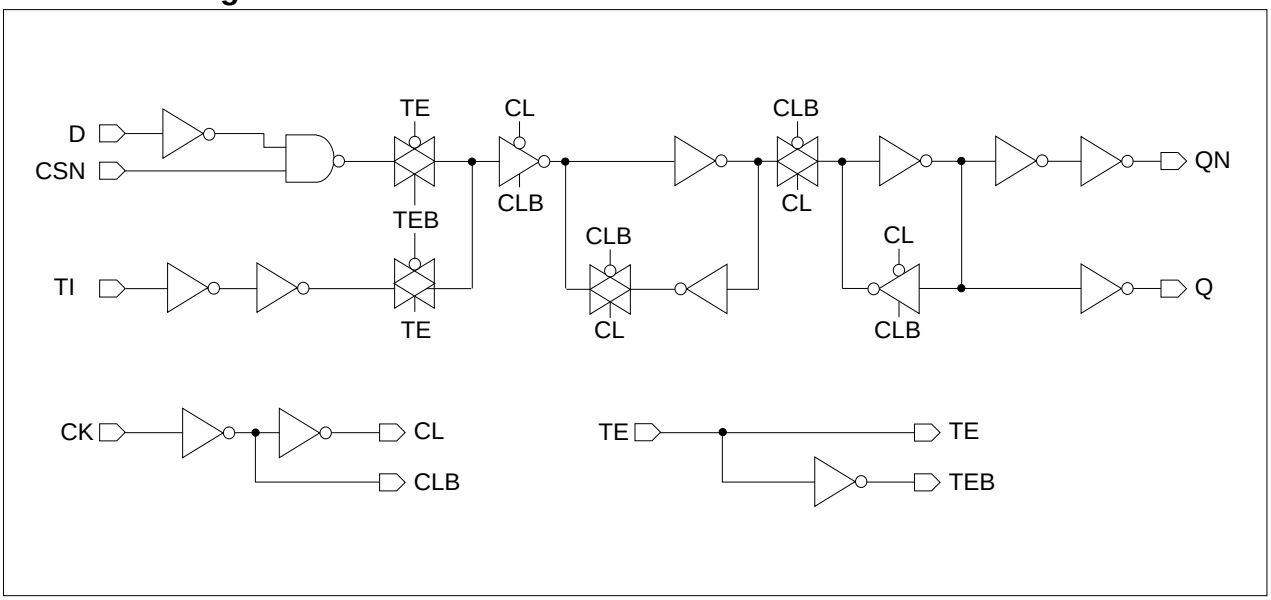
Truth Table

D	CSN	TI	TE	CK	Q(n+1)	QN(n+1)
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0
x	0	x	0	↑	1	0
x	x	x	x	↓	Q(n)	QN(n+1)

Cell Data

Input Load (SL)										Gate Count	
FDS3S					*FDS3SD2*					*FDS3S*	*FDS3SD2*
CK	CSN	D	TE	TI	CK	CSN	D	TE	TI		
0.7	1.0	0.7	1.3	0.7	0.7	1.0	0.7	1.3	0.7	8.67	9.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS3S	FDS3SD2
Pulse Width Low (CK)	t_{PWL}	0.423	0.423
Pulse Width High (CK)	t_{PWH}	0.395	0.407
Input Setup Time (D to CK)	t_{SU}	0.928	0.928
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (CSN to CK)	t_{SU}	1.093	1.093
Input Hold Time (CSN to CK)	t_{HD}	0.153	0.153
Input Setup Time (TI to CK)	t_{SU}	0.889	0.889
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	0.830	0.831
Input Hold Time (TE to CK)	t_{HD}	0.107	0.106

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FDS3S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.147	0.075 + 0.036*SL	0.066 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.125	0.061 + 0.032*SL	0.057 + 0.033*SL	0.038 + 0.034*SL
	t_{PLH}	0.405	0.366 + 0.019*SL	0.373 + 0.017*SL	0.375 + 0.017*SL
	t_{PHL}	0.403	0.363 + 0.020*SL	0.373 + 0.018*SL	0.377 + 0.018*SL
CK to QN	t_R	0.134	0.061 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.113	0.049 + 0.032*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.468	0.432 + 0.018*SL	0.435 + 0.017*SL	0.435 + 0.017*SL
	t_{PHL}	0.470	0.432 + 0.019*SL	0.438 + 0.018*SL	0.440 + 0.018*SL

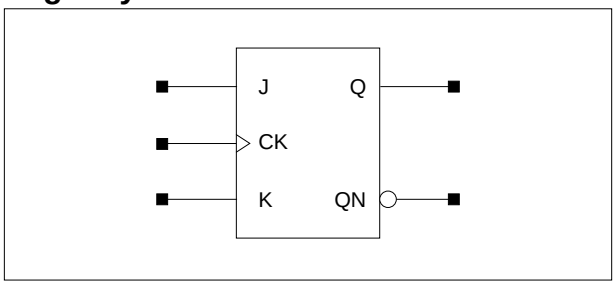
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FDS3SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.105	0.070 + 0.018*SL	0.064 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.088	0.056 + 0.016*SL	0.054 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.399	0.377 + 0.011*SL	0.386 + 0.009*SL	0.393 + 0.009*SL
	t_{PHL}	0.393	0.369 + 0.012*SL	0.381 + 0.009*SL	0.393 + 0.009*SL
CK to QN	t_R	0.099	0.064 + 0.018*SL	0.058 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.085	0.054 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.506	0.485 + 0.011*SL	0.492 + 0.009*SL	0.495 + 0.009*SL
	t_{PHL}	0.504	0.481 + 0.012*SL	0.491 + 0.009*SL	0.498 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



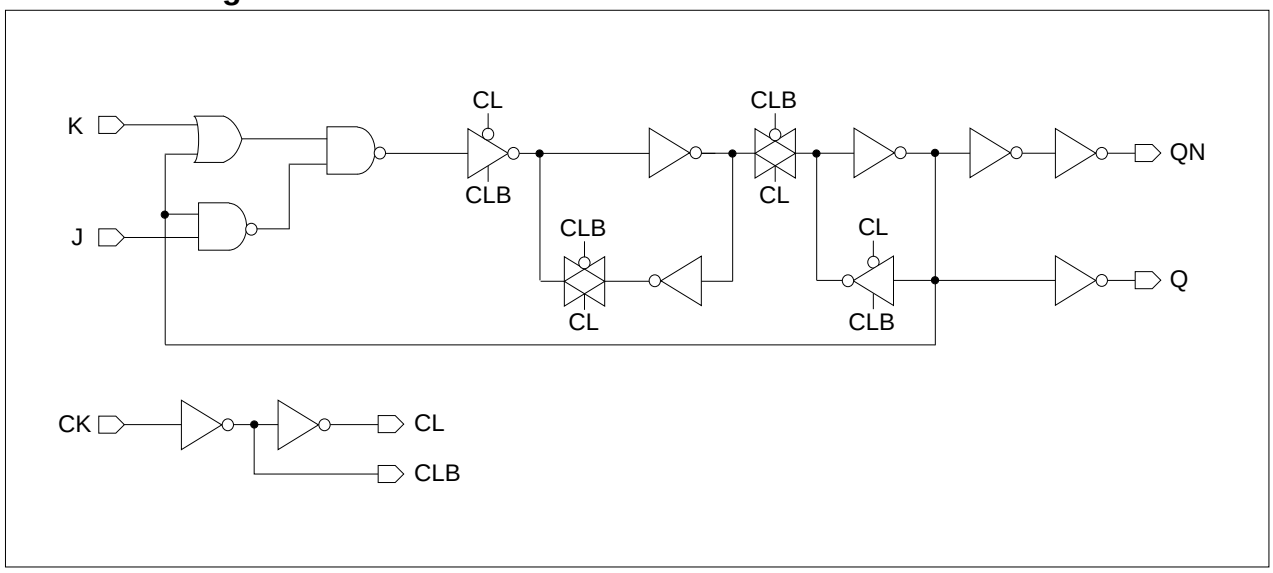
Truth Table

J	CK	K	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	0	1	0
0	↑	0	Q (n)	QN (n)
1	↑	1	QN (n)	Q (n)
x	↓	x	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FJ1			*FJ1D2*			*FJ1*	*FJ1D2*
J	CK	K	J	CK	K		
0.6	0.7	0.6	0.6	0.7	0.7	7.33	7.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C,3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ1	FJ1D2
Pulse Width Low (CK)	t_{PWL}	0.425	0.424
Pulse Width High (CK)	t_{PWH}	0.413	0.427
Input Setup Time (J to CK)	t_{SU}	0.396	0.387
Input Hold Time (J to CK)	t_{HD}	0.000	0.000
Input Setup Time (K to CK)	t_{SU}	0.396	0.387
Input Hold Time (K to CK)	t_{HD}	0.000	0.000

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FJ1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.157	0.086 + 0.036*SL	0.076 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.134	0.070 + 0.032*SL	0.067 + 0.033*SL	0.040 + 0.034*SL
	t_{PLH}	0.446	0.405 + 0.020*SL	0.416 + 0.018*SL	0.420 + 0.017*SL
	t_{PHL}	0.438	0.395 + 0.021*SL	0.409 + 0.018*SL	0.416 + 0.018*SL
CK to QN	t_R	0.137	0.065 + 0.036*SL	0.056 + 0.038*SL	0.047 + 0.038*SL
	t_F	0.114	0.052 + 0.031*SL	0.046 + 0.033*SL	0.035 + 0.033*SL
	t_{PLH}	0.506	0.470 + 0.018*SL	0.473 + 0.017*SL	0.473 + 0.017*SL
	t_{PHL}	0.512	0.474 + 0.019*SL	0.480 + 0.017*SL	0.482 + 0.017*SL

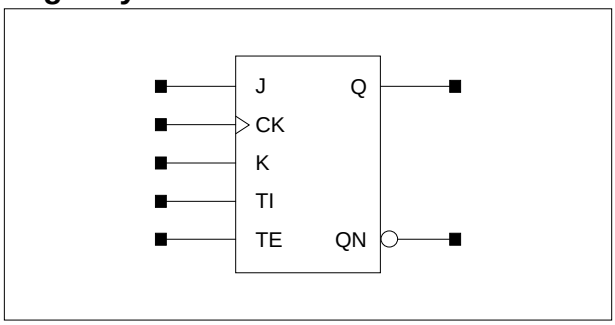
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FJ1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.117	0.080 + 0.018*SL	0.078 + 0.019*SL	0.043 + 0.019*SL
	t_F	0.100	0.067 + 0.017*SL	0.068 + 0.016*SL	0.035 + 0.017*SL
	t_{PLH}	0.444	0.420 + 0.012*SL	0.432 + 0.009*SL	0.444 + 0.009*SL
	t_{PHL}	0.428	0.402 + 0.013*SL	0.417 + 0.009*SL	0.435 + 0.009*SL
CK to QN	t_R	0.101	0.066 + 0.017*SL	0.059 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.084	0.051 + 0.016*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.545	0.524 + 0.011*SL	0.531 + 0.009*SL	0.533 + 0.009*SL
	t_{PHL}	0.549	0.527 + 0.011*SL	0.536 + 0.009*SL	0.543 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



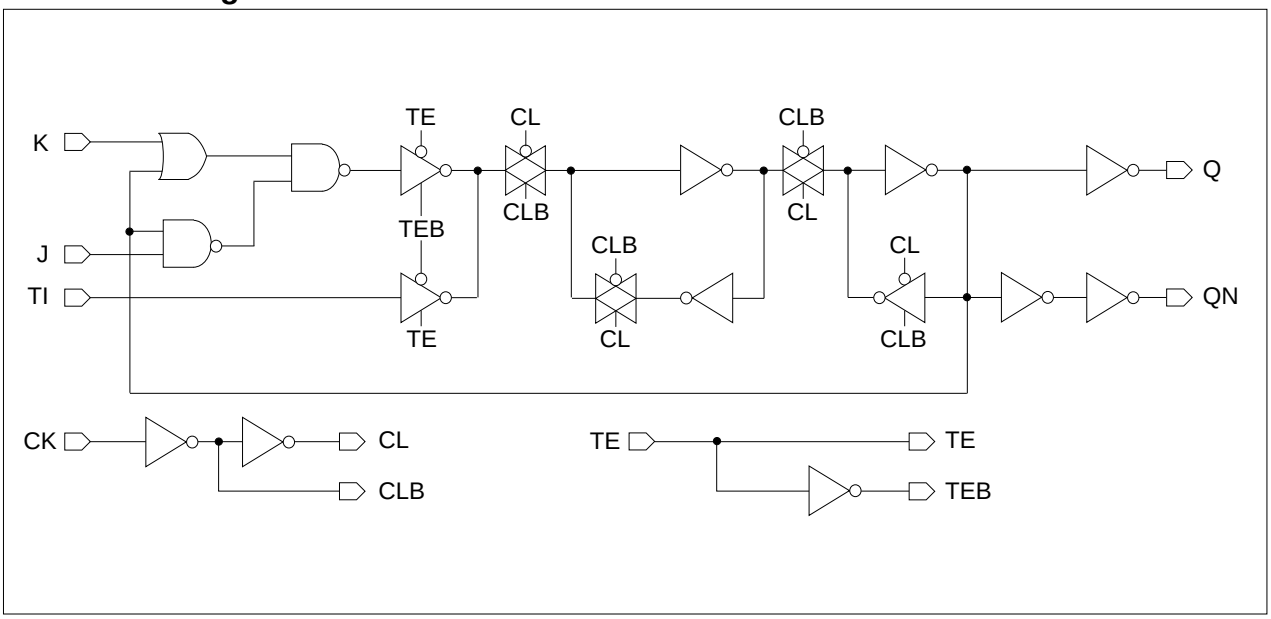
Truth Table

J	CK	K	TI	TE	Q (n+1)	QN (n+1)
0	↑	1	x	0	0	1
1	↑	0	x	0	1	0
0	↑	0	x	0	Q (n)	QN (n)
1	↑	1	x	0	QN (n)	Q (n)
x	↓	x	x	x	Q (n)	QN (n)
x	↑	x	0	1	0	1
x	↑	x	1	1	1	0

Cell Data

Input Load (SL)										Gate Count	
FJ1S					*FJ1SD2*					*FJ1S*	*FJ1SD2*
J	CK	K	TI	TE	J	CK	K	TI	TE		
0.6	0.7	0.6	0.7	1.5	0.6	0.7	0.6	0.7	1.5	9.00	9.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ1S	FJ1SD2
Pulse Width Low (CK)	t_{PWL}	0.405	0.405
Pulse Width High (CK)	t_{PWH}	0.414	0.429
Input Setup Time (J to CK)	t_{SU}	0.484	0.474
Input Hold Time (J to CK)	t_{HD}	0.000	0.000
Input Setup Time (K to CK)	t_{SU}	0.484	0.474
Input Hold Time (K to CK)	t_{HD}	0.000	0.000
Input Setup Time (TI to CK)	t_{SU}	0.975	0.975
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	1.042	1.043
Input Hold Time (TE to CK)	t_{HD}	0.055	0.056

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FJ1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.158	0.087 + 0.035*SL	0.077 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.136	0.072 + 0.032*SL	0.069 + 0.033*SL	0.040 + 0.034*SL
	t_{PLH}	0.445	0.405 + 0.020*SL	0.416 + 0.018*SL	0.421 + 0.017*SL
	t_{PHL}	0.440	0.396 + 0.022*SL	0.412 + 0.018*SL	0.418 + 0.018*SL
CK to QN	t_R	0.136	0.065 + 0.036*SL	0.056 + 0.038*SL	0.047 + 0.038*SL
	t_F	0.116	0.055 + 0.030*SL	0.047 + 0.033*SL	0.035 + 0.033*SL
	t_{PLH}	0.508	0.472 + 0.018*SL	0.475 + 0.017*SL	0.475 + 0.017*SL
	t_{PHL}	0.512	0.474 + 0.019*SL	0.480 + 0.017*SL	0.482 + 0.017*SL

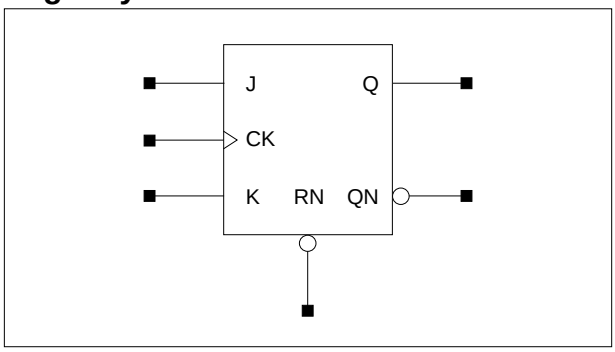
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FJ1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.118	0.083 + 0.018*SL	0.078 + 0.019*SL	0.044 + 0.019*SL
	t_F	0.102	0.069 + 0.017*SL	0.070 + 0.016*SL	0.035 + 0.017*SL
	t_{PLH}	0.446	0.422 + 0.012*SL	0.434 + 0.009*SL	0.447 + 0.009*SL
	t_{PHL}	0.431	0.405 + 0.013*SL	0.421 + 0.009*SL	0.440 + 0.009*SL
CK to QN	t_R	0.101	0.067 + 0.017*SL	0.059 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.084	0.052 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.548	0.527 + 0.011*SL	0.534 + 0.009*SL	0.537 + 0.009*SL
	t_{PHL}	0.551	0.528 + 0.011*SL	0.537 + 0.009*SL	0.544 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



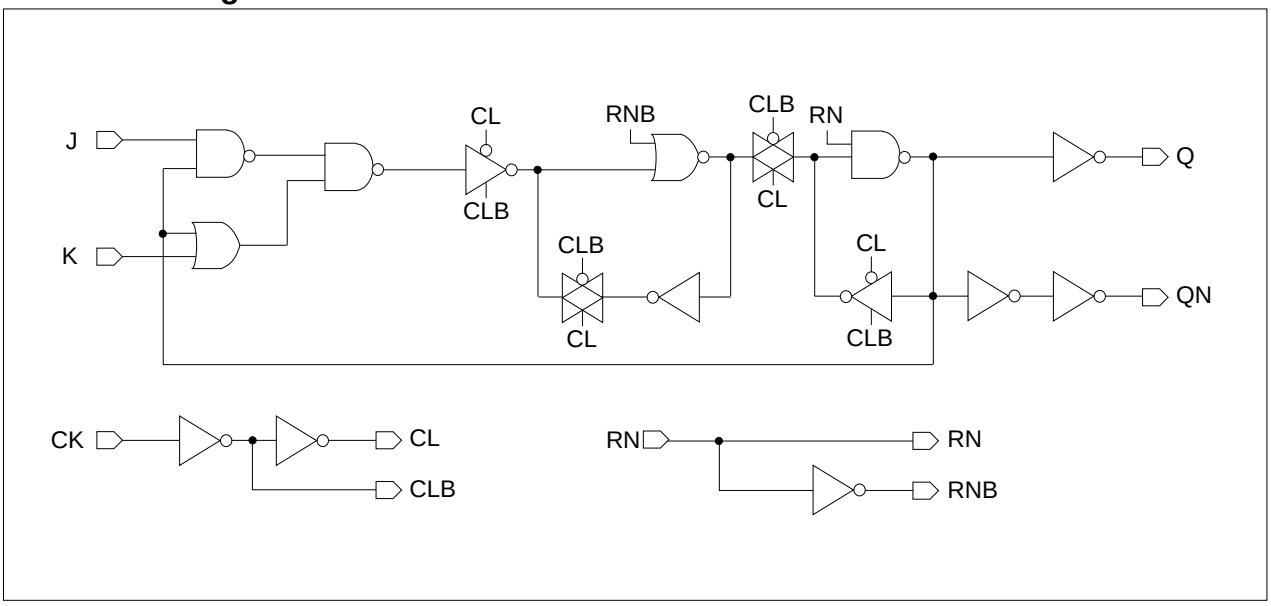
Truth Table

J	CK	K	RN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	0	1	1	0
0	↑	0	1	Q (n)	QN (n)
1	↑	1	1	QN (n)	Q (n)
x	↓	x	1	Q (n)	QN (n)
x	x	x	0	0	1

Cell Data

Input Load (SL)								Gate Count	
FJ2				*FJ2D2*				*FJ2*	*FJ2D2*
J	CK	K	RN	J	CK	K	RN		
0.6	0.7	0.6	2.0	0.6	0.7	0.6	2.0	8.33	8.67

Schematic Diagram



FJ2/FJ2D2

JK Flip-Flop with Reset, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ2	FJ2D2
Pulse Width Low (CK)	t_{PWL}	0.436	0.436
Pulse Width High (CK)	t_{PWH}	0.439	0.457
Pulse Width Low (RN)	t_{PWL}	0.400	0.429
Input Setup Time (J to CK)	t_{SU}	0.399	0.398
Input Hold Time (J to CK)	t_{HD}	0.000	0.000
Input Setup Time (K to CK)	t_{SU}	0.399	0.398
Input Hold Time (K to CK)	t_{HD}	0.000	0.000
Recovery Time (RN)	t_{RC}	0.293	0.292
Removal Time (RN)	t_{RM}	0.107	0.108

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FJ2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.172	0.098 + 0.037*SL	0.095 + 0.038*SL	0.063 + 0.038*SL
	t_F	0.148	0.083 + 0.032*SL	0.082 + 0.032*SL	0.050 + 0.033*SL
	t_{PLH}	0.487	0.444 + 0.022*SL	0.460 + 0.018*SL	0.473 + 0.017*SL
	t_{PHL}	0.486	0.440 + 0.023*SL	0.460 + 0.018*SL	0.475 + 0.018*SL
RN to Q	t_F	0.154	0.090 + 0.032*SL	0.088 + 0.032*SL	0.045 + 0.033*SL
	t_{PHL}	0.299	0.253 + 0.023*SL	0.274 + 0.018*SL	0.284 + 0.018*SL
CK to QN	t_R	0.137	0.066 + 0.036*SL	0.055 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.052 + 0.032*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.556	0.519 + 0.018*SL	0.522 + 0.017*SL	0.522 + 0.017*SL
	t_{PHL}	0.553	0.514 + 0.019*SL	0.520 + 0.018*SL	0.522 + 0.018*SL
RN to QN	t_R	0.138	0.067 + 0.035*SL	0.055 + 0.038*SL	0.045 + 0.039*SL
	t_{PLH}	0.369	0.333 + 0.018*SL	0.336 + 0.017*SL	0.336 + 0.017*SL

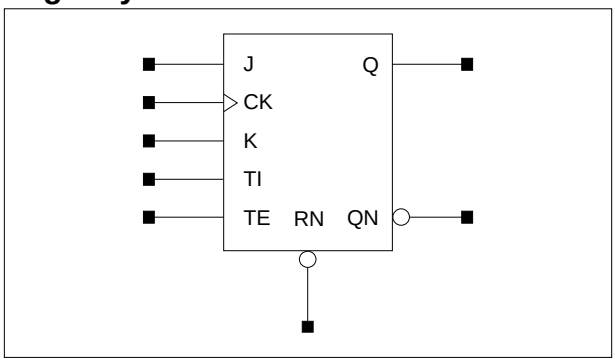
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FJ2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.134	0.096 + 0.019*SL	0.096 + 0.019*SL	0.061 + 0.019*SL
	t_F	0.118	0.084 + 0.017*SL	0.088 + 0.016*SL	0.052 + 0.017*SL
	t_{PLH}	0.487	0.461 + 0.013*SL	0.477 + 0.009*SL	0.505 + 0.009*SL
	t_{PHL}	0.484	0.456 + 0.014*SL	0.475 + 0.009*SL	0.509 + 0.009*SL
RN to Q	t_F	0.126	0.091 + 0.017*SL	0.096 + 0.016*SL	0.042 + 0.017*SL
	t_{PHL}	0.296	0.266 + 0.015*SL	0.288 + 0.009*SL	0.314 + 0.009*SL
CK to QN	t_R	0.105	0.071 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.089	0.056 + 0.016*SL	0.055 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.611	0.590 + 0.011*SL	0.597 + 0.009*SL	0.600 + 0.009*SL
	t_{PHL}	0.601	0.578 + 0.011*SL	0.588 + 0.009*SL	0.596 + 0.009*SL
RN to QN	t_R	0.105	0.071 + 0.017*SL	0.063 + 0.019*SL	0.036 + 0.020*SL
	t_{PLH}	0.424	0.403 + 0.011*SL	0.410 + 0.009*SL	0.413 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 60, *Group3 : 60 < SL

Logic Symbol



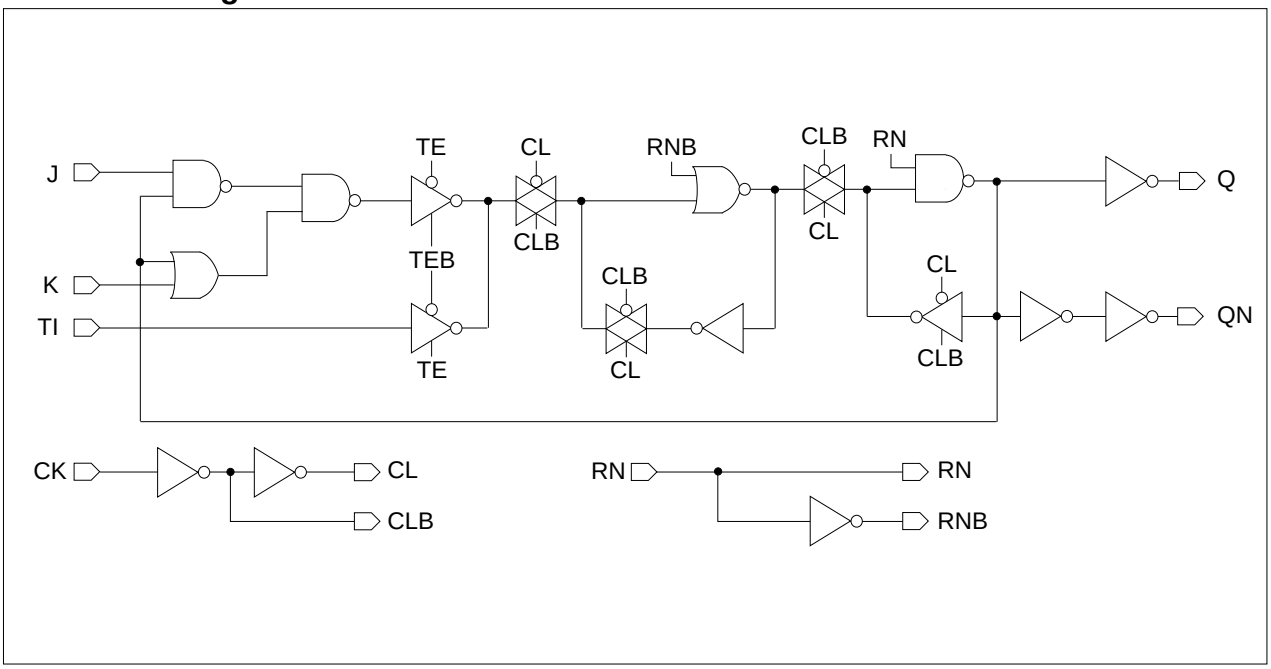
Truth Table

J	CK	K	TI	TE	RN	Q (n+1)	QN (n+1)
0	↑	1	x	0	1	0	1
1	↑	0	x	0	1	1	0
0	↑	0	x	0	1	Q (n)	QN (n)
1	↑	1	x	0	1	QN (n)	Q (n)
x	↓	x	x	x	1	Q (n)	QN (n)
x	x	x	x	x	0	0	1
x	↑	x	0	1	1	0	1
x	↑	x	1	1	1	1	0

Cell Data

Input Load (SL)												Gate Count	
FJ2S						*FJ2SD2*						*FJ2S*	*FJ2SD2*
J	CK	K	TI	TE	RN	J	CK	K	TI	TE	RN		
0.6	0.7	0.7	0.7	1.5	2.0	0.6	0.7	0.7	0.7	1.5	2.0	10.00	10.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ2S	FJ2SD2
Pulse Width Low (CK)	t_{PWL}	0.415	0.415
Pulse Width High (CK)	t_{PWH}	0.441	0.461
Pulse Width Low (RN)	t_{PWL}	0.396	0.423
Input Setup Time (J to CK)	t_{SU}	0.519	0.519
Input Hold Time (J to CK)	t_{HD}	0.000	0.000
Input Setup Time (K to CK)	t_{SU}	0.519	0.519
Input Hold Time (K to CK)	t_{HD}	0.000	0.000
Input Setup Time (TI to CK)	t_{SU}	0.988	0.988
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	1.068	1.068
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000
Recovery Time (RN)	t_{RC}	0.304	0.304
Removal Time (RN)	t_{RM}	0.096	0.096

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FJ2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.173	0.098 + 0.037*SL	0.098 + 0.038*SL	0.067 + 0.038*SL
	t_F	0.148	0.084 + 0.032*SL	0.082 + 0.032*SL	0.047 + 0.033*SL
	t_{PLH}	0.490	0.445 + 0.023*SL	0.463 + 0.018*SL	0.480 + 0.017*SL
	t_{PHL}	0.476	0.431 + 0.022*SL	0.449 + 0.018*SL	0.460 + 0.018*SL
RN to Q	t_F	0.152	0.090 + 0.031*SL	0.085 + 0.032*SL	0.042 + 0.033*SL
	t_{PHL}	0.290	0.245 + 0.023*SL	0.263 + 0.018*SL	0.270 + 0.018*SL
CK to QN	t_R	0.137	0.066 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.554	0.517 + 0.018*SL	0.520 + 0.017*SL	0.520 + 0.017*SL
	t_{PHL}	0.558	0.520 + 0.019*SL	0.526 + 0.018*SL	0.528 + 0.018*SL
RN to QN	t_R	0.137	0.066 + 0.036*SL	0.055 + 0.038*SL	0.045 + 0.039*SL
	t_{PLH}	0.368	0.331 + 0.018*SL	0.334 + 0.017*SL	0.334 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FJ2SD2

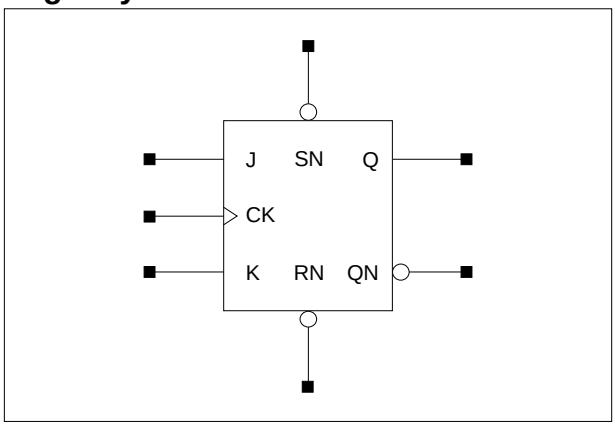
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.134	0.096 + 0.019*SL	0.097 + 0.019*SL	0.062 + 0.019*SL
	t_F	0.116	0.082 + 0.017*SL	0.085 + 0.016*SL	0.045 + 0.017*SL
	t_{PLH}	0.485	0.458 + 0.013*SL	0.475 + 0.009*SL	0.504 + 0.009*SL
	t_{PHL}	0.473	0.445 + 0.014*SL	0.464 + 0.009*SL	0.492 + 0.009*SL
RN to Q	t_F	0.121	0.087 + 0.017*SL	0.090 + 0.016*SL	0.036 + 0.017*SL
	t_{PHL}	0.284	0.256 + 0.014*SL	0.276 + 0.009*SL	0.297 + 0.009*SL
CK to QN	t_R	0.104	0.069 + 0.017*SL	0.062 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.089	0.057 + 0.016*SL	0.055 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.597	0.576 + 0.011*SL	0.584 + 0.009*SL	0.586 + 0.009*SL
	t_{PHL}	0.599	0.576 + 0.011*SL	0.586 + 0.009*SL	0.594 + 0.009*SL
RN to QN	t_R	0.103	0.068 + 0.018*SL	0.062 + 0.019*SL	0.035 + 0.020*SL
	t_{PLH}	0.410	0.389 + 0.011*SL	0.396 + 0.009*SL	0.398 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FJ4/FJ4D2

JK Flip-Flop with Reset, Set, 1X/2X Drive

Logic Symbol5



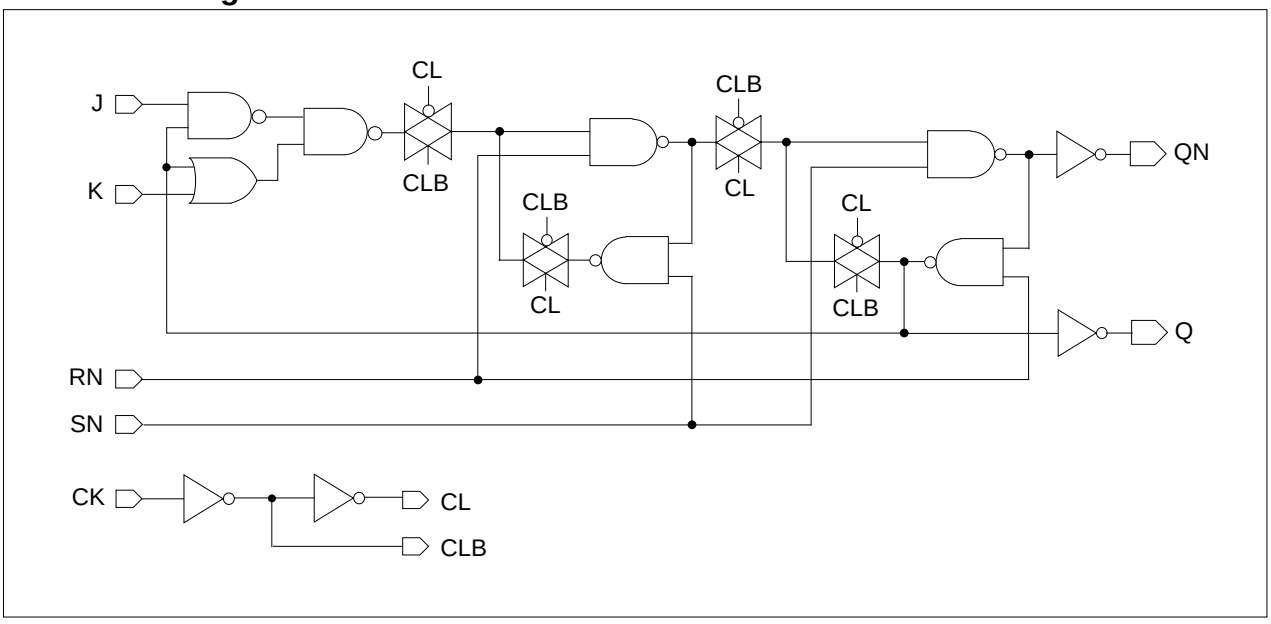
Truth Table

J	CK	K	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	1	0	1
1	↑	0	1	1	1	0
0	↑	0	1	1	Q (n)	QN (n)
1	↑	1	1	1	QN (n)	Q (n)
x	↓	x	1	1	Q (n)	QN (n)
x	x	x	0	1	0	1
x	x	x	1	0	1	0
x	x	x	0	0	0	0

Cell Data

Input Load (SL)										Gate Count	
FJ4					*FJ4D2*					*FJ4*	*FJ4D2*
J	CK	K	RN	SN	J	CK	K	RN	SN		
0.6	0.7	0.6	2.1	2.0	0.6	0.7	0.7	2.1	2.0	9.00	9.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ4	FJ4D2
Pulse Width Low (CK)	t_{PWL}	0.408	0.406
Pulse Width High (CK)	t_{PWH}	0.436	0.459
Pulse Width Low (RN)	t_{PWL}	0.399	0.432
Pulse Width Low (SN)	t_{PWL}	0.380	0.412
Input Setup Time (J to CK)	t_{SU}	0.248	0.245
Input Hold Time (J to CK)	t_{HD}	0.000	0.000
Input Setup Time (K to CK)	t_{SU}	0.248	0.245
Input Hold Time (K to CK)	t_{HD}	0.000	0.000
Recovery Time (RN)	t_{RC}	0.058	0.055
Removal Time (RN)	t_{RM}	0.341	0.341
Recovery Time (SN)	t_{RC}	0.000	0.000
Removal Time (SN)	t_{RM}	0.882	0.879

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FJ4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.158	0.085 + 0.036*SL	0.079 + 0.038*SL	0.054 + 0.039*SL
	t_F	0.128	0.065 + 0.032*SL	0.060 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.588	0.546 + 0.021*SL	0.559 + 0.018*SL	0.566 + 0.017*SL
	t_{PHL}	0.561	0.520 + 0.021*SL	0.532 + 0.018*SL	0.537 + 0.018*SL
RN to Q	t_R	0.183	0.109 + 0.037*SL	0.107 + 0.037*SL	0.071 + 0.038*SL
	t_F	0.148	0.084 + 0.032*SL	0.082 + 0.032*SL	0.049 + 0.033*SL
	t_{PLH}	0.272	0.226 + 0.023*SL	0.246 + 0.018*SL	0.265 + 0.017*SL
	t_{PHL}	0.276	0.230 + 0.023*SL	0.250 + 0.018*SL	0.264 + 0.018*SL
SN to Q	t_R	0.183	0.110 + 0.037*SL	0.107 + 0.037*SL	0.069 + 0.038*SL
	t_{PLH}	0.422	0.376 + 0.023*SL	0.397 + 0.018*SL	0.415 + 0.017*SL
CK to QN	t_R	0.155	0.082 + 0.037*SL	0.077 + 0.038*SL	0.058 + 0.039*SL
	t_F	0.125	0.061 + 0.032*SL	0.056 + 0.033*SL	0.040 + 0.034*SL
	t_{PLH}	0.444	0.403 + 0.020*SL	0.414 + 0.018*SL	0.423 + 0.017*SL
	t_{PHL}	0.450	0.409 + 0.020*SL	0.419 + 0.018*SL	0.426 + 0.018*SL
RN to QN	t_R	0.155	0.083 + 0.036*SL	0.076 + 0.038*SL	0.052 + 0.039*SL
	t_{PLH}	0.441	0.400 + 0.020*SL	0.412 + 0.018*SL	0.416 + 0.017*SL
SN to QN	t_R	0.153	0.080 + 0.036*SL	0.073 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.126	0.063 + 0.032*SL	0.057 + 0.033*SL	0.041 + 0.034*SL
	t_{PLH}	0.190	0.149 + 0.020*SL	0.160 + 0.018*SL	0.164 + 0.017*SL
	t_{PHL}	0.220	0.179 + 0.020*SL	0.189 + 0.018*SL	0.196 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

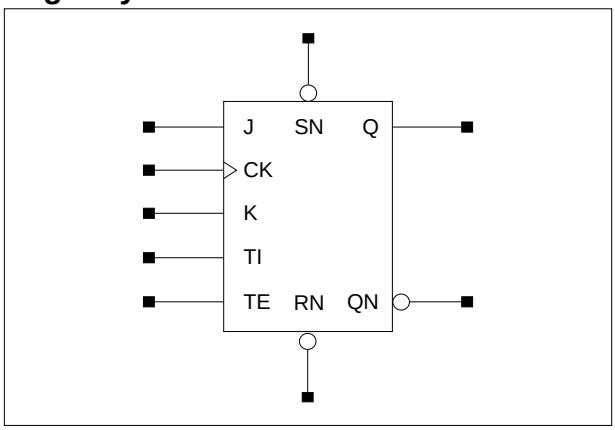
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FJ4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.120	0.082 + 0.019*SL	0.082 + 0.019*SL	0.049 + 0.019*SL
	t_F	0.097	0.064 + 0.016*SL	0.064 + 0.016*SL	0.032 + 0.017*SL
	t_{PLH}	0.611	0.586 + 0.013*SL	0.600 + 0.009*SL	0.619 + 0.009*SL
	t_{PHL}	0.588	0.563 + 0.013*SL	0.577 + 0.009*SL	0.592 + 0.009*SL
RN to Q	t_R	0.143	0.104 + 0.019*SL	0.106 + 0.019*SL	0.068 + 0.019*SL
	t_F	0.114	0.079 + 0.017*SL	0.084 + 0.016*SL	0.043 + 0.017*SL
	t_{PLH}	0.264	0.235 + 0.014*SL	0.255 + 0.009*SL	0.289 + 0.009*SL
	t_{PHL}	0.263	0.235 + 0.014*SL	0.254 + 0.009*SL	0.282 + 0.009*SL
SN to Q	t_R	0.144	0.107 + 0.019*SL	0.107 + 0.019*SL	0.066 + 0.019*SL
	t_{PLH}	0.442	0.414 + 0.014*SL	0.433 + 0.009*SL	0.467 + 0.009*SL
CK to QN	t_R	0.118	0.082 + 0.018*SL	0.078 + 0.019*SL	0.051 + 0.019*SL
	t_F	0.091	0.059 + 0.016*SL	0.058 + 0.017*SL	0.032 + 0.017*SL
	t_{PLH}	0.441	0.417 + 0.012*SL	0.429 + 0.009*SL	0.448 + 0.009*SL
	t_{PHL}	0.441	0.417 + 0.012*SL	0.429 + 0.009*SL	0.443 + 0.009*SL
RN to QN	t_R	0.118	0.081 + 0.018*SL	0.078 + 0.019*SL	0.045 + 0.019*SL
	t_{PLH}	0.466	0.441 + 0.012*SL	0.454 + 0.009*SL	0.467 + 0.009*SL
SN to QN	t_R	0.114	0.078 + 0.018*SL	0.074 + 0.019*SL	0.043 + 0.019*SL
	t_F	0.091	0.058 + 0.017*SL	0.058 + 0.016*SL	0.032 + 0.017*SL
	t_{PLH}	0.187	0.163 + 0.012*SL	0.175 + 0.009*SL	0.188 + 0.009*SL
	t_{PHL}	0.211	0.187 + 0.012*SL	0.199 + 0.009*SL	0.213 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



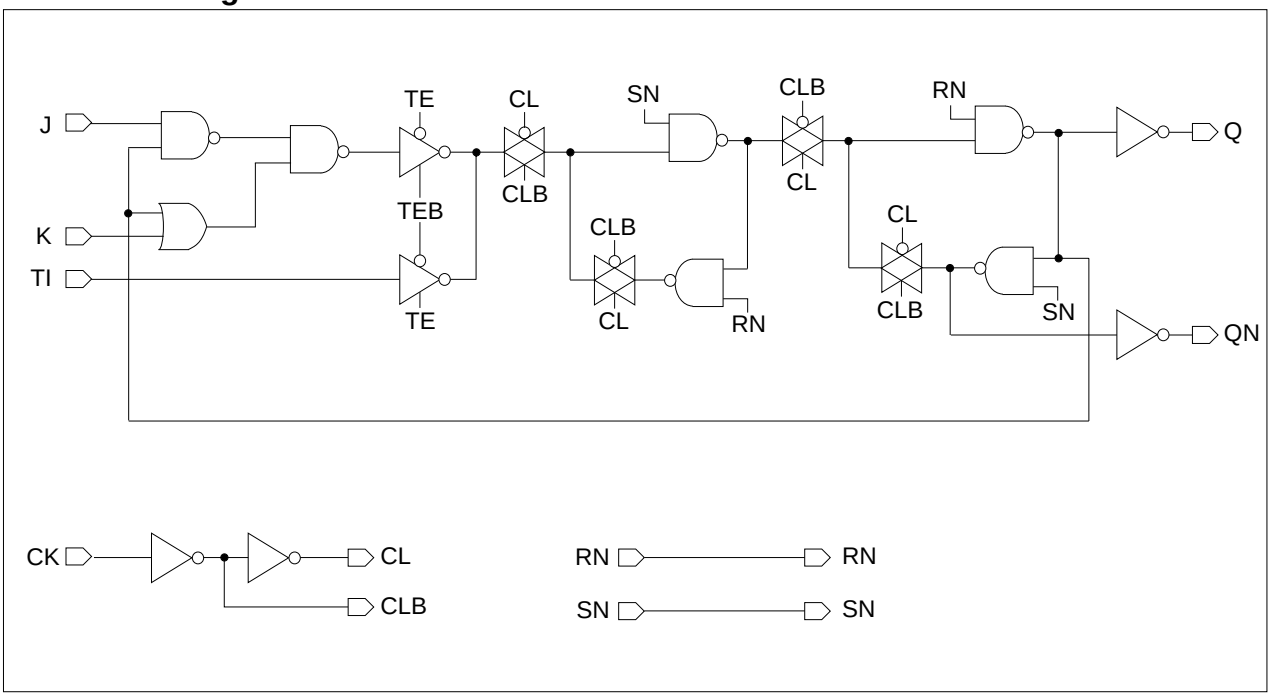
Truth Table

J	CK	K	TI	TE	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	x	0	1	1	0	1
1	↑	0	x	0	1	1	1	0
0	↑	0	x	0	1	1	Q (n)	QN (n)
1	↑	1	x	0	1	1	QN (n)	Q (n)
x	↓	x	x	x	1	1	Q (n)	QN (n)
x	x	x	x	x	0	1	0	1
x	x	x	x	x	1	0	1	0
x	x	x	x	x	0	0	0	0
x	↑	x	0	1	1	1	0	1
x	↑	x	1	1	1	1	1	0

Cell Data

Input Load (SL)														Gate Count	
FJ4S							*FJ4SD2*							*FJ4S*	*FJ4SD2*
J	CK	K	TI	TE	RN	SN	J	CK	K	TI	TE	RN	SN		
0.6	0.7	0.6	0.7	1.4	2.0	2.0	0.6	0.7	0.6	0.7	1.3	2.1	2.0	10.33	10.67

Schematic Diagram



FJ4S/FJ4SD2

JK Flip-Flop with Reset, Set, Scan, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ4S	FJ4SD2
Pulse Width Low (CK)	t_{PWL}	0.444	0.444
Pulse Width High (CK)	t_{PWH}	0.451	0.475
Pulse Width Low(RN)	t_{PWL}	0.390	0.424
Pulse Width Low (SN)	t_{PWL}	0.389	0.421
Input Setup Time (J to CK)	t_{SU}	0.485	0.488
Input Hold Time (J to CK)	t_{HD}	0.000	0.000
Input Setup Time (K to CK)	t_{SU}	0.485	0.488
Input Hold Time (K to CK)	t_{HD}	0.000	0.000
Input Setup Time (TI to CK)	t_{SU}	0.986	0.986
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	1.054	1.054
Input Hold Time (TE to CK)	t_{HD}	0.063	0.062
Recovery Time (RN)	t_{RC}	0.000	0.000
Removal Time (RN)	t_{RM}	0.888	0.888
Recovery Time (SN)	t_{RC}	0.049	0.049
Removal Time (SN)	t_{RM}	0.352	0.352

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FJ4S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.168	0.094 + 0.037*SL	0.092 + 0.038*SL	0.064 + 0.038*SL
	t_F	0.136	0.072 + 0.032*SL	0.069 + 0.033*SL	0.041 + 0.034*SL
	t_{PLH}	0.490	0.446 + 0.022*SL	0.462 + 0.018*SL	0.476 + 0.017*SL
	t_{PHL}	0.489	0.445 + 0.022*SL	0.460 + 0.018*SL	0.468 + 0.018*SL
RN to Q	t_R	0.164	0.091 + 0.037*SL	0.086 + 0.038*SL	0.056 + 0.039*SL
	t_F	0.136	0.073 + 0.031*SL	0.068 + 0.033*SL	0.041 + 0.034*SL
	t_{PLH}	0.226	0.183 + 0.021*SL	0.198 + 0.018*SL	0.206 + 0.017*SL
	t_{PHL}	0.249	0.206 + 0.021*SL	0.220 + 0.018*SL	0.228 + 0.018*SL
SN to Q	t_R	0.167	0.096 + 0.036*SL	0.089 + 0.038*SL	0.057 + 0.039*SL
	t_{PLH}	0.451	0.408 + 0.021*SL	0.423 + 0.018*SL	0.431 + 0.017*SL
CK to QN	t_R	0.147	0.075 + 0.036*SL	0.066 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.120	0.056 + 0.032*SL	0.052 + 0.033*SL	0.035 + 0.034*SL
	t_{PLH}	0.591	0.552 + 0.020*SL	0.560 + 0.018*SL	0.563 + 0.017*SL
	t_{PHL}	0.576	0.536 + 0.020*SL	0.545 + 0.018*SL	0.548 + 0.018*SL
RN to QN	t_R	0.171	0.098 + 0.037*SL	0.095 + 0.038*SL	0.061 + 0.038*SL
	t_{PLH}	0.418	0.373 + 0.022*SL	0.391 + 0.018*SL	0.404 + 0.017*SL
SN to QN	t_R	0.171	0.098 + 0.037*SL	0.094 + 0.038*SL	0.061 + 0.038*SL
	t_F	0.137	0.072 + 0.033*SL	0.071 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.235	0.190 + 0.022*SL	0.208 + 0.018*SL	0.221 + 0.017*SL
	t_{PHL}	0.246	0.202 + 0.022*SL	0.218 + 0.018*SL	0.232 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FJ4SD2

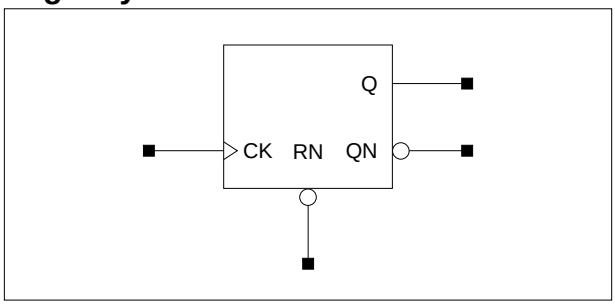
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.130	0.092 + 0.019*SL	0.091 + 0.019*SL	0.060 + 0.019*SL
	t_F	0.102	0.069 + 0.017*SL	0.070 + 0.016*SL	0.036 + 0.017*SL
	t_{PLH}	0.484	0.458 + 0.013*SL	0.473 + 0.009*SL	0.500 + 0.009*SL
	t_{PHL}	0.478	0.452 + 0.013*SL	0.467 + 0.009*SL	0.486 + 0.009*SL
RN to Q	t_R	0.125	0.088 + 0.019*SL	0.086 + 0.019*SL	0.051 + 0.019*SL
	t_F	0.103	0.070 + 0.016*SL	0.070 + 0.016*SL	0.034 + 0.017*SL
	t_{PLH}	0.221	0.195 + 0.013*SL	0.211 + 0.009*SL	0.231 + 0.009*SL
	t_{PHL}	0.239	0.213 + 0.013*SL	0.229 + 0.009*SL	0.247 + 0.009*SL
SN to Q	t_R	0.129	0.092 + 0.019*SL	0.091 + 0.019*SL	0.052 + 0.019*SL
	t_{PLH}	0.473	0.447 + 0.013*SL	0.463 + 0.009*SL	0.483 + 0.009*SL
CK to QN	t_R	0.109	0.073 + 0.018*SL	0.070 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.090	0.057 + 0.016*SL	0.056 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.619	0.595 + 0.012*SL	0.606 + 0.009*SL	0.617 + 0.009*SL
	t_{PHL}	0.605	0.581 + 0.012*SL	0.593 + 0.009*SL	0.603 + 0.009*SL
RN to QN	t_R	0.134	0.096 + 0.019*SL	0.096 + 0.019*SL	0.057 + 0.019*SL
	t_{PLH}	0.442	0.415 + 0.013*SL	0.432 + 0.009*SL	0.458 + 0.009*SL
SN to QN	t_R	0.132	0.093 + 0.019*SL	0.095 + 0.019*SL	0.057 + 0.019*SL
	t_F	0.103	0.069 + 0.017*SL	0.072 + 0.016*SL	0.041 + 0.017*SL
	t_{PLH}	0.230	0.203 + 0.013*SL	0.220 + 0.009*SL	0.246 + 0.009*SL
	t_{PHL}	0.236	0.210 + 0.013*SL	0.226 + 0.009*SL	0.251 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

FT2/FT2D2

Toggle Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



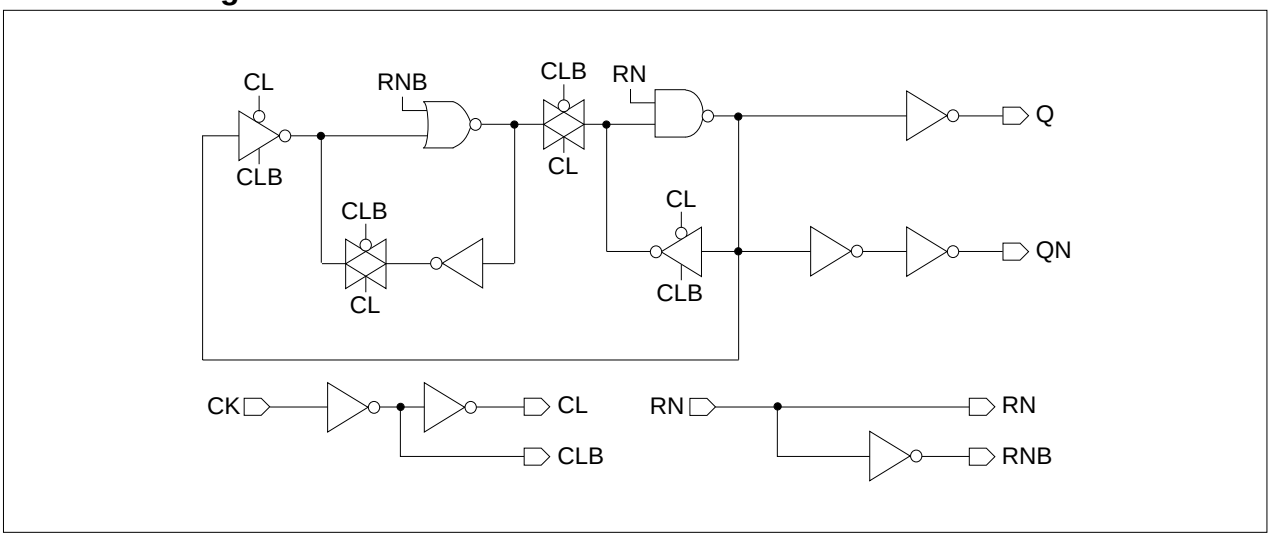
Truth Table

CK	RN	Q (n+1)	QN (n+1)
⎍	1	QN (n)	Q (n)
⎎	1	Q (n)	QN (n)
x	0	0	1

Cell Data

Input Load (SL)				Gate Count	
FT2		*FT2D2*		*FT2*	*FT2D2*
CK	RN	CK	RN		
0.7	2.0	0.7	2.0	6.67	7.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FT2	FT2D2
Pulse Width Low (CK)	t_{PWL}	0.388	0.388
Pulse Width High (CK)	t_{PWH}	0.429	0.449
Pulse Width Low (RN)	t_{PWL}	0.378	0.407
Recovery Time (RN)	t_{RC}	0.306	0.306
Removal Time (RN)	t_{RM}	0.094	0.094

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FT2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.167	0.095 + 0.036*SL	0.089 + 0.038*SL	0.058 + 0.039*SL
	t_F	0.138	0.074 + 0.032*SL	0.072 + 0.033*SL	0.043 + 0.033*SL
	t_{PLH}	0.468	0.425 + 0.021*SL	0.440 + 0.018*SL	0.449 + 0.017*SL
	t_{PHL}	0.457	0.413 + 0.022*SL	0.429 + 0.018*SL	0.438 + 0.018*SL
RN to Q	t_F	0.135	0.077 + 0.029*SL	0.063 + 0.033*SL	0.035 + 0.034*SL
	t_{PHL}	0.272	0.231 + 0.021*SL	0.242 + 0.018*SL	0.244 + 0.018*SL
CK to QN	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.525	0.488 + 0.018*SL	0.491 + 0.017*SL	0.491 + 0.017*SL
	t_{PHL}	0.534	0.495 + 0.019*SL	0.502 + 0.018*SL	0.503 + 0.018*SL
RN to QN	t_R	0.135	0.062 + 0.036*SL	0.053 + 0.038*SL	0.045 + 0.039*SL
	t_{PLH}	0.339	0.303 + 0.018*SL	0.306 + 0.017*SL	0.306 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

FT2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.131	0.094 + 0.018*SL	0.093 + 0.019*SL	0.056 + 0.019*SL
	t_F	0.110	0.077 + 0.017*SL	0.078 + 0.016*SL	0.042 + 0.017*SL
	t_{PLH}	0.472	0.446 + 0.013*SL	0.462 + 0.009*SL	0.484 + 0.009*SL
	t_{PHL}	0.457	0.430 + 0.013*SL	0.447 + 0.009*SL	0.471 + 0.009*SL
RN to Q	t_F	0.103	0.073 + 0.015*SL	0.067 + 0.016*SL	0.028 + 0.017*SL
	t_{PHL}	0.269	0.245 + 0.012*SL	0.257 + 0.009*SL	0.265 + 0.009*SL
CK to QN	t_R	0.103	0.069 + 0.017*SL	0.061 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.090	0.058 + 0.016*SL	0.055 + 0.016*SL	0.027 + 0.017*SL
	t_{PLH}	0.578	0.557 + 0.011*SL	0.564 + 0.009*SL	0.567 + 0.009*SL
	t_{PHL}	0.584	0.561 + 0.012*SL	0.572 + 0.009*SL	0.578 + 0.009*SL
RN to QN	t_R	0.099	0.064 + 0.018*SL	0.058 + 0.019*SL	0.035 + 0.020*SL
	t_{PLH}	0.381	0.360 + 0.011*SL	0.367 + 0.009*SL	0.369 + 0.009*SL

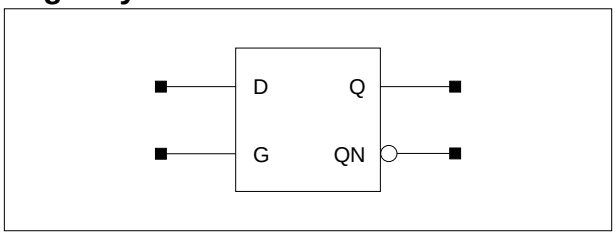
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

LATCHES

Cell List

Cell Name	Function Description
LD1	D Latch with Active High
LD1D2	D Latch with Active High, 2X Drive
LD1A	D Latch with Active High, Tri-State Output
LD1D2A	D Latch with Active High, Tri-State Output, 2x Drive
LD1Q	D Latch with Active High, Q Output Only
LD1QD2	D Latch with Active High, Q Output Only, 2X Drive
LD2	D Latch with Active High, Reset
LD2D2	D Latch with Active High, Reset, 2X Drive
LD2Q	D Latch with Active High, Reset, Q Output Only
LD2QD2	D Latch with Active High, Reset, Q Output Only, 2X Drive
LD3	D Latch with Active High, Set
LD3D2	D Latch with Active High, Set, 2X Drive
LD4	D Latch with Active High, Reset, Set
LD4D2	D Latch with Active High, Reset, Set, 2X Drive
LD5	D Latch with Active Low
LD5D2	D Latch with Active Low, 2X Drive
LD5S	D Latch with Active Low, Scan
LD5SD2	D Latch with Active Low, Scan, 2X Drive
LD5Q	D Latch with Active Low, Q Output Only
LD5QD2	D Latch with Active Low, Q Output Only, 2X Drive
LD6	D Latch with Active Low, Reset
LD6D2	D Latch with Active Low, Reset, 2X Drive
LD6Q	D Latch with Active Low, Reset, Q Output Only
LD6QD2	D Latch with Active Low, Reset, Q Output Only, 2X Drive
LD7	D Latch with Active Low, Set
LD7D2	D Latch with Active Low, Set, 2X Drive
LD8	D Latch with Active Low, Reset, Set
LD8D2	D Latch with Active Low, Reset, Set, 2X Drive
LS0	SR Latch
LS0D2	SR Latch with 2X Drive
LS1	SR Latch with Separate Inputs
LS1D2	SR Latch with Separate Inputs, 2X Drive

Logic Symbol



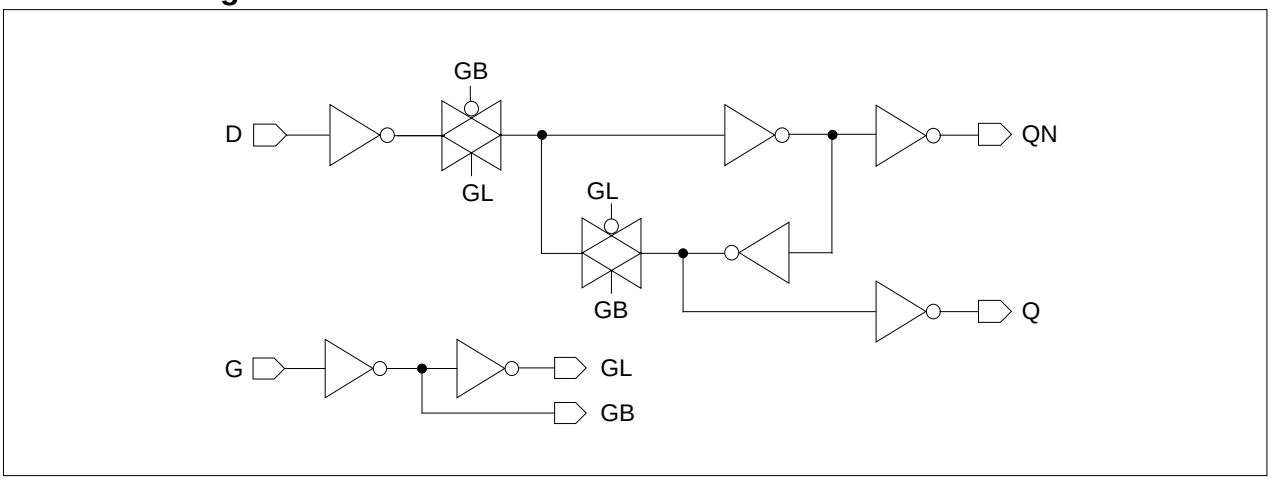
Truth Table

D	G	Q (n+1)	QN (n+1)
0	1	0	1
1	1	1	0
x	0	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
LD1		*LD1D2*		*LD1*	*LD1D2*
D	G	D	G		
0.8	0.8	0.8	0.8	4.00	4.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD1	LD1D2
Pulse Width High (G)	t_{PWH}	0.399	0.428
Input Setup Time (D to G)	t_{SU}	0.464	0.497
Input Hold Time (D to G)	t_{HD}	0.324	0.285

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

LD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.046 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.394	0.358 + 0.018*SL	0.361 + 0.017*SL	0.362 + 0.017*SL
	t_{PHL}	0.407	0.368 + 0.020*SL	0.375 + 0.018*SL	0.377 + 0.018*SL
G to Q	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.053 + 0.032*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.464	0.427 + 0.018*SL	0.431 + 0.017*SL	0.431 + 0.017*SL
	t_{PHL}	0.463	0.424 + 0.020*SL	0.432 + 0.018*SL	0.434 + 0.018*SL
D to QN	t_R	0.146	0.073 + 0.036*SL	0.065 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.123	0.059 + 0.032*SL	0.055 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.332	0.293 + 0.019*SL	0.300 + 0.018*SL	0.303 + 0.017*SL
	t_{PHL}	0.316	0.275 + 0.020*SL	0.285 + 0.018*SL	0.289 + 0.018*SL
G to QN	t_R	0.145	0.073 + 0.036*SL	0.064 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.123	0.059 + 0.032*SL	0.055 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.388	0.350 + 0.019*SL	0.356 + 0.018*SL	0.359 + 0.017*SL
	t_{PHL}	0.385	0.344 + 0.020*SL	0.354 + 0.018*SL	0.359 + 0.018*SL

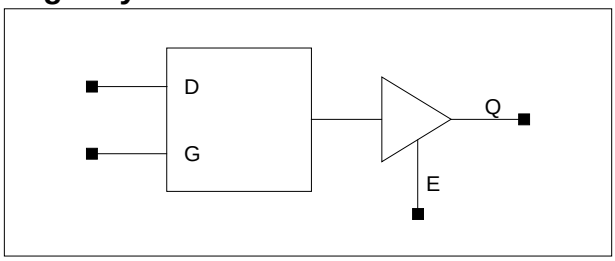
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

LD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.102	0.066 + 0.018*SL	0.061 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.087	0.054 + 0.016*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.437	0.415 + 0.011*SL	0.424 + 0.009*SL	0.427 + 0.009*SL
	t_{PHL}	0.449	0.426 + 0.012*SL	0.436 + 0.009*SL	0.444 + 0.009*SL
G to Q	t_R	0.102	0.068 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.087	0.056 + 0.016*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.507	0.485 + 0.011*SL	0.493 + 0.009*SL	0.497 + 0.009*SL
	t_{PHL}	0.505	0.482 + 0.012*SL	0.493 + 0.009*SL	0.501 + 0.009*SL
D to QN	t_R	0.109	0.074 + 0.018*SL	0.068 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.090	0.057 + 0.017*SL	0.057 + 0.016*SL	0.031 + 0.017*SL
	t_{PLH}	0.336	0.313 + 0.011*SL	0.323 + 0.009*SL	0.332 + 0.009*SL
	t_{PHL}	0.313	0.289 + 0.012*SL	0.301 + 0.009*SL	0.314 + 0.009*SL
G to QN	t_R	0.109	0.074 + 0.018*SL	0.068 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.091	0.059 + 0.016*SL	0.057 + 0.016*SL	0.031 + 0.017*SL
	t_{PLH}	0.392	0.370 + 0.011*SL	0.379 + 0.009*SL	0.388 + 0.009*SL
	t_{PHL}	0.383	0.359 + 0.012*SL	0.371 + 0.009*SL	0.384 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



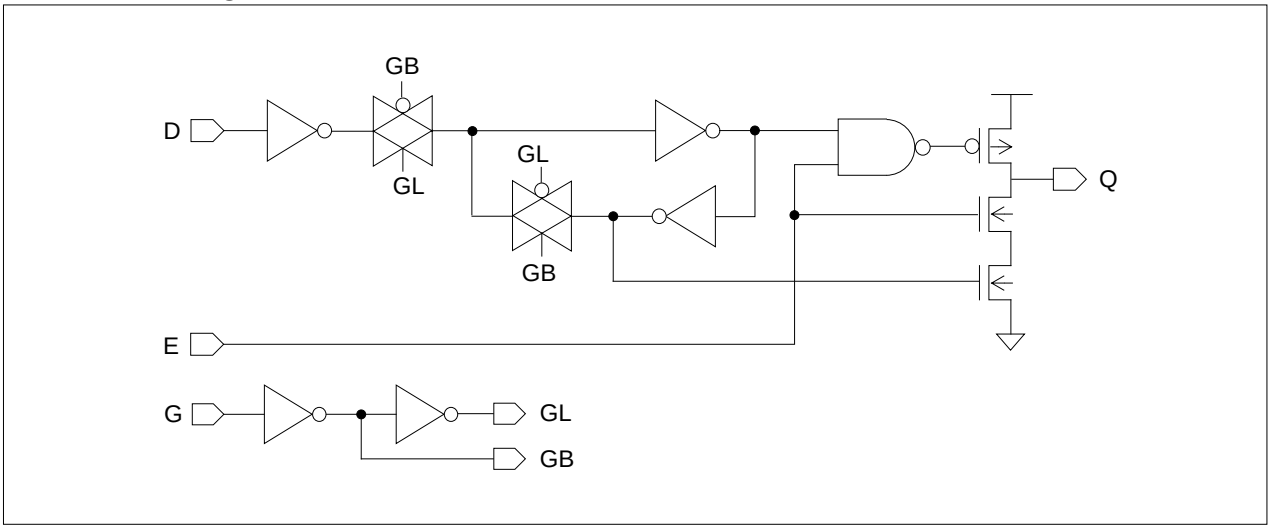
Truth Table

D	G	E	Q (n+1)
x	x	0	Hi-Z
0	1	1	0
1	1	1	1
x	0	1	Q (n)

Cell Data

Input Load (SL)						Output Load (SL)		Gate Count	
LD1A			*LD1D2A*			*LD1A*	*LD1D2A*	*LD1A*	*LD1D2A*
D	G	E	D	G	E	Q	Q		
0.8	0.8	1.3	0.8	0.8	1.5	0.9	1.1	4.67	5.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD1A	LD1D2A
Pulse Width High (G)	t_{PWH}	0.393	0.395
Input Setup Time (D to G)	t_{SU}	0.458	0.460
Input Hold Time (D to G)	t_{HD}	0.331	0.327

Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD1A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.149	0.077 + 0.036*SL	0.070 + 0.038*SL	0.059 + 0.038*SL
	t_F	0.169	0.066 + 0.051*SL	0.059 + 0.053*SL	0.056 + 0.053*SL
	t_{PLH}	0.391	0.353 + 0.019*SL	0.359 + 0.017*SL	0.361 + 0.017*SL
	t_{PHL}	0.412	0.360 + 0.026*SL	0.362 + 0.025*SL	0.364 + 0.025*SL
G to Q	t_R	0.150	0.078 + 0.036*SL	0.070 + 0.038*SL	0.059 + 0.038*SL
	t_F	0.169	0.065 + 0.052*SL	0.060 + 0.053*SL	0.056 + 0.053*SL
	t_{PLH}	0.460	0.423 + 0.019*SL	0.428 + 0.017*SL	0.430 + 0.017*SL
	t_{PHL}	0.469	0.417 + 0.026*SL	0.419 + 0.025*SL	0.420 + 0.025*SL
E to Q	t_R	0.201	0.146 + 0.027*SL	0.088 + 0.042*SL	0.066 + 0.043*SL
	t_F	0.242	0.136 + 0.053*SL	0.106 + 0.060*SL	0.065 + 0.061*SL
	t_{PLH}	0.144	0.104 + 0.020*SL	0.115 + 0.017*SL	0.206 + 0.015*SL
	t_{PHL}	0.105	0.044 + 0.031*SL	0.066 + 0.025*SL	0.200 + 0.021*SL
	t_{PLZ}	0.128	0.128 + 0.000*SL	0.128 + 0.000*SL	0.128 + 0.000*SL
	t_{PHZ}	0.177	0.177 + 0.000*SL	0.177 + 0.000*SL	0.177 + 0.000*SL

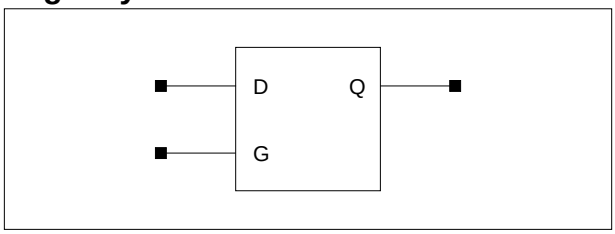
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

LD1D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.109	0.073 + 0.018*SL	0.070 + 0.019*SL	0.050 + 0.019*SL
	t_F	0.106	0.056 + 0.025*SL	0.050 + 0.027*SL	0.039 + 0.027*SL
	t_{PLH}	0.384	0.362 + 0.011*SL	0.371 + 0.009*SL	0.379 + 0.009*SL
	t_{PHL}	0.388	0.361 + 0.013*SL	0.364 + 0.013*SL	0.365 + 0.013*SL
G to Q	t_R	0.110	0.074 + 0.018*SL	0.070 + 0.019*SL	0.050 + 0.019*SL
	t_F	0.106	0.055 + 0.026*SL	0.050 + 0.027*SL	0.039 + 0.027*SL
	t_{PLH}	0.454	0.431 + 0.011*SL	0.441 + 0.009*SL	0.448 + 0.009*SL
	t_{PHL}	0.444	0.418 + 0.013*SL	0.420 + 0.013*SL	0.421 + 0.013*SL
E to Q	t_R	0.211	0.211 + 0.000*SL	0.110 + 0.021*SL	0.056 + 0.022*SL
	t_F	0.170	0.114 + 0.028*SL	0.103 + 0.031*SL	0.046 + 0.031*SL
	t_{PLH}	0.133	0.109 + 0.012*SL	0.123 + 0.009*SL	0.219 + 0.007*SL
	t_{PHL}	0.058	0.017 + 0.021*SL	0.047 + 0.013*SL	0.186 + 0.011*SL
	t_{PLZ}	0.128	0.128 + 0.000*SL	0.128 + 0.000*SL	0.128 + 0.000*SL
	t_{PHZ}	0.204	0.204 + 0.000*SL	0.204 + 0.000*SL	0.203 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



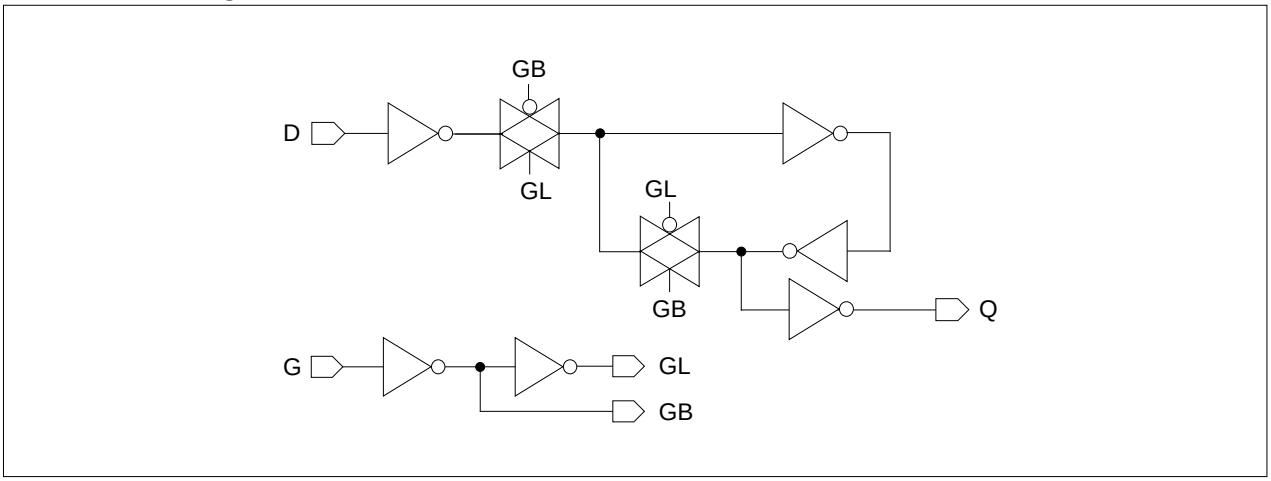
Truth Table

D	G	Q (n+1)
0	1	0
1	1	1
x	0	Q (n)

Cell Data

Input Load (SL)				Gate Count	
LD1Q		*LD1QD2*		*LD1Q*	*LD1QD2*
D	G	D	G		
0.8	0.8	0.8	0.8	3.67	4.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD1Q	LD1QD2
Pulse Width High (G)	t_{PWH}	0.378	0.383
Input Setup Time (D to G)	t_{SU}	0.431	0.438
Input Hold Time (D to G)	t_{HD}	0.353	0.345

Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD1Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.134	0.062 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.113	0.049 + 0.032*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.355	0.318 + 0.018*SL	0.322 + 0.017*SL	0.322 + 0.017*SL
	t_{PHL}	0.363	0.324 + 0.019*SL	0.330 + 0.018*SL	0.332 + 0.018*SL
G to Q	t_R	0.134	0.061 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.115	0.052 + 0.032*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.425	0.388 + 0.018*SL	0.392 + 0.017*SL	0.392 + 0.017*SL
	t_{PHL}	0.419	0.380 + 0.019*SL	0.387 + 0.018*SL	0.389 + 0.018*SL

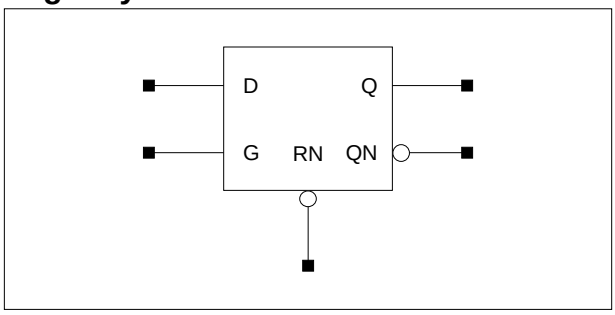
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

LD1QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.099	0.064 + 0.018*SL	0.057 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.081	0.048 + 0.017*SL	0.048 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.361	0.339 + 0.011*SL	0.347 + 0.009*SL	0.351 + 0.009*SL
	t_{PHL}	0.362	0.339 + 0.012*SL	0.349 + 0.009*SL	0.358 + 0.009*SL
G to Q	t_R	0.098	0.063 + 0.018*SL	0.057 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.081	0.048 + 0.017*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.430	0.409 + 0.011*SL	0.417 + 0.009*SL	0.420 + 0.009*SL
	t_{PHL}	0.418	0.395 + 0.012*SL	0.406 + 0.009*SL	0.414 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



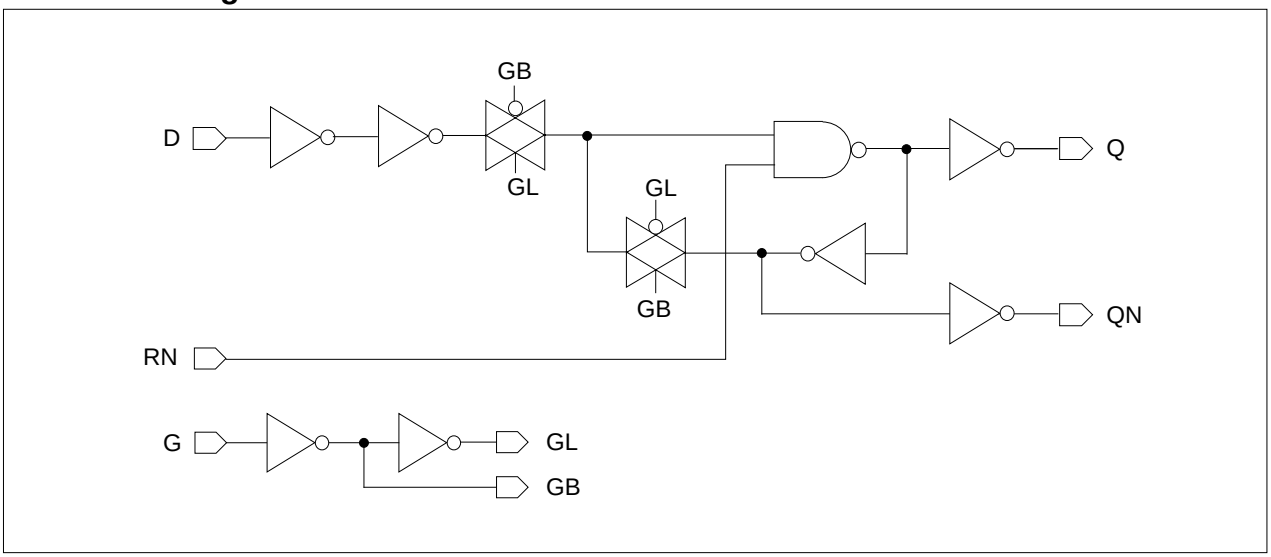
Truth Table

D	G	RN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
LD2			*LD2D2*			*LD2*	*LD2D2*
D	G	RN	D	G	RN		
0.8	0.8	1.1	0.8	0.8	1.1	4.67	5.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD2	LD2D2
Pulse Width High (G)	t_{PWH}	0.409	0.435
Pulse Width Low (RN)	t_{PWL}	0.352	0.389
Input Setup Time (D to G)	t_{SU}	0.288	0.310
Input Hold Time (D to G)	t_{HD}	0.160	0.137
Recovery Time (RN)	t_{RC}	0.000	0.000
Removal Time (RN)	t_{RM}	0.627	0.561

Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.151	0.078 + 0.037*SL	0.073 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.120	0.055 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.384	0.344 + 0.020*SL	0.354 + 0.018*SL	0.360 + 0.017*SL
	t_{PHL}	0.396	0.356 + 0.020*SL	0.365 + 0.018*SL	0.369 + 0.018*SL
G to Q	t_R	0.151	0.078 + 0.037*SL	0.072 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.120	0.055 + 0.033*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.404	0.364 + 0.020*SL	0.374 + 0.018*SL	0.381 + 0.017*SL
	t_{PHL}	0.396	0.356 + 0.020*SL	0.365 + 0.018*SL	0.369 + 0.018*SL
RN to Q	t_R	0.150	0.076 + 0.037*SL	0.072 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.123	0.060 + 0.032*SL	0.054 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.183	0.143 + 0.020*SL	0.153 + 0.018*SL	0.159 + 0.017*SL
	t_{PHL}	0.212	0.172 + 0.020*SL	0.181 + 0.018*SL	0.185 + 0.018*SL
D to QN	t_R	0.136	0.063 + 0.036*SL	0.054 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.116	0.053 + 0.032*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.474	0.437 + 0.018*SL	0.441 + 0.017*SL	0.441 + 0.017*SL
	t_{PHL}	0.460	0.421 + 0.020*SL	0.428 + 0.018*SL	0.430 + 0.018*SL
G to QN	t_R	0.136	0.064 + 0.036*SL	0.055 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.118	0.055 + 0.031*SL	0.048 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.474	0.438 + 0.018*SL	0.442 + 0.017*SL	0.442 + 0.017*SL
	t_{PHL}	0.480	0.441 + 0.020*SL	0.448 + 0.018*SL	0.451 + 0.018*SL
RN to QN	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.118	0.055 + 0.031*SL	0.048 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.291	0.255 + 0.018*SL	0.258 + 0.017*SL	0.259 + 0.017*SL
	t_{PHL}	0.259	0.220 + 0.020*SL	0.227 + 0.018*SL	0.229 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD2D2

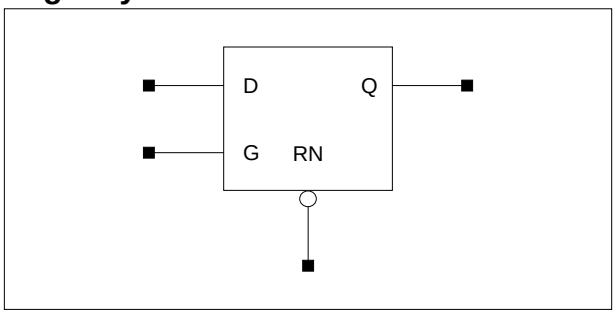
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.112	0.076 + 0.018*SL	0.073 + 0.019*SL	0.046 + 0.019*SL
	t_F	0.085	0.052 + 0.017*SL	0.053 + 0.017*SL	0.028 + 0.017*SL
	t_{PLH}	0.383	0.359 + 0.012*SL	0.371 + 0.009*SL	0.387 + 0.009*SL
	t_{PHL}	0.389	0.365 + 0.012*SL	0.377 + 0.009*SL	0.388 + 0.009*SL
G to Q	t_R	0.111	0.074 + 0.018*SL	0.072 + 0.019*SL	0.046 + 0.019*SL
	t_F	0.085	0.051 + 0.017*SL	0.053 + 0.017*SL	0.028 + 0.017*SL
	t_{PLH}	0.404	0.380 + 0.012*SL	0.392 + 0.009*SL	0.407 + 0.009*SL
	t_{PHL}	0.389	0.366 + 0.012*SL	0.377 + 0.009*SL	0.388 + 0.009*SL
RN to Q	t_R	0.110	0.073 + 0.018*SL	0.070 + 0.019*SL	0.045 + 0.019*SL
	t_F	0.089	0.057 + 0.016*SL	0.054 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.180	0.156 + 0.012*SL	0.168 + 0.009*SL	0.183 + 0.009*SL
	t_{PHL}	0.204	0.180 + 0.012*SL	0.192 + 0.009*SL	0.203 + 0.009*SL
D to QN	t_R	0.101	0.066 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.089	0.057 + 0.016*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.510	0.489 + 0.011*SL	0.497 + 0.009*SL	0.500 + 0.009*SL
	t_{PHL}	0.498	0.475 + 0.012*SL	0.486 + 0.009*SL	0.495 + 0.009*SL
G to QN	t_R	0.101	0.066 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.087	0.054 + 0.017*SL	0.055 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.511	0.489 + 0.011*SL	0.497 + 0.009*SL	0.501 + 0.009*SL
	t_{PHL}	0.519	0.495 + 0.012*SL	0.506 + 0.009*SL	0.515 + 0.009*SL
RN to QN	t_R	0.101	0.065 + 0.018*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.088	0.055 + 0.016*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.326	0.305 + 0.011*SL	0.313 + 0.009*SL	0.316 + 0.009*SL
	t_{PHL}	0.295	0.272 + 0.012*SL	0.282 + 0.009*SL	0.291 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

LD2Q/LD2QD2

D Latch with Active High, Reset, Q Output Only, 1X/2X Drive

Logic Symbol



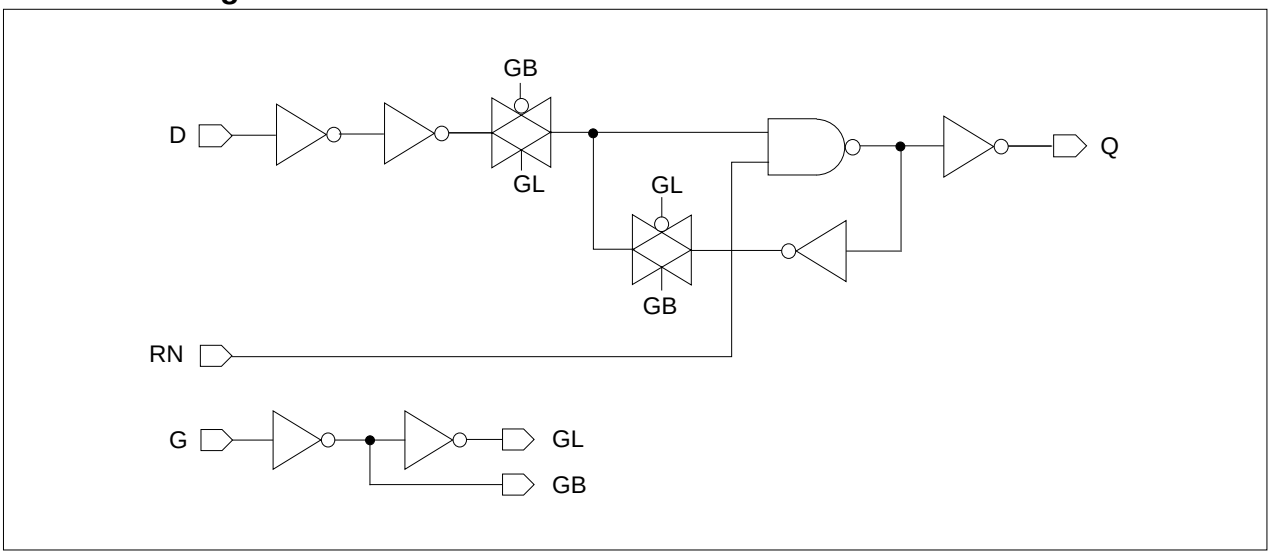
Truth Table

D	G	RN	Q (n+1)
0	1	1	0
1	1	1	1
x	0	1	Q (n)
x	x	0	0

Cell Data

Input Load (SL)						Gate Count	
LD2Q			*LD2QD2*			*LD2Q*	*LD2QD2*
D	G	RN	D	G	RN		
0.8	0.8	1.1	0.8	0.8	1.1	4.33	4.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD2Q	LD2QD2
Pulse Width High (G)	t_{PWH}	0.401	0.414
Pulse Width Low (RN)	t_{PWL}	0.332	0.357
Input Setup Time (D to G)	t_{SU}	0.281	0.294
Input Hold Time (D to G)	t_{HD}	0.166	0.150
Recovery Time (RN)	t_{RC}	0.000	0.000
Removal Time (RN)	t_{RM}	0.648	0.604

Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD2Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.153	0.081 + 0.036*SL	0.073 + 0.038*SL	0.051 + 0.038*SL
	t_F	0.122	0.058 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.387	0.347 + 0.020*SL	0.358 + 0.017*SL	0.363 + 0.017*SL
	t_{PHL}	0.397	0.357 + 0.020*SL	0.367 + 0.018*SL	0.370 + 0.018*SL
G to Q	t_R	0.152	0.079 + 0.036*SL	0.074 + 0.038*SL	0.051 + 0.038*SL
	t_F	0.122	0.059 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.408	0.367 + 0.020*SL	0.379 + 0.017*SL	0.383 + 0.017*SL
	t_{PHL}	0.398	0.357 + 0.020*SL	0.367 + 0.018*SL	0.370 + 0.018*SL
RN to Q	t_R	0.152	0.081 + 0.036*SL	0.073 + 0.038*SL	0.050 + 0.038*SL
	t_F	0.125	0.062 + 0.031*SL	0.056 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.185	0.145 + 0.020*SL	0.157 + 0.017*SL	0.161 + 0.017*SL
	t_{PHL}	0.213	0.173 + 0.020*SL	0.182 + 0.018*SL	0.185 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

LD2QD2

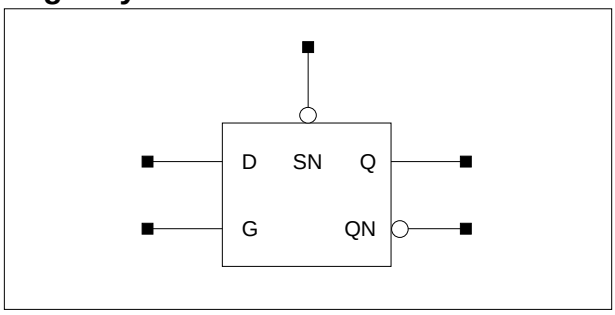
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.116	0.079 + 0.018*SL	0.077 + 0.019*SL	0.045 + 0.019*SL
	t_F	0.089	0.055 + 0.017*SL	0.056 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.389	0.365 + 0.012*SL	0.377 + 0.009*SL	0.392 + 0.009*SL
	t_{PHL}	0.392	0.369 + 0.012*SL	0.380 + 0.009*SL	0.391 + 0.009*SL
G to Q	t_R	0.114	0.077 + 0.019*SL	0.076 + 0.019*SL	0.045 + 0.019*SL
	t_F	0.088	0.054 + 0.017*SL	0.056 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.409	0.385 + 0.012*SL	0.398 + 0.009*SL	0.412 + 0.009*SL
	t_{PHL}	0.393	0.369 + 0.012*SL	0.380 + 0.009*SL	0.391 + 0.009*SL
RN to Q	t_R	0.114	0.077 + 0.018*SL	0.075 + 0.019*SL	0.044 + 0.019*SL
	t_F	0.091	0.059 + 0.016*SL	0.057 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.185	0.161 + 0.012*SL	0.173 + 0.009*SL	0.187 + 0.009*SL
	t_{PHL}	0.207	0.183 + 0.012*SL	0.195 + 0.009*SL	0.205 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

LD3/LD3D2

D Latch with Active High, Set, 1X/2X Drive

Logic Symbol



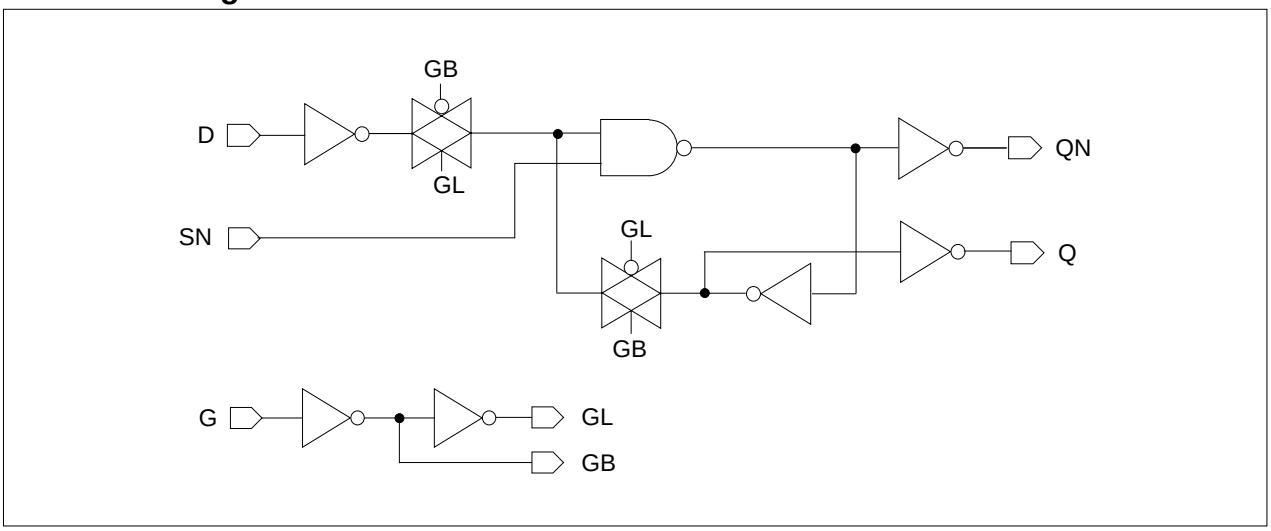
Truth Table

D	G	SN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	1	0

Cell Data

Input Load (SL)						Gate Count	
LD3			*LD3D2*			*LD3*	*LD3D2*
D	G	SN	D	G	SN		
0.8	0.8	1.1	0.8	0.8	1.1	4.33	5.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD3	LD3D2
Pulse Width High (G)	t_{PWH}	0.409	0.435
Pulse Width Low (SN)	t_{PWL}	0.352	0.389
Input Setup Time (D to G)	t_{SU}	0.479	0.506
Input Hold Time (D to G)	t_{HD}	0.306	0.274
Recovery Time (SN)	t_{RC}	0.000	0.000
Removal Time (SN)	t_{RM}	0.623	0.556

Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.053 + 0.032*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.403	0.366 + 0.018*SL	0.370 + 0.017*SL	0.370 + 0.017*SL
	t_{PHL}	0.420	0.381 + 0.020*SL	0.388 + 0.018*SL	0.390 + 0.018*SL
G to Q	t_R	0.135	0.063 + 0.036*SL	0.054 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.116	0.052 + 0.032*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.473	0.436 + 0.018*SL	0.440 + 0.017*SL	0.441 + 0.017*SL
	t_{PHL}	0.479	0.440 + 0.020*SL	0.447 + 0.018*SL	0.450 + 0.018*SL
SN to Q	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.118	0.055 + 0.031*SL	0.048 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.291	0.255 + 0.018*SL	0.258 + 0.017*SL	0.258 + 0.017*SL
	t_{PHL}	0.259	0.220 + 0.020*SL	0.227 + 0.018*SL	0.229 + 0.018*SL
D to QN	t_R	0.151	0.078 + 0.037*SL	0.073 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.122	0.058 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.344	0.304 + 0.020*SL	0.314 + 0.018*SL	0.321 + 0.017*SL
	t_{PHL}	0.324	0.284 + 0.020*SL	0.293 + 0.018*SL	0.297 + 0.018*SL
G to QN	t_R	0.151	0.078 + 0.037*SL	0.072 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.121	0.056 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.403	0.363 + 0.020*SL	0.373 + 0.018*SL	0.380 + 0.017*SL
	t_{PHL}	0.395	0.355 + 0.020*SL	0.364 + 0.018*SL	0.368 + 0.018*SL
SN to QN	t_R	0.150	0.076 + 0.037*SL	0.072 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.123	0.060 + 0.032*SL	0.054 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.183	0.143 + 0.020*SL	0.153 + 0.018*SL	0.159 + 0.017*SL
	t_{PHL}	0.212	0.172 + 0.020*SL	0.181 + 0.018*SL	0.185 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

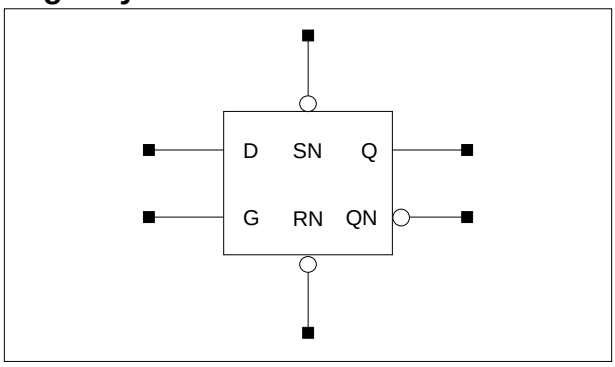
(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.101	0.067 + 0.017*SL	0.059 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.089	0.057 + 0.016*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.439	0.417 + 0.011*SL	0.425 + 0.009*SL	0.429 + 0.009*SL
	t_{PHL}	0.459	0.435 + 0.012*SL	0.446 + 0.009*SL	0.455 + 0.009*SL
G to Q	t_R	0.101	0.066 + 0.017*SL	0.059 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.089	0.057 + 0.016*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.509	0.488 + 0.011*SL	0.496 + 0.009*SL	0.500 + 0.009*SL
	t_{PHL}	0.518	0.494 + 0.012*SL	0.505 + 0.009*SL	0.514 + 0.009*SL
SN to Q	t_R	0.101	0.065 + 0.018*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.088	0.055 + 0.016*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.326	0.305 + 0.011*SL	0.313 + 0.009*SL	0.316 + 0.009*SL
	t_{PHL}	0.295	0.272 + 0.012*SL	0.283 + 0.009*SL	0.291 + 0.009*SL
D to QN	t_R	0.112	0.076 + 0.018*SL	0.073 + 0.019*SL	0.046 + 0.019*SL
	t_F	0.087	0.056 + 0.016*SL	0.052 + 0.017*SL	0.028 + 0.017*SL
	t_{PLH}	0.343	0.320 + 0.012*SL	0.331 + 0.009*SL	0.347 + 0.009*SL
	t_{PHL}	0.317	0.294 + 0.012*SL	0.305 + 0.009*SL	0.316 + 0.009*SL
G to QN	t_R	0.112	0.075 + 0.019*SL	0.072 + 0.019*SL	0.046 + 0.019*SL
	t_F	0.085	0.052 + 0.017*SL	0.052 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.402	0.379 + 0.012*SL	0.390 + 0.009*SL	0.406 + 0.009*SL
	t_{PHL}	0.388	0.364 + 0.012*SL	0.376 + 0.009*SL	0.387 + 0.009*SL
SN to QN	t_R	0.110	0.073 + 0.018*SL	0.070 + 0.019*SL	0.045 + 0.019*SL
	t_F	0.089	0.057 + 0.016*SL	0.054 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.180	0.156 + 0.012*SL	0.168 + 0.009*SL	0.183 + 0.009*SL
	t_{PHL}	0.204	0.180 + 0.012*SL	0.192 + 0.009*SL	0.203 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



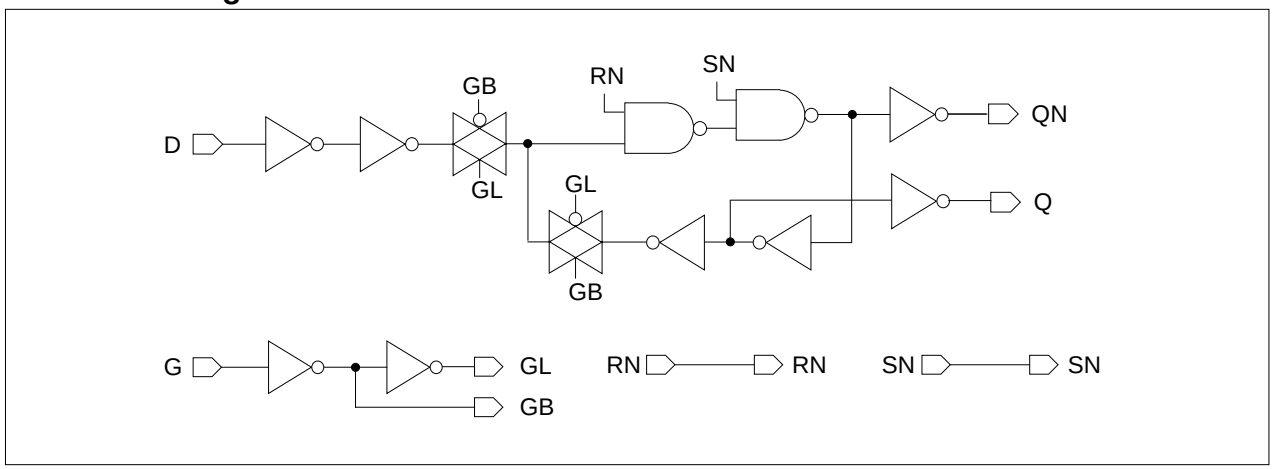
Truth Table

D	G	RN	SN	Q (n+1)	QN (n+1)
0	1	1	1	0	1
1	1	1	1	1	0
x	0	1	1	Q (n)	QN (n)
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0

Cell Data

Input Load (SL)								Gate Count	
LD4				*LD4D2*				*LD4*	*LD4D2*
D	G	SN	RN	D	G	SN	RN		
0.8	0.8	1.1	1.1	0.8	0.8	1.1	1.1	6.00	6.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD4	LD4D2
Pulse Width High (G)	t_{PWH}	0.460	0.495
Pulse Width Low (RN)	t_{PWL}	0.416	0.464
Pulse Width Low (SN)	t_{PWL}	0.407	0.446
Input Setup Time (D to G)	t_{SU}	0.328	0.298
Input Hold Time (D to G)	t_{HD}	0.123	0.034
Recovery Time (RN)	t_{RC}	0.000	0.000
Removal Time (RN)	t_{RM}	0.519	0.477
Recovery Time (SN)	t_{RC}	0.000	0.000
Removal Time (SN)	t_{RM}	0.636	0.548

Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.144	0.072 + 0.036*SL	0.063 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.125	0.062 + 0.031*SL	0.055 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.548	0.509 + 0.019*SL	0.517 + 0.017*SL	0.517 + 0.017*SL
	t_{PHL}	0.573	0.532 + 0.020*SL	0.543 + 0.018*SL	0.545 + 0.018*SL
G to Q	t_R	0.144	0.071 + 0.036*SL	0.063 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.125	0.062 + 0.031*SL	0.055 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.568	0.529 + 0.019*SL	0.537 + 0.017*SL	0.538 + 0.017*SL
	t_{PHL}	0.574	0.533 + 0.020*SL	0.543 + 0.018*SL	0.546 + 0.018*SL
SN to Q	t_R	0.144	0.072 + 0.036*SL	0.064 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.124	0.060 + 0.032*SL	0.055 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.312	0.273 + 0.019*SL	0.280 + 0.017*SL	0.281 + 0.017*SL
	t_{PHL}	0.281	0.240 + 0.020*SL	0.251 + 0.018*SL	0.254 + 0.018*SL
RN to Q	t_R	0.145	0.073 + 0.036*SL	0.063 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.124	0.060 + 0.032*SL	0.055 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.345	0.307 + 0.019*SL	0.314 + 0.017*SL	0.315 + 0.017*SL
	t_{PHL}	0.388	0.347 + 0.020*SL	0.357 + 0.018*SL	0.360 + 0.018*SL
D to QN	t_R	0.148	0.074 + 0.037*SL	0.069 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.120	0.056 + 0.032*SL	0.052 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.476	0.436 + 0.020*SL	0.446 + 0.018*SL	0.452 + 0.017*SL
	t_{PHL}	0.450	0.410 + 0.020*SL	0.419 + 0.018*SL	0.423 + 0.018*SL
G to QN	t_R	0.148	0.074 + 0.037*SL	0.069 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.120	0.055 + 0.032*SL	0.052 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.476	0.436 + 0.020*SL	0.446 + 0.018*SL	0.452 + 0.017*SL
	t_{PHL}	0.471	0.431 + 0.020*SL	0.439 + 0.018*SL	0.443 + 0.018*SL
SN to QN	t_R	0.150	0.076 + 0.037*SL	0.071 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.123	0.060 + 0.032*SL	0.055 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.184	0.144 + 0.020*SL	0.154 + 0.018*SL	0.159 + 0.017*SL
	t_{PHL}	0.213	0.173 + 0.020*SL	0.182 + 0.018*SL	0.186 + 0.018*SL
RN to QN	t_R	0.148	0.074 + 0.037*SL	0.069 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.121	0.057 + 0.032*SL	0.052 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.291	0.251 + 0.020*SL	0.260 + 0.018*SL	0.266 + 0.017*SL
	t_{PHL}	0.248	0.208 + 0.020*SL	0.217 + 0.018*SL	0.221 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD4D2

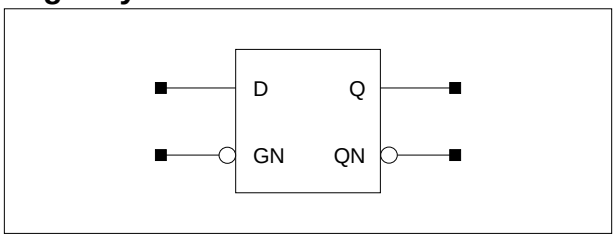
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.107	0.072 + 0.018*SL	0.067 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.095	0.062 + 0.016*SL	0.062 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.582	0.559 + 0.011*SL	0.569 + 0.009*SL	0.576 + 0.009*SL
	t_{PHL}	0.609	0.584 + 0.012*SL	0.597 + 0.009*SL	0.609 + 0.009*SL
G to Q	t_R	0.108	0.072 + 0.018*SL	0.067 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.094	0.062 + 0.016*SL	0.061 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.602	0.579 + 0.011*SL	0.589 + 0.009*SL	0.596 + 0.009*SL
	t_{PHL}	0.609	0.585 + 0.012*SL	0.597 + 0.009*SL	0.609 + 0.009*SL
SN to Q	t_R	0.108	0.073 + 0.018*SL	0.068 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.094	0.061 + 0.017*SL	0.062 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.344	0.321 + 0.011*SL	0.331 + 0.009*SL	0.338 + 0.009*SL
	t_{PHL}	0.316	0.291 + 0.012*SL	0.304 + 0.009*SL	0.316 + 0.009*SL
RN to Q	t_R	0.107	0.072 + 0.018*SL	0.067 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.094	0.060 + 0.017*SL	0.062 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.379	0.357 + 0.011*SL	0.367 + 0.009*SL	0.374 + 0.009*SL
	t_{PHL}	0.423	0.399 + 0.012*SL	0.411 + 0.009*SL	0.423 + 0.009*SL
D to QN	t_R	0.110	0.073 + 0.018*SL	0.070 + 0.019*SL	0.046 + 0.019*SL
	t_F	0.086	0.055 + 0.016*SL	0.051 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.476	0.452 + 0.012*SL	0.464 + 0.009*SL	0.479 + 0.009*SL
	t_{PHL}	0.445	0.421 + 0.012*SL	0.433 + 0.009*SL	0.444 + 0.009*SL
G to QN	t_R	0.110	0.074 + 0.018*SL	0.070 + 0.019*SL	0.046 + 0.019*SL
	t_F	0.086	0.053 + 0.016*SL	0.052 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.476	0.452 + 0.012*SL	0.464 + 0.009*SL	0.479 + 0.009*SL
	t_{PHL}	0.465	0.442 + 0.012*SL	0.453 + 0.009*SL	0.465 + 0.009*SL
SN to QN	t_R	0.111	0.075 + 0.018*SL	0.072 + 0.019*SL	0.046 + 0.019*SL
	t_F	0.089	0.057 + 0.016*SL	0.055 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.183	0.159 + 0.012*SL	0.171 + 0.009*SL	0.185 + 0.009*SL
	t_{PHL}	0.207	0.184 + 0.012*SL	0.195 + 0.009*SL	0.206 + 0.009*SL
RN to QN	t_R	0.110	0.073 + 0.018*SL	0.071 + 0.019*SL	0.046 + 0.019*SL
	t_F	0.086	0.055 + 0.016*SL	0.052 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.290	0.266 + 0.012*SL	0.278 + 0.009*SL	0.293 + 0.009*SL
	t_{PHL}	0.243	0.219 + 0.012*SL	0.231 + 0.009*SL	0.242 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

LD5/LD5D2

D Latch with Active Low, 1X/2X Drive

Logic Symbol



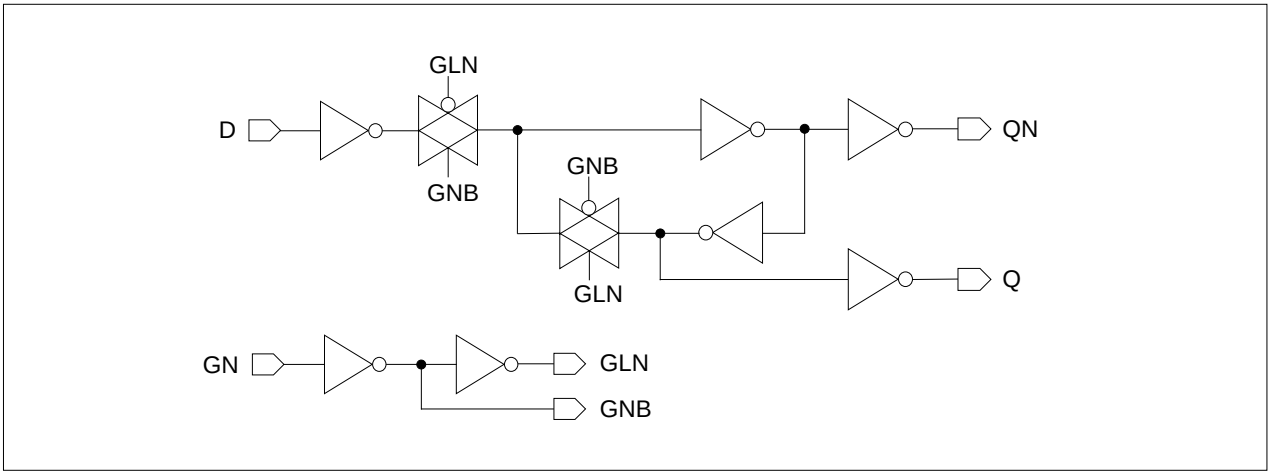
Truth Table

D	GN	Q (n+1)	QN (n+1)
0	0	0	1
1	0	1	0
x	1	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
LD5		*LD5D2*		*LD5*	*LD5D2*
D	GN	D	GN		
0.8	0.8	0.8	0.8	4.00	4.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD5	LD5D2
Pulse Width Low (GN)	t_{PWL}	0.359	0.389
Input Setup Time (D to GN)	t_{SU}	0.562	0.473
Input Hold Time (D to GN)	t_{HD}	0.000	0.000

Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.046 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.394	0.357 + 0.018*SL	0.361 + 0.017*SL	0.362 + 0.017*SL
	t_{PHL}	0.407	0.368 + 0.020*SL	0.375 + 0.018*SL	0.377 + 0.018*SL
GN to Q	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.053 + 0.032*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.447	0.410 + 0.018*SL	0.414 + 0.017*SL	0.414 + 0.017*SL
	t_{PHL}	0.487	0.448 + 0.020*SL	0.455 + 0.018*SL	0.457 + 0.018*SL
D to QN	t_R	0.146	0.073 + 0.036*SL	0.065 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.123	0.059 + 0.032*SL	0.055 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.332	0.293 + 0.019*SL	0.300 + 0.018*SL	0.303 + 0.017*SL
	t_{PHL}	0.315	0.275 + 0.020*SL	0.285 + 0.018*SL	0.289 + 0.018*SL
GN to QN	t_R	0.145	0.073 + 0.036*SL	0.065 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.123	0.059 + 0.032*SL	0.054 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.411	0.373 + 0.019*SL	0.379 + 0.018*SL	0.382 + 0.017*SL
	t_{PHL}	0.368	0.328 + 0.020*SL	0.337 + 0.018*SL	0.342 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

LD5D2

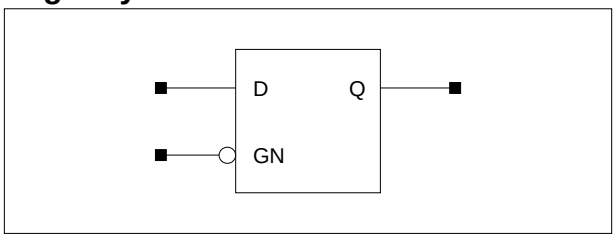
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.102	0.066 + 0.018*SL	0.061 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.087	0.054 + 0.016*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.437	0.416 + 0.011*SL	0.424 + 0.009*SL	0.427 + 0.009*SL
	t_{PHL}	0.449	0.426 + 0.012*SL	0.436 + 0.009*SL	0.445 + 0.009*SL
GN to Q	t_R	0.102	0.068 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.087	0.056 + 0.016*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.490	0.468 + 0.011*SL	0.476 + 0.009*SL	0.480 + 0.009*SL
	t_{PHL}	0.528	0.505 + 0.012*SL	0.516 + 0.009*SL	0.524 + 0.009*SL
D to QN	t_R	0.109	0.074 + 0.018*SL	0.068 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.090	0.057 + 0.017*SL	0.057 + 0.016*SL	0.031 + 0.017*SL
	t_{PLH}	0.336	0.314 + 0.011*SL	0.323 + 0.009*SL	0.332 + 0.009*SL
	t_{PHL}	0.313	0.289 + 0.012*SL	0.301 + 0.009*SL	0.314 + 0.009*SL
GN to QN	t_R	0.109	0.074 + 0.018*SL	0.068 + 0.019*SL	0.040 + 0.019*SL
	t_F	0.090	0.059 + 0.016*SL	0.056 + 0.017*SL	0.031 + 0.017*SL
	t_{PLH}	0.416	0.393 + 0.011*SL	0.403 + 0.009*SL	0.411 + 0.009*SL
	t_{PHL}	0.366	0.342 + 0.012*SL	0.354 + 0.009*SL	0.367 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

LD5Q/LD5QD2

D Latch with Active Low,Q Output Only, 1X/2X Drive

Logic Symbol



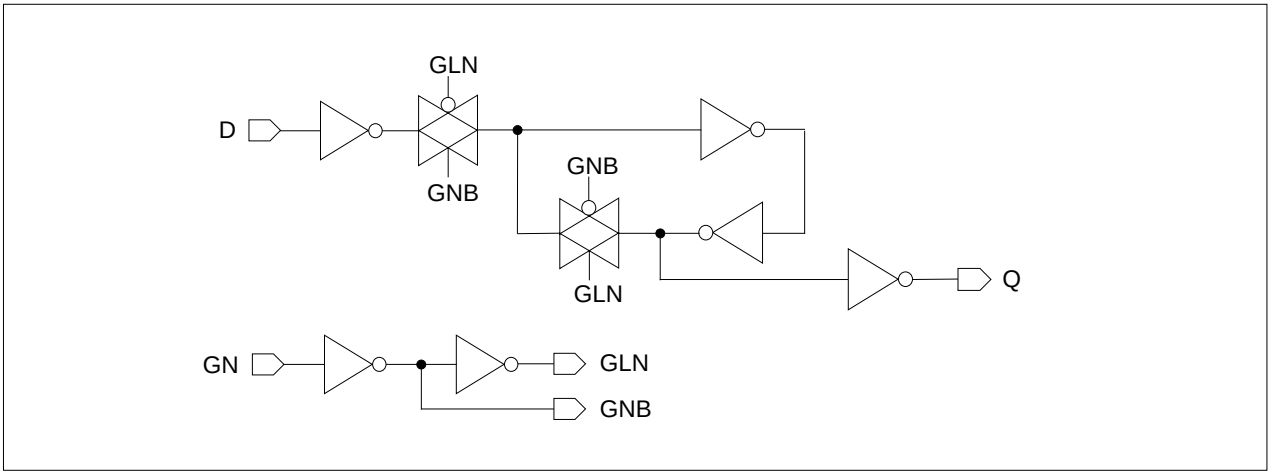
Truth Table

D	GN	Q (n+1)
0	0	0
1	0	1
x	1	Q (n)

Cell Data

Input Load (SL)				Gate Count	
LD5Q		*LD5QD2*		*LD5Q*	*LD5QD2*
D	GN	D	GN		
0.8	0.8	0.8	0.8	3.67	4.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD5Q	LD5QD2
Pulse Width Low (GN)	t_{PWL}	0.341	0.345
Input Setup Time (D to GN)	t_{SU}	0.542	0.548
Input Hold Time (D to GN)	t_{HD}	0.000	0.000

Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD5Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.134	0.062 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.113	0.049 + 0.032*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.355	0.318 + 0.018*SL	0.322 + 0.017*SL	0.322 + 0.017*SL
	t_{PHL}	0.363	0.324 + 0.019*SL	0.331 + 0.018*SL	0.332 + 0.018*SL
GN to Q	t_R	0.134	0.062 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.115	0.052 + 0.032*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.408	0.371 + 0.018*SL	0.375 + 0.017*SL	0.375 + 0.017*SL
	t_{PHL}	0.442	0.403 + 0.019*SL	0.410 + 0.018*SL	0.412 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

LD5QD2

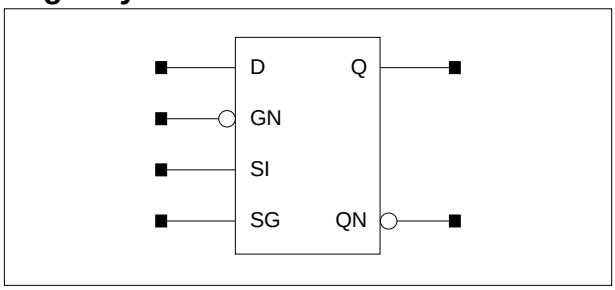
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.099	0.064 + 0.018*SL	0.057 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.081	0.048 + 0.017*SL	0.048 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.361	0.339 + 0.011*SL	0.347 + 0.009*SL	0.351 + 0.009*SL
	t_{PHL}	0.362	0.339 + 0.012*SL	0.350 + 0.009*SL	0.358 + 0.009*SL
GN to Q	t_R	0.098	0.064 + 0.017*SL	0.056 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.081	0.048 + 0.017*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.413	0.392 + 0.011*SL	0.400 + 0.009*SL	0.403 + 0.009*SL
	t_{PHL}	0.442	0.419 + 0.012*SL	0.429 + 0.009*SL	0.437 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

LD5S/LD5SD2

D Latch with Active Low, Scan, 1X/2X Drive

Logic Symbol



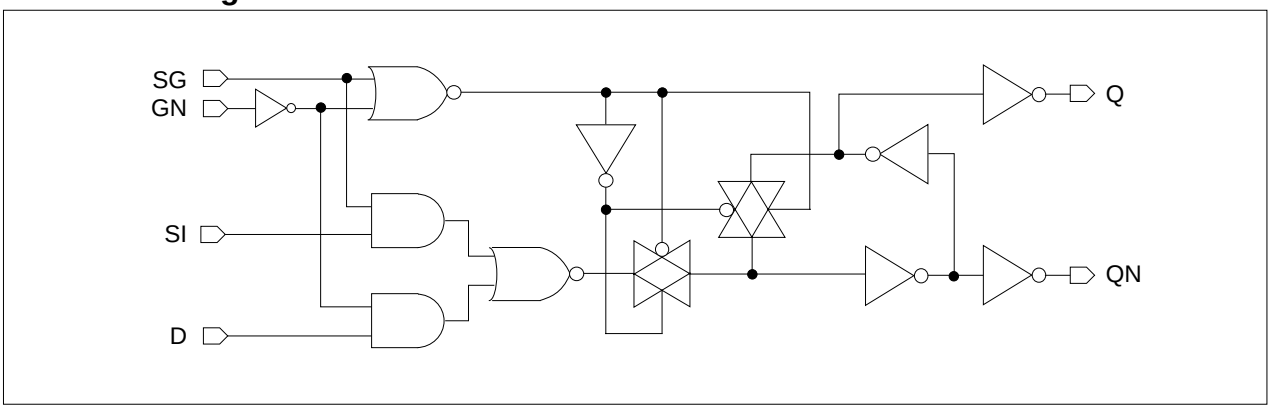
Truth Table

D	GN	SI	SG	Q (n+1)	QN (n+1)
x	1	x	0	Q (n)	QN (n)
x	x	1	1	1	0
x	1	0	1	0	1
1	0	x	x	1	0
0	0	x	0	0	1
0	0	0	1	0	1

Cell Data

Input Load (SL)								Gate Count	
LD5S				*LD5SD2*				*LD5S*	*LD5SD2*
D	GN	SI	SG	D	GN	SI	SG		
0.7	0.8	1.0	2.1	0.7	0.8	1.0	2.1	6.00	6.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD5S	LD5SD2
Pulse Width Low (GN)	t_{PWL}	0.376	0.396
Pulse Width High (SG)	t_{PWH}	0.355	0.377
Input Setup Time (D to GN)	t_{SU}	0.598	0.458
Input Hold Time (D to GN)	t_{HD}	0.006	0.000
Input Setup Time (SI to SG)	t_{SU}	1.041	1.052
Input Hold Time (SI to SG)	t_{HD}	0.588	0.511

Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD5S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.457	0.420 + 0.018*SL	0.424 + 0.017*SL	0.424 + 0.017*SL
	t_{PHL}	0.504	0.465 + 0.019*SL	0.472 + 0.018*SL	0.474 + 0.018*SL
SI to Q	t_R	0.136	0.065 + 0.036*SL	0.055 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.053 + 0.031*SL	0.046 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.540	0.503 + 0.018*SL	0.506 + 0.017*SL	0.507 + 0.017*SL
	t_{PHL}	0.548	0.509 + 0.019*SL	0.516 + 0.018*SL	0.518 + 0.018*SL
GN to Q	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.602	0.566 + 0.018*SL	0.569 + 0.017*SL	0.569 + 0.017*SL
	t_{PHL}	0.579	0.540 + 0.019*SL	0.547 + 0.018*SL	0.549 + 0.018*SL
SG to Q	t_R	0.136	0.064 + 0.036*SL	0.055 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.117	0.055 + 0.031*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.549	0.513 + 0.018*SL	0.517 + 0.017*SL	0.517 + 0.017*SL
	t_{PHL}	0.545	0.506 + 0.019*SL	0.513 + 0.018*SL	0.515 + 0.018*SL
D to QN	t_R	0.151	0.080 + 0.035*SL	0.070 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.126	0.063 + 0.032*SL	0.057 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.429	0.390 + 0.019*SL	0.398 + 0.017*SL	0.400 + 0.017*SL
	t_{PHL}	0.379	0.339 + 0.020*SL	0.349 + 0.018*SL	0.353 + 0.018*SL
SI to QN	t_R	0.151	0.081 + 0.035*SL	0.070 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.126	0.063 + 0.032*SL	0.058 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.473	0.435 + 0.019*SL	0.442 + 0.017*SL	0.445 + 0.017*SL
	t_{PHL}	0.462	0.421 + 0.020*SL	0.431 + 0.018*SL	0.436 + 0.018*SL
GN to QN	t_R	0.151	0.080 + 0.035*SL	0.069 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.125	0.062 + 0.032*SL	0.056 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.504	0.465 + 0.019*SL	0.473 + 0.017*SL	0.475 + 0.017*SL
	t_{PHL}	0.525	0.484 + 0.020*SL	0.494 + 0.018*SL	0.499 + 0.018*SL
SG to QN	t_R	0.151	0.080 + 0.036*SL	0.070 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.126	0.063 + 0.032*SL	0.058 + 0.033*SL	0.037 + 0.034*SL
	t_{PLH}	0.470	0.431 + 0.019*SL	0.439 + 0.017*SL	0.442 + 0.017*SL
	t_{PHL}	0.472	0.431 + 0.020*SL	0.441 + 0.018*SL	0.446 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

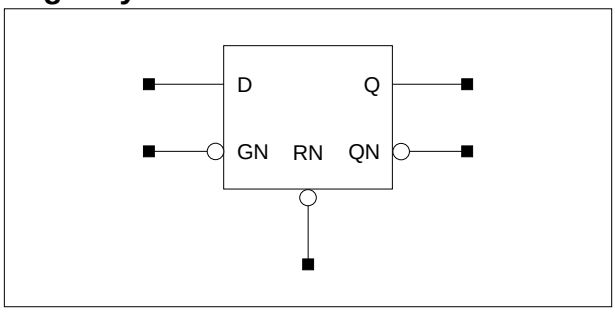
(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD5SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.102	0.067 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.087	0.055 + 0.016*SL	0.053 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.503	0.481 + 0.011*SL	0.489 + 0.009*SL	0.492 + 0.009*SL
	t_{PHL}	0.551	0.528 + 0.012*SL	0.538 + 0.009*SL	0.546 + 0.009*SL
SI to Q	t_R	0.102	0.068 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.087	0.053 + 0.017*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.586	0.564 + 0.011*SL	0.572 + 0.009*SL	0.576 + 0.009*SL
	t_{PHL}	0.595	0.572 + 0.012*SL	0.583 + 0.009*SL	0.590 + 0.009*SL
GN to Q	t_R	0.101	0.066 + 0.018*SL	0.060 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.088	0.056 + 0.016*SL	0.053 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.654	0.633 + 0.011*SL	0.641 + 0.009*SL	0.644 + 0.009*SL
	t_{PHL}	0.626	0.603 + 0.012*SL	0.613 + 0.009*SL	0.621 + 0.009*SL
SG to Q	t_R	0.102	0.068 + 0.017*SL	0.060 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.087	0.055 + 0.016*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.596	0.574 + 0.011*SL	0.582 + 0.009*SL	0.586 + 0.009*SL
	t_{PHL}	0.592	0.568 + 0.012*SL	0.579 + 0.009*SL	0.587 + 0.009*SL
D to QN	t_R	0.115	0.080 + 0.017*SL	0.074 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.094	0.062 + 0.016*SL	0.061 + 0.016*SL	0.031 + 0.017*SL
	t_{PLH}	0.438	0.415 + 0.012*SL	0.425 + 0.009*SL	0.434 + 0.009*SL
	t_{PHL}	0.380	0.355 + 0.012*SL	0.368 + 0.009*SL	0.381 + 0.009*SL
SI to QN	t_R	0.116	0.081 + 0.017*SL	0.075 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.095	0.063 + 0.016*SL	0.061 + 0.016*SL	0.031 + 0.017*SL
	t_{PLH}	0.482	0.459 + 0.011*SL	0.470 + 0.009*SL	0.478 + 0.009*SL
	t_{PHL}	0.463	0.438 + 0.012*SL	0.451 + 0.009*SL	0.464 + 0.009*SL
GN to QN	t_R	0.115	0.080 + 0.018*SL	0.074 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.094	0.061 + 0.016*SL	0.060 + 0.016*SL	0.031 + 0.017*SL
	t_{PLH}	0.513	0.489 + 0.012*SL	0.500 + 0.009*SL	0.509 + 0.009*SL
	t_{PHL}	0.531	0.507 + 0.012*SL	0.519 + 0.009*SL	0.532 + 0.009*SL
SG to QN	t_R	0.116	0.081 + 0.017*SL	0.075 + 0.019*SL	0.041 + 0.019*SL
	t_F	0.095	0.062 + 0.016*SL	0.061 + 0.016*SL	0.031 + 0.017*SL
	t_{PLH}	0.479	0.456 + 0.011*SL	0.466 + 0.009*SL	0.475 + 0.009*SL
	t_{PHL}	0.473	0.448 + 0.012*SL	0.461 + 0.009*SL	0.474 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



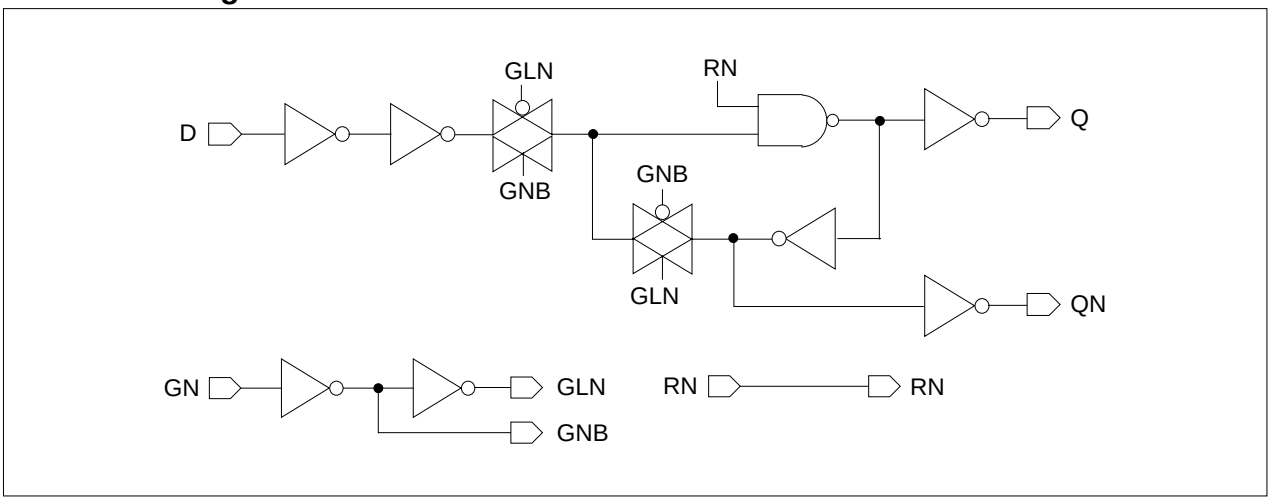
Truth Table

D	GN	RN	Q (n+1)	QN (n+1)
0	0	1	0	1
1	0	1	1	0
x	1	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
LD6			*LD6D2*			*LD6*	*LD6D2*
D	GN	RN	D	GN	RN		
0.8	0.8	1.1	0.8	0.8	1.1	4.67	5.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD6	LD6D2
Pulse Width Low (GN)	t_{PWL}	0.353	0.383
Pulse Width Low (RN)	t_{PWL}	0.350	0.372
Input Setup Time (D to GN)	t_{SU}	0.665	0.672
Input Hold Time (D to GN)	t_{HD}	0.068	0.046
Recovery Time (RN)	t_{RC}	0.000	0.068
Removal Time (RN)	t_{RM}	0.424	0.337

Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.151	0.078 + 0.037*SL	0.073 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.121	0.056 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.381	0.340 + 0.020*SL	0.351 + 0.018*SL	0.357 + 0.017*SL
	t_{PHL}	0.391	0.351 + 0.020*SL	0.360 + 0.018*SL	0.365 + 0.018*SL
GN to Q	t_R	0.151	0.077 + 0.037*SL	0.072 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.121	0.057 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.416	0.376 + 0.020*SL	0.386 + 0.018*SL	0.392 + 0.017*SL
	t_{PHL}	0.365	0.324 + 0.020*SL	0.334 + 0.018*SL	0.338 + 0.018*SL
RN to Q	t_R	0.150	0.077 + 0.037*SL	0.072 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.123	0.059 + 0.032*SL	0.055 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.183	0.143 + 0.020*SL	0.153 + 0.018*SL	0.159 + 0.017*SL
	t_{PHL}	0.212	0.172 + 0.020*SL	0.181 + 0.018*SL	0.185 + 0.018*SL
D to QN	t_R	0.135	0.063 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.117	0.054 + 0.032*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.466	0.429 + 0.018*SL	0.433 + 0.017*SL	0.433 + 0.017*SL
	t_{PHL}	0.453	0.414 + 0.019*SL	0.421 + 0.018*SL	0.423 + 0.018*SL
GN to QN	t_R	0.135	0.063 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.116	0.052 + 0.032*SL	0.046 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.439	0.402 + 0.018*SL	0.406 + 0.017*SL	0.406 + 0.017*SL
	t_{PHL}	0.488	0.450 + 0.019*SL	0.456 + 0.018*SL	0.458 + 0.018*SL
RN to QN	t_R	0.135	0.063 + 0.036*SL	0.054 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.047 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.287	0.251 + 0.018*SL	0.254 + 0.017*SL	0.254 + 0.017*SL
	t_{PHL}	0.256	0.217 + 0.019*SL	0.224 + 0.018*SL	0.226 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26ns, SL: Standard Load)

LD6D2

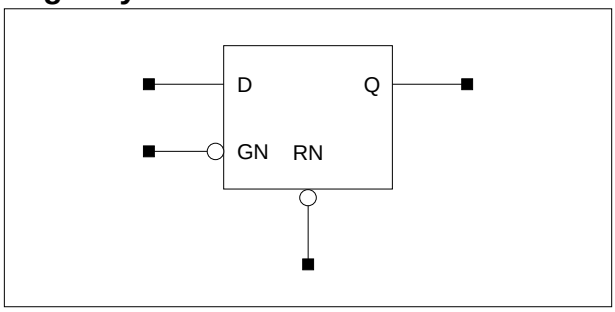
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.113	0.075 + 0.019*SL	0.075 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.088	0.055 + 0.016*SL	0.054 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.387	0.363 + 0.012*SL	0.375 + 0.009*SL	0.393 + 0.009*SL
	t_{PHL}	0.390	0.366 + 0.012*SL	0.378 + 0.009*SL	0.391 + 0.009*SL
GN to Q	t_R	0.113	0.075 + 0.019*SL	0.074 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.089	0.057 + 0.016*SL	0.054 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.423	0.399 + 0.012*SL	0.411 + 0.009*SL	0.429 + 0.009*SL
	t_{PHL}	0.363	0.339 + 0.012*SL	0.351 + 0.009*SL	0.364 + 0.009*SL
RN to Q	t_R	0.112	0.075 + 0.019*SL	0.074 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.090	0.058 + 0.016*SL	0.056 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.187	0.163 + 0.012*SL	0.175 + 0.009*SL	0.192 + 0.009*SL
	t_{PHL}	0.210	0.186 + 0.012*SL	0.198 + 0.009*SL	0.210 + 0.009*SL
D to QN	t_R	0.094	0.060 + 0.017*SL	0.051 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.084	0.053 + 0.015*SL	0.048 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.483	0.463 + 0.010*SL	0.469 + 0.009*SL	0.471 + 0.009*SL
	t_{PHL}	0.487	0.464 + 0.012*SL	0.474 + 0.009*SL	0.481 + 0.009*SL
GN to QN	t_R	0.094	0.060 + 0.017*SL	0.051 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.082	0.049 + 0.017*SL	0.049 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.457	0.436 + 0.010*SL	0.442 + 0.009*SL	0.444 + 0.009*SL
	t_{PHL}	0.523	0.500 + 0.011*SL	0.510 + 0.009*SL	0.517 + 0.009*SL
RN to QN	t_R	0.094	0.060 + 0.017*SL	0.051 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.082	0.049 + 0.016*SL	0.049 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.303	0.282 + 0.010*SL	0.289 + 0.009*SL	0.291 + 0.009*SL
	t_{PHL}	0.287	0.264 + 0.011*SL	0.274 + 0.009*SL	0.281 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

LD6Q/LD6QD2

D Latch with Active Low, Reset, Q Output Only, 1X/2X Drive

Logic Symbol



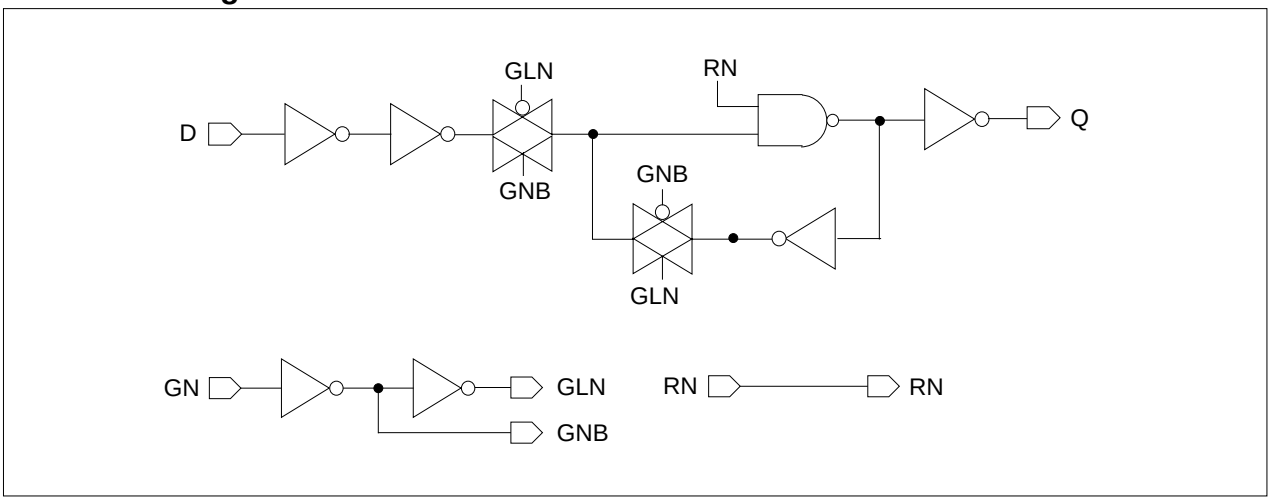
Truth Table

D	GN	RN	Q (n+1)
0	0	1	0
1	0	1	1
x	1	1	Q (n)
x	x	0	0

Cell Data

Input Load (SL)						Gate Count	
LD6Q			*LD6QD2*			*LD6Q*	*LD6QD2*
D	GN	RN	D	GN	RN		
0.8	0.8	1.1	0.8	0.8	1.1	4.33	4.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD6Q	LD6QD2
Pulse Width Low (GN)	t_{PWL}	0.346	0.366
Pulse Width Low (RN)	t_{PWL}	0.329	0.345
Input Setup Time (D to GN)	t_{SU}	0.660	0.671
Input Hold Time (D to GN)	t_{HD}	0.075	0.057
Recovery Time (RN)	t_{RC}	0.000	0.020
Removal Time (RN)	t_{RM}	0.456	0.382

Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD6Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.153	0.081 + 0.036*SL	0.074 + 0.038*SL	0.051 + 0.038*SL
	t_F	0.122	0.059 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.384	0.343 + 0.020*SL	0.355 + 0.017*SL	0.359 + 0.017*SL
	t_{PHL}	0.393	0.353 + 0.020*SL	0.362 + 0.018*SL	0.366 + 0.018*SL
GN to Q	t_R	0.152	0.080 + 0.036*SL	0.074 + 0.038*SL	0.051 + 0.038*SL
	t_F	0.122	0.059 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.419	0.378 + 0.020*SL	0.390 + 0.017*SL	0.395 + 0.017*SL
	t_{PHL}	0.366	0.326 + 0.020*SL	0.336 + 0.018*SL	0.339 + 0.018*SL
RN to Q	t_R	0.152	0.080 + 0.036*SL	0.073 + 0.038*SL	0.050 + 0.038*SL
	t_F	0.125	0.062 + 0.031*SL	0.055 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.186	0.145 + 0.020*SL	0.157 + 0.017*SL	0.161 + 0.017*SL
	t_{PHL}	0.213	0.173 + 0.020*SL	0.182 + 0.018*SL	0.185 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

LD6QD2

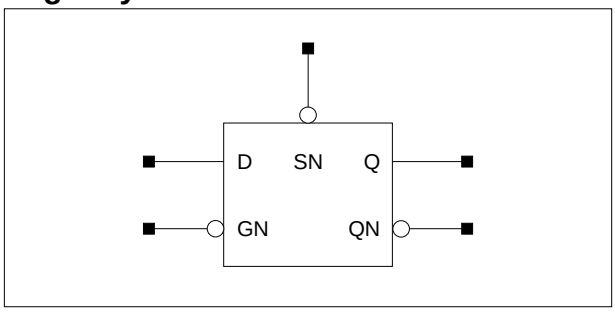
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.118	0.080 + 0.019*SL	0.080 + 0.019*SL	0.046 + 0.019*SL
	t_F	0.091	0.059 + 0.016*SL	0.058 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.393	0.368 + 0.012*SL	0.382 + 0.009*SL	0.398 + 0.009*SL
	t_{PHL}	0.394	0.370 + 0.012*SL	0.382 + 0.009*SL	0.394 + 0.009*SL
GN to Q	t_R	0.119	0.083 + 0.018*SL	0.080 + 0.019*SL	0.046 + 0.019*SL
	t_F	0.091	0.059 + 0.016*SL	0.058 + 0.016*SL	0.030 + 0.017*SL
	t_{PLH}	0.428	0.404 + 0.012*SL	0.417 + 0.009*SL	0.433 + 0.009*SL
	t_{PHL}	0.367	0.343 + 0.012*SL	0.355 + 0.009*SL	0.367 + 0.009*SL
RN to Q	t_R	0.117	0.081 + 0.018*SL	0.079 + 0.019*SL	0.046 + 0.019*SL
	t_F	0.093	0.059 + 0.017*SL	0.060 + 0.016*SL	0.030 + 0.017*SL
	t_{PLH}	0.192	0.167 + 0.012*SL	0.181 + 0.009*SL	0.196 + 0.009*SL
	t_{PHL}	0.213	0.189 + 0.012*SL	0.201 + 0.009*SL	0.212 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

LD7/LD7D2

D Latch with Active Low, Set, 1X/2X Drive

Logic Symbol



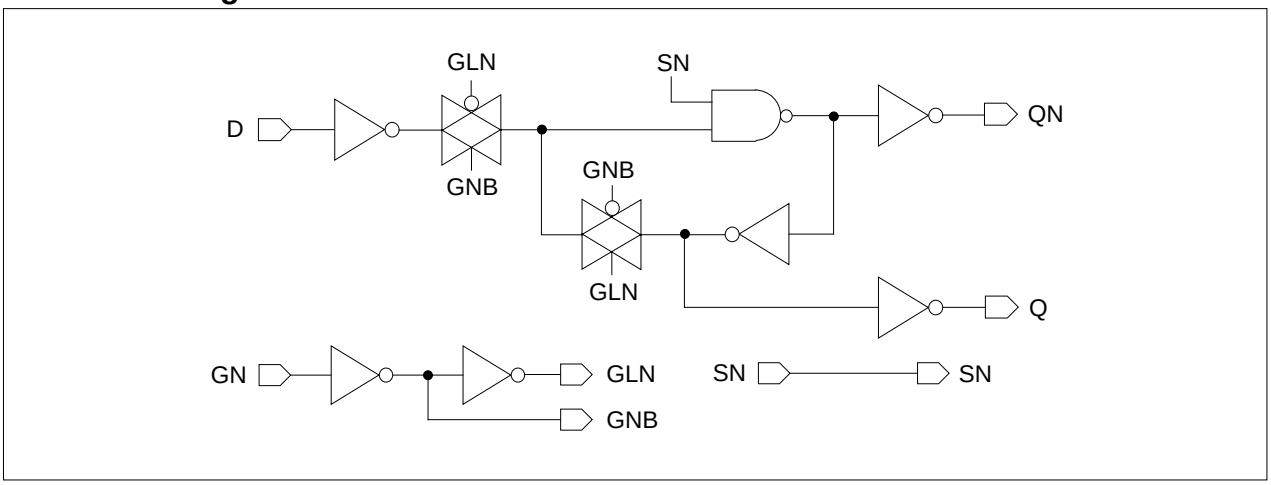
Truth Table

D	GN	SN	Q (n+1)	QN (n+1)
0	0	1	0	1
1	0	1	1	0
x	1	1	Q (n)	QN (n)
x	x	0	1	0

Cell Data

Input Load (SL)						Gate Count	
LD7			*LD7D2*			*LD7*	*LD7D2*
D	GN	SN	D	GN	SN		
0.8	0.8	1.1	0.8	0.8	1.1	4.33	5.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD7	LD7D2
Pulse Width Low (GN)	t_{PWL}	0.353	0.383
Pulse Width Low (SN)	t_{PWL}	0.350	0.372
Input Setup Time (D to GN)	t_{SU}	0.577	0.474
Input Hold Time (D to GN)	t_{HD}	0.000	0.000
Recovery Time (SN)	t_{RC}	0.000	0.070
Removal Time (SN)	t_{RM}	0.422	0.330

Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.135	0.063 + 0.036*SL	0.054 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.117	0.054 + 0.032*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.394	0.358 + 0.018*SL	0.361 + 0.017*SL	0.361 + 0.017*SL
	t_{PHL}	0.413	0.374 + 0.019*SL	0.381 + 0.018*SL	0.383 + 0.018*SL
GN to Q	t_R	0.135	0.063 + 0.036*SL	0.053 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.116	0.052 + 0.032*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.438	0.402 + 0.018*SL	0.405 + 0.017*SL	0.405 + 0.017*SL
	t_{PHL}	0.487	0.448 + 0.019*SL	0.455 + 0.018*SL	0.457 + 0.018*SL
SN to Q	t_R	0.135	0.063 + 0.036*SL	0.054 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.047 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.287	0.251 + 0.018*SL	0.254 + 0.017*SL	0.254 + 0.017*SL
	t_{PHL}	0.256	0.217 + 0.019*SL	0.224 + 0.018*SL	0.226 + 0.018*SL
D to QN	t_R	0.151	0.078 + 0.037*SL	0.072 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.121	0.057 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.341	0.300 + 0.020*SL	0.311 + 0.018*SL	0.317 + 0.017*SL
	t_{PHL}	0.320	0.280 + 0.020*SL	0.289 + 0.018*SL	0.293 + 0.018*SL
GN to QN	t_R	0.151	0.078 + 0.037*SL	0.072 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.121	0.056 + 0.032*SL	0.053 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.415	0.374 + 0.020*SL	0.385 + 0.018*SL	0.391 + 0.017*SL
	t_{PHL}	0.364	0.324 + 0.020*SL	0.333 + 0.018*SL	0.337 + 0.018*SL
SN to QN	t_R	0.150	0.077 + 0.037*SL	0.072 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.123	0.059 + 0.032*SL	0.055 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.183	0.143 + 0.020*SL	0.153 + 0.018*SL	0.159 + 0.017*SL
	t_{PHL}	0.212	0.172 + 0.020*SL	0.181 + 0.018*SL	0.185 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

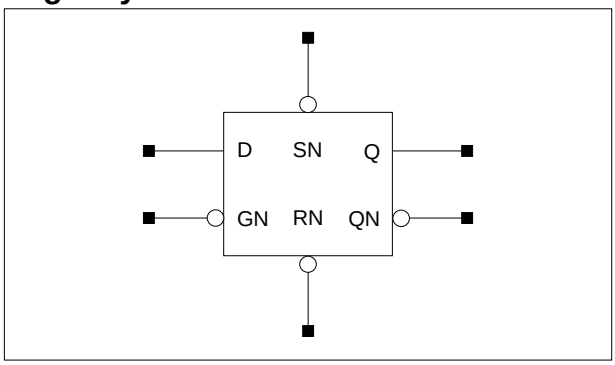
(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD7D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.094	0.060 + 0.017*SL	0.051 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.083	0.051 + 0.016*SL	0.049 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.412	0.391 + 0.010*SL	0.398 + 0.009*SL	0.399 + 0.009*SL
	t_{PHL}	0.447	0.424 + 0.011*SL	0.434 + 0.009*SL	0.441 + 0.009*SL
GN to Q	t_R	0.094	0.059 + 0.017*SL	0.051 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.084	0.052 + 0.016*SL	0.049 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.456	0.435 + 0.010*SL	0.441 + 0.009*SL	0.444 + 0.009*SL
	t_{PHL}	0.522	0.499 + 0.011*SL	0.509 + 0.009*SL	0.516 + 0.009*SL
SN to Q	t_R	0.094	0.060 + 0.017*SL	0.051 + 0.019*SL	0.033 + 0.020*SL
	t_F	0.082	0.049 + 0.016*SL	0.049 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.303	0.282 + 0.010*SL	0.289 + 0.009*SL	0.291 + 0.009*SL
	t_{PHL}	0.287	0.264 + 0.011*SL	0.274 + 0.009*SL	0.281 + 0.009*SL
D to QN	t_R	0.114	0.077 + 0.019*SL	0.076 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.089	0.057 + 0.016*SL	0.054 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.347	0.323 + 0.012*SL	0.335 + 0.009*SL	0.353 + 0.009*SL
	t_{PHL}	0.319	0.294 + 0.012*SL	0.307 + 0.009*SL	0.319 + 0.009*SL
GN to QN	t_R	0.113	0.076 + 0.019*SL	0.074 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.088	0.054 + 0.017*SL	0.055 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.422	0.397 + 0.012*SL	0.410 + 0.009*SL	0.427 + 0.009*SL
	t_{PHL}	0.363	0.338 + 0.012*SL	0.351 + 0.009*SL	0.363 + 0.009*SL
SN to QN	t_R	0.112	0.075 + 0.019*SL	0.074 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.090	0.058 + 0.016*SL	0.056 + 0.016*SL	0.029 + 0.017*SL
	t_{PLH}	0.187	0.163 + 0.012*SL	0.175 + 0.009*SL	0.192 + 0.009*SL
	t_{PHL}	0.210	0.186 + 0.012*SL	0.198 + 0.009*SL	0.210 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



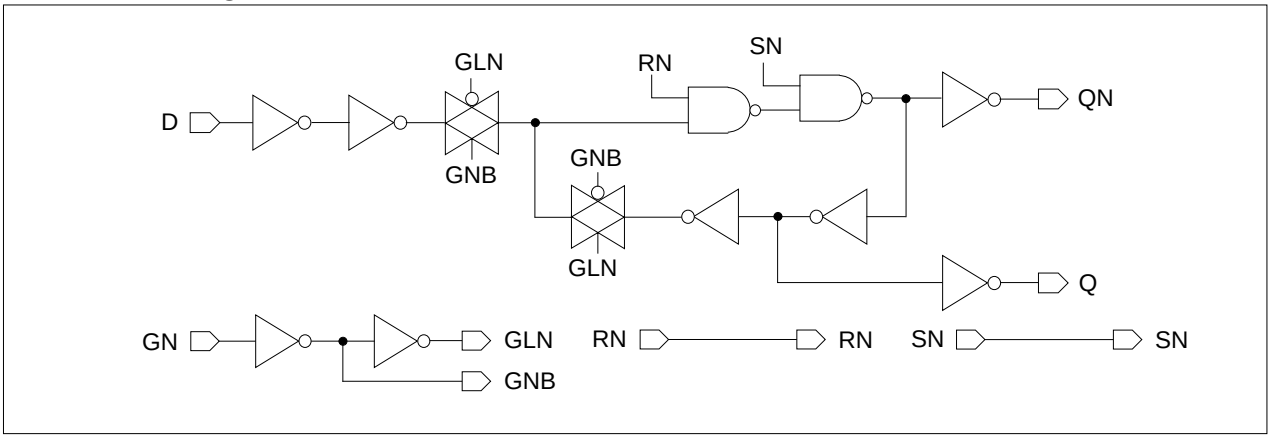
Truth Table

D	GN	RN	SN	Q (n+1)	QN (n+1)
0	0	1	1	0	1
1	0	1	1	1	0
x	1	1	1	Q (n)	QN (n)
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0

Cell Data

Input Load (SL)								Gate Count	
LD8				*LD8D2*				*LD8*	*LD8D2*
D	GN	RN	SN	D	GN	RN	SN		
0.8	0.8	1.1	1.1	0.8	0.8	1.1	1.1	6.00	6.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD8	LD8D2
Pulse Width Low (GN)	t_{PWL}	0.407	0.435
Pulse Width Low (RN)	t_{PWL}	0.384	0.428
Pulse Width Low (SN)	t_{PWL}	0.478	0.488
Input Setup Time (D to GN)	t_{SU}	0.671	0.400
Input Hold Time (D to GN)	t_{HD}	0.022	0.000
Recovery Time (RN)	t_{RC}	0.084	0.119
Removal Time(RN)	t_{RM}	0.315	0.281
Recovery Time (SN)	t_{RC}	0.000	0.008
Removal Time(SN)	t_{RM}	0.479	0.392

Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.139	0.067 + 0.036*SL	0.058 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.120	0.057 + 0.032*SL	0.052 + 0.033*SL	0.035 + 0.034*SL
	t_{PLH}	0.534	0.497 + 0.019*SL	0.502 + 0.017*SL	0.502 + 0.017*SL
	t_{PHL}	0.558	0.518 + 0.020*SL	0.527 + 0.018*SL	0.529 + 0.018*SL
GN to Q	t_R	0.140	0.069 + 0.036*SL	0.059 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.121	0.057 + 0.032*SL	0.052 + 0.033*SL	0.035 + 0.034*SL
	t_{PLH}	0.570	0.532 + 0.019*SL	0.537 + 0.017*SL	0.538 + 0.017*SL
	t_{PHL}	0.533	0.493 + 0.020*SL	0.501 + 0.018*SL	0.503 + 0.018*SL
SN to Q	t_R	0.140	0.067 + 0.036*SL	0.059 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.121	0.057 + 0.032*SL	0.052 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.301	0.264 + 0.019*SL	0.269 + 0.017*SL	0.270 + 0.017*SL
	t_{PHL}	0.270	0.230 + 0.020*SL	0.239 + 0.018*SL	0.241 + 0.018*SL
RN to Q	t_R	0.140	0.069 + 0.036*SL	0.059 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.121	0.057 + 0.032*SL	0.052 + 0.033*SL	0.035 + 0.034*SL
	t_{PLH}	0.335	0.298 + 0.019*SL	0.303 + 0.017*SL	0.304 + 0.017*SL
	t_{PHL}	0.377	0.337 + 0.020*SL	0.346 + 0.018*SL	0.348 + 0.018*SL
D to QN	t_R	0.148	0.074 + 0.037*SL	0.069 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.120	0.055 + 0.032*SL	0.051 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.472	0.432 + 0.020*SL	0.442 + 0.018*SL	0.448 + 0.017*SL
	t_{PHL}	0.447	0.407 + 0.020*SL	0.416 + 0.018*SL	0.420 + 0.018*SL
GN to QN	t_R	0.148	0.074 + 0.037*SL	0.069 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.120	0.057 + 0.032*SL	0.051 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.446	0.406 + 0.020*SL	0.416 + 0.018*SL	0.422 + 0.017*SL
	t_{PHL}	0.482	0.442 + 0.020*SL	0.451 + 0.018*SL	0.455 + 0.018*SL
SN to QN	t_R	0.150	0.077 + 0.037*SL	0.071 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.123	0.060 + 0.032*SL	0.054 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.184	0.144 + 0.020*SL	0.154 + 0.018*SL	0.159 + 0.017*SL
	t_{PHL}	0.213	0.173 + 0.020*SL	0.182 + 0.018*SL	0.186 + 0.018*SL
RN to QN	t_R	0.148	0.074 + 0.037*SL	0.069 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.121	0.057 + 0.032*SL	0.052 + 0.033*SL	0.036 + 0.034*SL
	t_{PLH}	0.291	0.251 + 0.020*SL	0.260 + 0.018*SL	0.266 + 0.017*SL
	t_{PHL}	0.248	0.208 + 0.020*SL	0.217 + 0.018*SL	0.221 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LD8D2

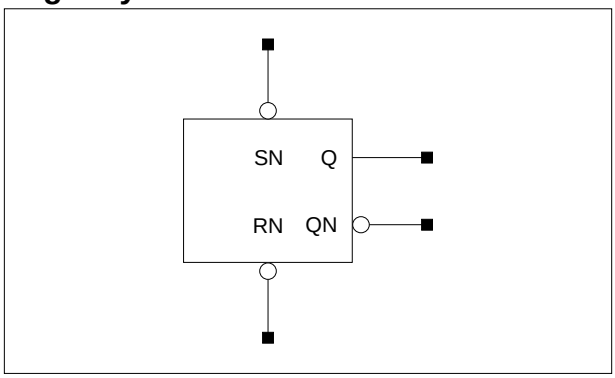
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.096	0.061 + 0.018*SL	0.054 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.086	0.054 + 0.016*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.550	0.528 + 0.011*SL	0.536 + 0.009*SL	0.539 + 0.009*SL
	t_{PHL}	0.586	0.563 + 0.012*SL	0.574 + 0.009*SL	0.581 + 0.009*SL
GN to Q	t_R	0.096	0.059 + 0.018*SL	0.055 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.086	0.054 + 0.016*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.585	0.564 + 0.011*SL	0.571 + 0.009*SL	0.574 + 0.009*SL
	t_{PHL}	0.561	0.537 + 0.012*SL	0.548 + 0.009*SL	0.556 + 0.009*SL
SN to Q	t_R	0.096	0.061 + 0.018*SL	0.055 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.086	0.054 + 0.016*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.315	0.294 + 0.011*SL	0.301 + 0.009*SL	0.304 + 0.009*SL
	t_{PHL}	0.297	0.274 + 0.012*SL	0.285 + 0.009*SL	0.293 + 0.009*SL
RN to Q	t_R	0.096	0.061 + 0.018*SL	0.055 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.086	0.054 + 0.016*SL	0.051 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.351	0.329 + 0.011*SL	0.337 + 0.009*SL	0.340 + 0.009*SL
	t_{PHL}	0.404	0.381 + 0.012*SL	0.392 + 0.009*SL	0.399 + 0.009*SL
D to QN	t_R	0.112	0.074 + 0.019*SL	0.074 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.088	0.057 + 0.016*SL	0.054 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.478	0.454 + 0.012*SL	0.466 + 0.009*SL	0.484 + 0.009*SL
	t_{PHL}	0.447	0.423 + 0.012*SL	0.435 + 0.009*SL	0.448 + 0.009*SL
GN to QN	t_R	0.112	0.074 + 0.019*SL	0.073 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.088	0.055 + 0.017*SL	0.056 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.453	0.429 + 0.012*SL	0.441 + 0.009*SL	0.458 + 0.009*SL
	t_{PHL}	0.483	0.458 + 0.012*SL	0.471 + 0.009*SL	0.483 + 0.009*SL
SN to QN	t_R	0.115	0.078 + 0.018*SL	0.075 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.091	0.059 + 0.016*SL	0.058 + 0.016*SL	0.030 + 0.017*SL
	t_{PLH}	0.189	0.165 + 0.012*SL	0.178 + 0.009*SL	0.194 + 0.009*SL
	t_{PHL}	0.213	0.188 + 0.012*SL	0.201 + 0.009*SL	0.213 + 0.009*SL
RN to QN	t_R	0.112	0.074 + 0.019*SL	0.074 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.089	0.056 + 0.016*SL	0.055 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.296	0.272 + 0.012*SL	0.284 + 0.009*SL	0.302 + 0.009*SL
	t_{PHL}	0.248	0.224 + 0.012*SL	0.236 + 0.009*SL	0.249 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

LS0/LS0D2

SR Latch with 1X/2X Drive

Logic Symbol



Truth Table

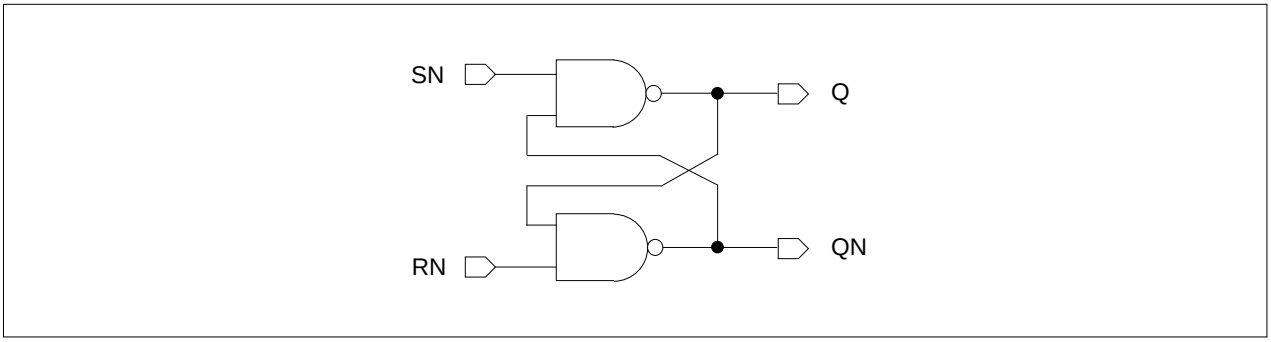
RN	SN	Q (n+1)	QN (n+1)
0	0	*	*
1	0	1	0
0	1	0	1
1	1	Q (n)	QN (n)

* Both Q and QN outputs will remain high during RN and SN are low. However, if RN and SN go high simultaneously, the output states are unpredictable.

Cell Data

Input Load (SL)				Gate Count	
LS0		*LS0D2*		*LS0*	*LS0D2*
RN	SN	RN	SN		
1.1	1.1	2.2	2.1	1.67	3.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LS0	LS0D2
Pulse Width Low (SN)	t_{PWL}	0.368	0.324
Recovery Time (SN to RN)	t_{RC}	0.437	0.372
Removal Time (SN to RN)	t_{RM}	0.000	0.024
Pulse Width Low (RN)	t_{PWL}	0.357	0.319

Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

LS0

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_R	0.208	0.154 + 0.027*SL	0.157 + 0.027*SL	0.149 + 0.027*SL
	t_F	0.228	0.151 + 0.038*SL	0.133 + 0.043*SL	0.102 + 0.044*SL
	t_{PLH}	0.141	0.104 + 0.019*SL	0.109 + 0.017*SL	0.108 + 0.017*SL
	t_{PHL}	0.132	0.087 + 0.022*SL	0.093 + 0.021*SL	0.091 + 0.021*SL
RN to Q	t_F	0.199	0.115 + 0.042*SL	0.109 + 0.044*SL	0.103 + 0.044*SL
	t_{PHL}	0.236	0.192 + 0.022*SL	0.196 + 0.021*SL	0.200 + 0.021*SL
SN to QN	t_F	0.211	0.127 + 0.042*SL	0.121 + 0.044*SL	0.113 + 0.044*SL
	t_{PHL}	0.225	0.181 + 0.022*SL	0.185 + 0.021*SL	0.187 + 0.021*SL
RN to QN	t_R	0.222	0.172 + 0.025*SL	0.168 + 0.026*SL	0.155 + 0.026*SL
	t_F	0.227	0.148 + 0.040*SL	0.133 + 0.043*SL	0.113 + 0.044*SL
	t_{PLH}	0.153	0.118 + 0.018*SL	0.119 + 0.017*SL	0.126 + 0.017*SL
	t_{PHL}	0.124	0.080 + 0.022*SL	0.085 + 0.021*SL	0.085 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

LS0D2

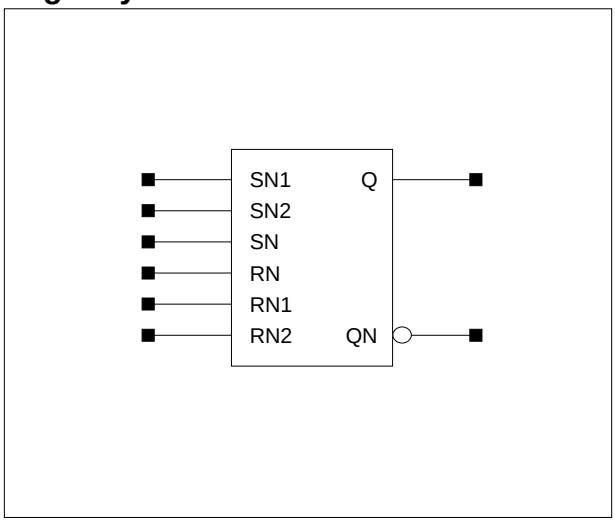
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_R	0.174	0.145 + 0.014*SL	0.150 + 0.013*SL	0.138 + 0.013*SL
	t_F	0.185	0.147 + 0.019*SL	0.134 + 0.022*SL	0.095 + 0.023*SL
	t_{PLH}	0.117	0.096 + 0.011*SL	0.103 + 0.009*SL	0.104 + 0.009*SL
	t_{PHL}	0.105	0.079 + 0.013*SL	0.087 + 0.011*SL	0.087 + 0.011*SL
RN to Q	t_F	0.151	0.108 + 0.021*SL	0.104 + 0.022*SL	0.096 + 0.023*SL
	t_{PHL}	0.210	0.187 + 0.012*SL	0.191 + 0.011*SL	0.197 + 0.011*SL
SN to QN	t_F	0.163	0.121 + 0.021*SL	0.116 + 0.022*SL	0.105 + 0.023*SL
	t_{PHL}	0.192	0.168 + 0.012*SL	0.172 + 0.011*SL	0.176 + 0.011*SL
RN to QN	t_R	0.193	0.168 + 0.013*SL	0.167 + 0.013*SL	0.148 + 0.013*SL
	t_F	0.180	0.140 + 0.020*SL	0.131 + 0.022*SL	0.105 + 0.023*SL
	t_{PLH}	0.132	0.113 + 0.010*SL	0.117 + 0.009*SL	0.125 + 0.009*SL
	t_{PHL}	0.100	0.076 + 0.012*SL	0.081 + 0.011*SL	0.083 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

LS1/LS1D2

SR Latch with Separate Inputs, 1X/2X Drive

Logic Symbol



Truth Table

RN	SN	RN*	SN*	Q (n+1)	QN (n+1)
0	0	x	x	*	*
x	0	0	x	*	*
x	x	0	0	*	*
0	x	x	0	*	*
1	0	1	x	1	0
0	1	x	1	0	1
1	x	1	0	1	0
x	1	0	1	0	1
1	1	1	1	Q (n)	QN (n)

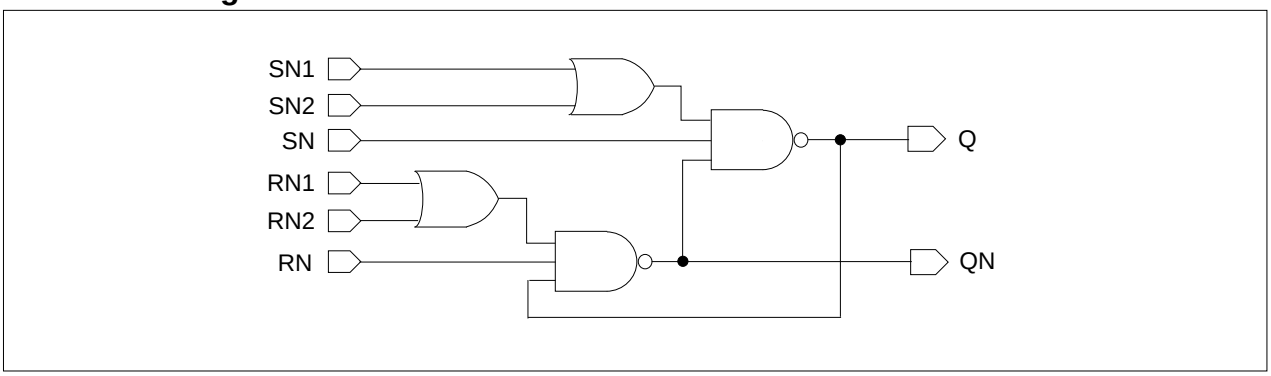
RN* = RN1 + RN2, SN* = SN1 + SN2

* Both Q and QN outputs will remain high during RN (RN*) and SN (SN*) are low. If RN (RN*) and SN (SN*) go high simultaneously, the output states are unpredictable.

Cell Data

Input Load (SL)												Gate Count	
LS1						*LS1D2*						*LS1*	*LS1*D2
RN	RN1	RN2	SN	SN1	SN2	RN	RN1	RN2	SN	SN1	SN2		
1.1	1.0	1.1	1.1	1.0	1.1	0.7	0.6	0.7	0.7	0.6	0.7	3.00	5.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LS1	LS1D2
Pulse Width Low (SN1)	t_{PWL}	0.539	0.485
Removal Time (SN1 to RN1)	t_{RM}	0.031	0.200
Recovery Time (SN1 to RN1)	t_{RC}	0.368	0.197
Removal Time (SN1 to RN2)	t_{RM}	0.125	0.312
Recovery Time (SN1 to RN2)	t_{RC}	0.247	0.085
Removal Time (SN1 to RN)	t_{RM}	0.056	0.239
Recovery Time (SN1 to RN)	t_{RC}	0.330	0.490
Pulse Width Low (SN2)	t_{PWL}	0.548	0.490
Removal Time (SN2 to RN1)	t_{RM}	0.000	0.086
Recovery Time (SN2 to RN1)	t_{RC}	0.479	0.316
Removal Time (SN2 to RN2)	t_{RM}	0.051	0.199
Recovery Time (SN2 to RN2)	t_{RC}	0.344	0.217
Removal Time (SN2 to RN)	t_{RM}	0.000	0.113
Recovery Time (SN2 to RN)	t_{RC}	0.422	0.270
Pulse Width Low (SN)	t_{PWL}	0.425	0.400
Removal Time (SN to RN1)	t_{RM}	0.000	0.113
Recovery Time (SN to RN1)	t_{RC}	0.439	0.286
Removal Time (SN to RN2)	t_{RM}	0.089	0.228
Recovery Time (SN to RN2)	t_{RC}	0.302	0.171
Removal Time (SN to RN)	t_{RM}	0.044	0.199
Recovery Time (SN to RN)	t_{RC}	0.337	0.202
Pulse Width Low (RN1)	t_{PWL}	0.539	0.485
Pulse Width Low (RN2)	t_{PWL}	0.547	0.490
Pulse Width Low (RN)	t_{PWL}	0.425	0.400

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

LS1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN1 to Q	t_R	0.348	0.260 + 0.044*SL	0.266 + 0.043*SL	0.295 + 0.042*SL
	t_F	0.350	0.232 + 0.059*SL	0.219 + 0.062*SL	0.205 + 0.062*SL
	t_{PLH}	0.227	0.162 + 0.033*SL	0.163 + 0.033*SL	0.190 + 0.032*SL
	t_{PHL}	0.189	0.132 + 0.028*SL	0.132 + 0.028*SL	0.132 + 0.028*SL
SN2 to Q	t_R	0.362	0.267 + 0.047*SL	0.284 + 0.043*SL	0.324 + 0.042*SL
	t_F	0.396	0.283 + 0.056*SL	0.266 + 0.061*SL	0.249 + 0.061*SL
	t_{PLH}	0.235	0.169 + 0.033*SL	0.170 + 0.033*SL	0.191 + 0.032*SL
	t_{PHL}	0.216	0.160 + 0.028*SL	0.160 + 0.028*SL	0.161 + 0.028*SL
SN to Q	t_R	0.254	0.199 + 0.028*SL	0.203 + 0.027*SL	0.205 + 0.027*SL
	t_F	0.347	0.228 + 0.059*SL	0.218 + 0.062*SL	0.205 + 0.062*SL
	t_{PLH}	0.168	0.133 + 0.018*SL	0.133 + 0.017*SL	0.136 + 0.017*SL
	t_{PHL}	0.192	0.135 + 0.029*SL	0.135 + 0.028*SL	0.136 + 0.028*SL
RN1 to Q	t_F	0.345	0.224 + 0.061*SL	0.218 + 0.062*SL	0.208 + 0.062*SL
	t_{PHL}	0.353	0.293 + 0.030*SL	0.298 + 0.029*SL	0.304 + 0.028*SL
RN2 to Q	t_F	0.387	0.268 + 0.059*SL	0.262 + 0.061*SL	0.251 + 0.061*SL
	t_{PHL}	0.395	0.336 + 0.029*SL	0.341 + 0.028*SL	0.347 + 0.028*SL
RN to Q	t_F	0.337	0.215 + 0.061*SL	0.210 + 0.062*SL	0.205 + 0.062*SL
	t_{PHL}	0.318	0.260 + 0.029*SL	0.263 + 0.029*SL	0.267 + 0.028*SL
SN1 to QN	t_F	0.344	0.223 + 0.061*SL	0.216 + 0.062*SL	0.206 + 0.062*SL
	t_{PHL}	0.353	0.293 + 0.030*SL	0.299 + 0.029*SL	0.304 + 0.028*SL
SN2 to QN	t_F	0.385	0.267 + 0.059*SL	0.261 + 0.061*SL	0.250 + 0.061*SL
	t_{PHL}	0.395	0.336 + 0.029*SL	0.342 + 0.028*SL	0.348 + 0.028*SL
SN to QN	t_F	0.336	0.214 + 0.061*SL	0.209 + 0.062*SL	0.203 + 0.062*SL
	t_{PHL}	0.318	0.260 + 0.029*SL	0.263 + 0.029*SL	0.267 + 0.028*SL
RN1 to QN	t_R	0.347	0.259 + 0.044*SL	0.265 + 0.043*SL	0.294 + 0.042*SL
	t_F	0.348	0.231 + 0.059*SL	0.217 + 0.062*SL	0.203 + 0.062*SL
	t_{PLH}	0.226	0.161 + 0.033*SL	0.162 + 0.033*SL	0.189 + 0.032*SL
	t_{PHL}	0.188	0.131 + 0.028*SL	0.131 + 0.028*SL	0.132 + 0.028*SL
RN2 to QN	t_R	0.361	0.266 + 0.048*SL	0.284 + 0.043*SL	0.323 + 0.042*SL
	t_F	0.395	0.282 + 0.056*SL	0.265 + 0.061*SL	0.247 + 0.061*SL
	t_{PLH}	0.234	0.167 + 0.033*SL	0.169 + 0.033*SL	0.189 + 0.032*SL
	t_{PHL}	0.215	0.158 + 0.028*SL	0.159 + 0.028*SL	0.160 + 0.028*SL
RN to QN	t_R	0.254	0.198 + 0.028*SL	0.203 + 0.027*SL	0.205 + 0.027*SL
	t_F	0.346	0.227 + 0.059*SL	0.216 + 0.062*SL	0.203 + 0.062*SL
	t_{PLH}	0.167	0.132 + 0.017*SL	0.132 + 0.017*SL	0.135 + 0.017*SL
	t_{PHL}	0.191	0.134 + 0.029*SL	0.134 + 0.028*SL	0.135 + 0.028*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

LS1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN1 to Q	t_R	0.104	0.070 + 0.017*SL	0.062 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.089	0.057 + 0.016*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.400	0.378 + 0.011*SL	0.386 + 0.009*SL	0.388 + 0.009*SL
	t_{PHL}	0.342	0.318 + 0.012*SL	0.329 + 0.009*SL	0.337 + 0.009*SL
SN2 to Q	t_R	0.106	0.072 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.089	0.058 + 0.016*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.404	0.383 + 0.011*SL	0.391 + 0.009*SL	0.393 + 0.009*SL
	t_{PHL}	0.373	0.350 + 0.012*SL	0.361 + 0.009*SL	0.368 + 0.009*SL
SN to Q	t_R	0.100	0.065 + 0.017*SL	0.058 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.088	0.057 + 0.015*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.328	0.306 + 0.011*SL	0.314 + 0.009*SL	0.316 + 0.009*SL
	t_{PHL}	0.346	0.323 + 0.012*SL	0.333 + 0.009*SL	0.341 + 0.009*SL
RN1 to Q	t_F	0.087	0.054 + 0.017*SL	0.055 + 0.017*SL	0.027 + 0.017*SL
	t_{PHL}	0.559	0.536 + 0.012*SL	0.546 + 0.009*SL	0.554 + 0.009*SL
RN2 to Q	t_F	0.089	0.057 + 0.016*SL	0.055 + 0.016*SL	0.027 + 0.017*SL
	t_{PHL}	0.603	0.580 + 0.012*SL	0.591 + 0.009*SL	0.598 + 0.009*SL
RN to Q	t_F	0.089	0.058 + 0.015*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PHL}	0.502	0.478 + 0.012*SL	0.489 + 0.009*SL	0.497 + 0.009*SL
SN1 to QN	t_F	0.087	0.054 + 0.017*SL	0.055 + 0.017*SL	0.027 + 0.017*SL
	t_{PHL}	0.559	0.536 + 0.012*SL	0.546 + 0.009*SL	0.554 + 0.009*SL
SN2 to QN	t_F	0.089	0.058 + 0.016*SL	0.055 + 0.017*SL	0.027 + 0.017*SL
	t_{PHL}	0.603	0.580 + 0.012*SL	0.591 + 0.009*SL	0.598 + 0.009*SL
SN to QN	t_F	0.088	0.058 + 0.015*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PHL}	0.501	0.478 + 0.012*SL	0.489 + 0.009*SL	0.496 + 0.009*SL
RN1 to QN	t_R	0.105	0.070 + 0.017*SL	0.062 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.088	0.057 + 0.016*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.398	0.377 + 0.011*SL	0.385 + 0.009*SL	0.387 + 0.009*SL
	t_{PHL}	0.341	0.317 + 0.012*SL	0.328 + 0.009*SL	0.336 + 0.009*SL
RN2 to QN	t_R	0.106	0.072 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.019*SL
	t_F	0.089	0.058 + 0.016*SL	0.054 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.403	0.381 + 0.011*SL	0.389 + 0.009*SL	0.392 + 0.009*SL
	t_{PHL}	0.372	0.349 + 0.012*SL	0.360 + 0.009*SL	0.367 + 0.009*SL
RN to QN	t_R	0.100	0.065 + 0.017*SL	0.058 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.088	0.057 + 0.016*SL	0.053 + 0.017*SL	0.027 + 0.017*SL
	t_{PLH}	0.327	0.306 + 0.011*SL	0.313 + 0.009*SL	0.316 + 0.009*SL
	t_{PHL}	0.345	0.322 + 0.012*SL	0.332 + 0.009*SL	0.340 + 0.009*SL

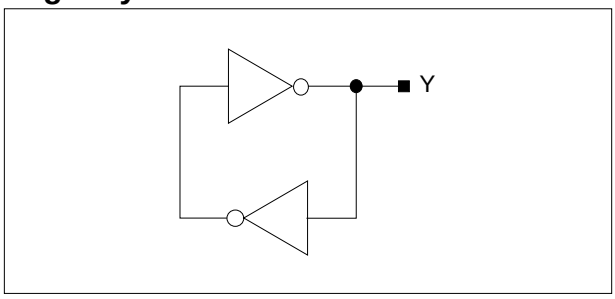
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

BUSHOLDER

Cell List

Cell Name	Function Description
BUSHOLDER	Bus Holder

Logic Symbol



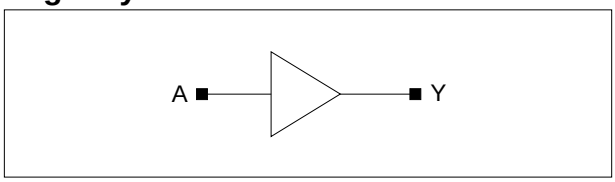
Cell Data

Input Load (SL)	Gate Count
Y	
6.9	1.33

Cell List

Cell Name	Function Description
CK2	Internal Clock Driver CMOS 2mA
CK4	Internal Clock Driver CMOS 4mA
CK6	Internal Clock Driver CMOS 6mA
CK8	Internal Clock Driver CMOS 8mA
CK12	Internal Clock Driver CMOS 12mA
Ck16	Internal Clock Driver CMOS 16mA
CK20	Internal Clock Driver CMOS 20mA

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Standard Load (SL)							I/O Slot						
CK2	*CK4*	*CK6*	*CK8*	*CK12*	*CK16*	*CK20*	*CK2*	*CK4*	*CK6*	*CK8*	*CK12*	*CK16*	*CK20*
A	A	A	A	A	A	A							
2.889	2.889	2.889	2.889	2.889	2.889	2.889	1.0	1.0	1.0	1.0	1.0	1.0	1.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, SL: Standard Load)

CK2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.067	0.058 + 0.005*SL	0.039 + 0.005*SL	0.039 + 0.005*SL
	t_F	0.061	0.051 + 0.005*SL	0.036 + 0.005*SL	0.035 + 0.005*SL
	t_{PLH}	0.198	0.194 + 0.002*SL	0.202 + 0.002*SL	0.202 + 0.002*SL
	t_{PHL}	0.259	0.253 + 0.003*SL	0.265 + 0.003*SL	0.265 + 0.003*SL

*Group1 : SL < 205, *Group2 : 205 ≦ SL ≦ 410, *Group3 : 410 < SL

CK4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.078	0.074 + 0.002*SL	0.046 + 0.002*SL	0.043 + 0.002*SL
	t_F	0.072	0.067 + 0.003*SL	0.042 + 0.003*SL	0.039 + 0.003*SL
	t_{PLH}	0.234	0.231 + 0.001*SL	0.246 + 0.001*SL	0.246 + 0.001*SL
	t_{PHL}	0.300	0.297 + 0.001*SL	0.316 + 0.001*SL	0.316 + 0.001*SL

*Group1 : SL < 405, *Group2 : 405 ≦ SL ≦ 809, *Group3 : 809 < SL

CK6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.095	0.092 + 0.001*SL	0.055 + 0.002*SL	0.048 + 0.002*SL
	t_F	0.091	0.088 + 0.002*SL	0.052 + 0.002*SL	0.045 + 0.002*SL
	t_{PLH}	0.268	0.267 + 0.001*SL	0.290 + 0.001*SL	0.289 + 0.001*SL
	t_{PHL}	0.344	0.342 + 0.001*SL	0.367 + 0.001*SL	0.367 + 0.001*SL

*Group1 : SL < 604, *Group2 : 604 ≦ SL ≦ 1209, *Group3 : 1209 < SL

CK8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.112	0.110 + 0.001*SL	0.067 + 0.001*SL	0.056 + 0.001*SL
	t_F	0.109	0.106 + 0.001*SL	0.064 + 0.001*SL	0.052 + 0.001*SL
	t_{PLH}	0.303	0.302 + 0.001*SL	0.333 + 0.001*SL	0.333 + 0.001*SL
	t_{PHL}	0.388	0.387 + 0.001*SL	0.419 + 0.001*SL	0.418 + 0.001*SL

*Group1 : SL < 802, *Group2 : 802 ≦ SL ≦ 1603, *Group3 : 1603 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, SL: Standard Load)

CK12

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.148	0.147 + 0.001*SL	0.096 + 0.001*SL	0.075 + 0.001*SL
	t_F	0.149	0.147 + 0.001*SL	0.095 + 0.001*SL	0.071 + 0.001*SL
	t_{PLH}	0.371	0.371 + 0.000*SL	0.421 + 0.000*SL	0.420 + 0.000*SL
	t_{PHL}	0.476	0.475 + 0.001*SL	0.523 + 0.000*SL	0.521 + 0.000*SL

*Group1 : SL < 1201, *Group2 : 1201 ≦ SL ≦ 2402, *Group3 : 2402 < SL

CK16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.184	0.183 + 0.001*SL	0.129 + 0.001*SL	0.100 + 0.001*SL
	t_F	0.191	0.189 + 0.001*SL	0.132 + 0.001*SL	0.097 + 0.001*SL
	t_{PLH}	0.440	0.439 + 0.000*SL	0.507 + 0.000*SL	0.507 + 0.000*SL
	t_{PHL}	0.564	0.563 + 0.000*SL	0.628 + 0.000*SL	0.626 + 0.000*SL

*Group1 : SL < 1595, *Group2 : 1595 ≦ SL ≦ 3191, *Group3 : 3191 < SL

CK20

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.222	0.221 + 0.000*SL	0.163 + 0.000*SL	0.130 + 0.000*SL
	t_F	0.231	0.230 + 0.000*SL	0.174 + 0.001*SL	0.128 + 0.001*SL
	t_{PLH}	0.506	0.506 + 0.000*SL	0.592 + 0.000*SL	0.594 + 0.000*SL
	t_{PHL}	0.651	0.650 + 0.000*SL	0.732 + 0.000*SL	0.731 + 0.000*SL

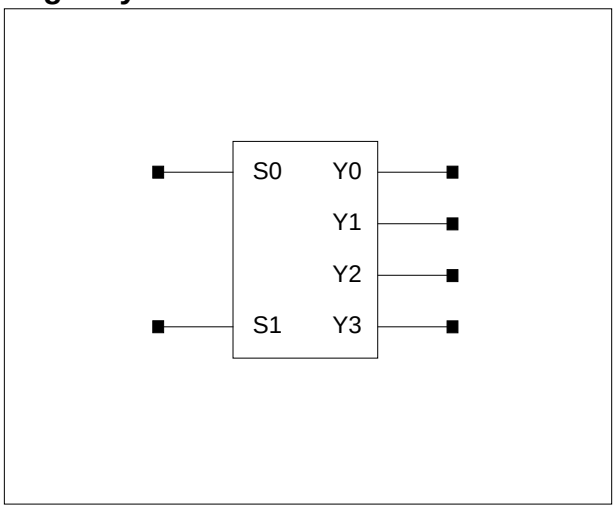
*Group1 : SL < 1990, *Group2 : 1990 ≦ SL ≦ 3980, *Group3 : 3980 < SL

DECODERS

Cell List

Cell Name	Function Description
DC4	2 > 4 Non-Inverting Decoder
DC4I	2 > 4 Inverting Decoder
DC8I	3 > 8 Inverting Decoder

Logic Symbol



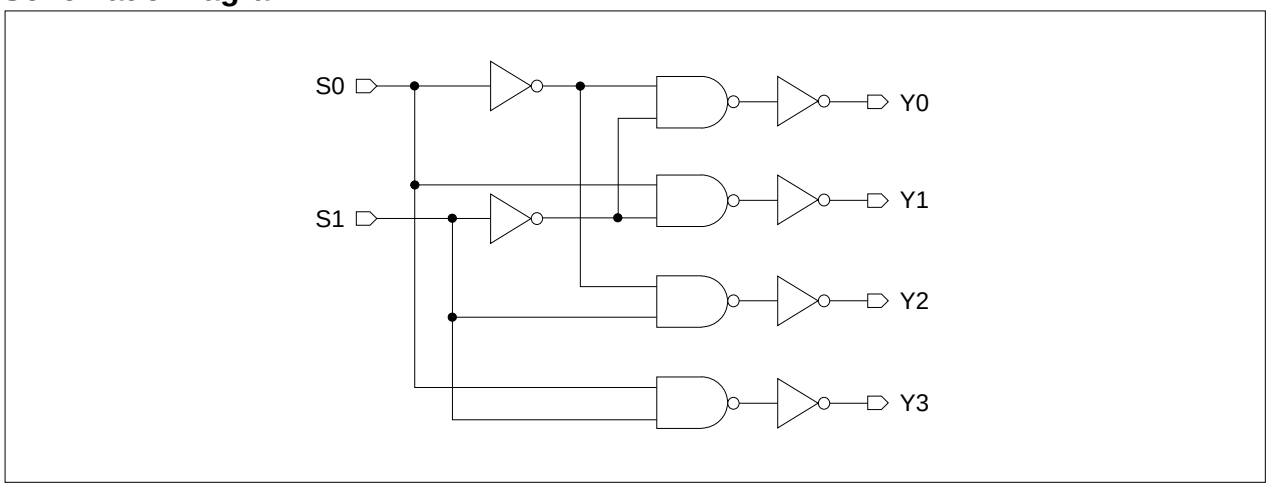
Truth Table

S1	S0	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Cell Data

Input Load (SL)		Gate Count
S0	S1	
2.6	2.4	6.00

Schematic Diagram



DC4

2 > 4 Non-Inverting Decoder

Switching Characteristics

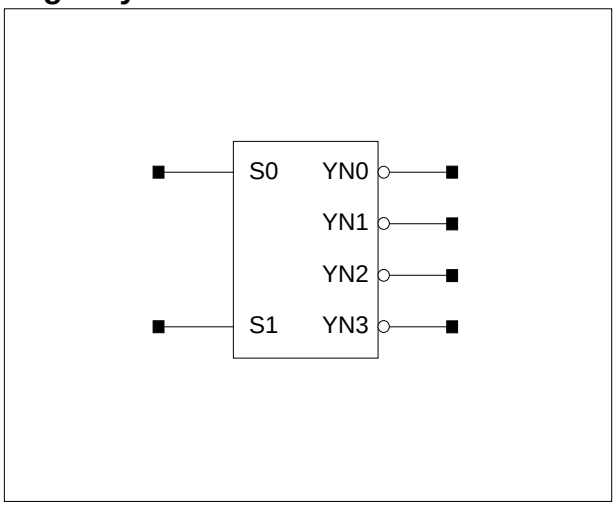
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

DC4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to Y0	t_R	0.145	0.073 + 0.036*SL	0.064 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.115	0.051 + 0.032*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.293	0.254 + 0.020*SL	0.262 + 0.017*SL	0.264 + 0.017*SL
	t_{PHL}	0.264	0.226 + 0.019*SL	0.232 + 0.018*SL	0.234 + 0.018*SL
S1 to Y0	t_R	0.144	0.072 + 0.036*SL	0.064 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.117	0.054 + 0.032*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.287	0.248 + 0.020*SL	0.256 + 0.017*SL	0.258 + 0.017*SL
	t_{PHL}	0.272	0.233 + 0.019*SL	0.240 + 0.018*SL	0.242 + 0.018*SL
S0 to Y1	t_R	0.145	0.073 + 0.036*SL	0.065 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.118	0.055 + 0.031*SL	0.048 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.185	0.147 + 0.019*SL	0.154 + 0.017*SL	0.156 + 0.017*SL
	t_{PHL}	0.185	0.146 + 0.019*SL	0.153 + 0.018*SL	0.154 + 0.018*SL
S1 to Y1	t_R	0.144	0.071 + 0.036*SL	0.063 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.118	0.056 + 0.031*SL	0.048 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.284	0.245 + 0.019*SL	0.253 + 0.017*SL	0.255 + 0.017*SL
	t_{PHL}	0.270	0.231 + 0.019*SL	0.238 + 0.018*SL	0.240 + 0.018*SL
S0 to Y2	t_R	0.144	0.071 + 0.036*SL	0.064 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.118	0.056 + 0.031*SL	0.048 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.285	0.246 + 0.019*SL	0.254 + 0.017*SL	0.256 + 0.017*SL
	t_{PHL}	0.269	0.230 + 0.020*SL	0.237 + 0.018*SL	0.239 + 0.018*SL
S1 to Y2	t_R	0.145	0.073 + 0.036*SL	0.065 + 0.038*SL	0.047 + 0.039*SL
	t_F	0.118	0.055 + 0.031*SL	0.048 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.187	0.148 + 0.019*SL	0.156 + 0.017*SL	0.157 + 0.017*SL
	t_{PHL}	0.186	0.147 + 0.019*SL	0.154 + 0.018*SL	0.156 + 0.018*SL
S0 to Y3	t_R	0.145	0.072 + 0.037*SL	0.065 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.118	0.055 + 0.031*SL	0.048 + 0.033*SL	0.035 + 0.034*SL
	t_{PLH}	0.173	0.134 + 0.019*SL	0.142 + 0.017*SL	0.144 + 0.017*SL
	t_{PHL}	0.196	0.158 + 0.019*SL	0.164 + 0.018*SL	0.166 + 0.018*SL
S1 to Y3	t_R	0.145	0.073 + 0.036*SL	0.065 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.118	0.055 + 0.031*SL	0.048 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.184	0.146 + 0.019*SL	0.153 + 0.017*SL	0.155 + 0.017*SL
	t_{PHL}	0.184	0.146 + 0.019*SL	0.152 + 0.018*SL	0.154 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Logic Symbol



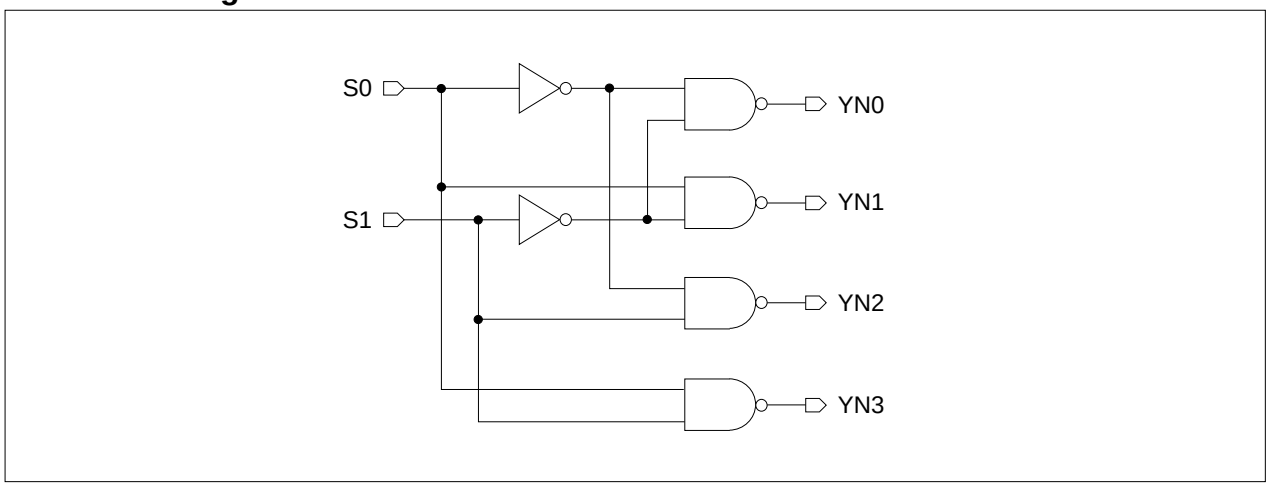
Truth Table

S1	S0	YN0	YN1	YN2	YN3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Cell Data

Input Load (SL)		Gate Count
S0	S1	
3.1	2.8	4.00

Schematic Diagram



DC4I

2 > 4 Inverting Decoder

Switching Characteristics

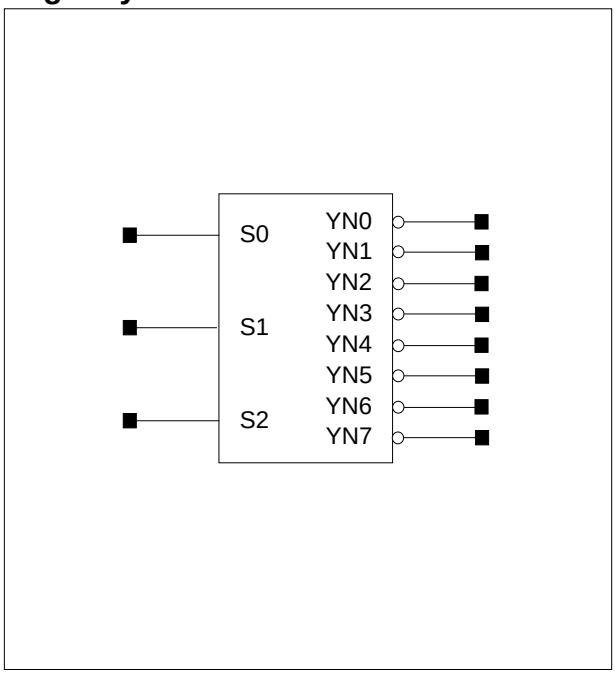
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

DC4I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	t_R	0.154	0.085 + 0.035*SL	0.071 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.166	0.082 + 0.042*SL	0.076 + 0.043*SL	0.058 + 0.044*SL
	t_{PLH}	0.218	0.180 + 0.019*SL	0.187 + 0.017*SL	0.188 + 0.017*SL
	t_{PHL}	0.237	0.190 + 0.023*SL	0.199 + 0.021*SL	0.202 + 0.021*SL
S1 to YN0	t_R	0.168	0.098 + 0.035*SL	0.085 + 0.038*SL	0.067 + 0.039*SL
	t_F	0.159	0.076 + 0.041*SL	0.068 + 0.043*SL	0.057 + 0.044*SL
	t_{PLH}	0.220	0.183 + 0.018*SL	0.187 + 0.017*SL	0.187 + 0.017*SL
	t_{PHL}	0.225	0.181 + 0.022*SL	0.186 + 0.021*SL	0.188 + 0.021*SL
S0 to YN1	t_R	0.174	0.110 + 0.032*SL	0.086 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.183	0.108 + 0.038*SL	0.087 + 0.043*SL	0.054 + 0.044*SL
	t_{PLH}	0.116	0.076 + 0.020*SL	0.087 + 0.017*SL	0.084 + 0.017*SL
	t_{PHL}	0.109	0.061 + 0.024*SL	0.073 + 0.021*SL	0.070 + 0.021*SL
S1 to YN1	t_R	0.168	0.099 + 0.035*SL	0.085 + 0.038*SL	0.068 + 0.039*SL
	t_F	0.159	0.077 + 0.041*SL	0.067 + 0.043*SL	0.056 + 0.044*SL
	t_{PLH}	0.221	0.184 + 0.018*SL	0.188 + 0.017*SL	0.188 + 0.017*SL
	t_{PHL}	0.225	0.181 + 0.022*SL	0.186 + 0.021*SL	0.187 + 0.021*SL
S0 to YN2	t_R	0.172	0.102 + 0.035*SL	0.090 + 0.038*SL	0.072 + 0.039*SL
	t_F	0.163	0.080 + 0.042*SL	0.072 + 0.044*SL	0.060 + 0.044*SL
	t_{PLH}	0.225	0.188 + 0.019*SL	0.192 + 0.017*SL	0.192 + 0.017*SL
	t_{PHL}	0.232	0.188 + 0.022*SL	0.192 + 0.021*SL	0.194 + 0.021*SL
S1 to YN2	t_R	0.177	0.113 + 0.032*SL	0.089 + 0.038*SL	0.054 + 0.039*SL
	t_F	0.188	0.112 + 0.038*SL	0.091 + 0.043*SL	0.057 + 0.044*SL
	t_{PLH}	0.118	0.078 + 0.020*SL	0.089 + 0.017*SL	0.086 + 0.017*SL
	t_{PHL}	0.112	0.064 + 0.024*SL	0.076 + 0.021*SL	0.072 + 0.021*SL
S0 to YN3	t_R	0.190	0.127 + 0.032*SL	0.103 + 0.038*SL	0.066 + 0.039*SL
	t_F	0.178	0.101 + 0.038*SL	0.080 + 0.044*SL	0.056 + 0.044*SL
	t_{PLH}	0.129	0.091 + 0.019*SL	0.097 + 0.017*SL	0.093 + 0.017*SL
	t_{PHL}	0.099	0.053 + 0.023*SL	0.060 + 0.021*SL	0.059 + 0.021*SL
S1 to YN3	t_R	0.174	0.111 + 0.032*SL	0.087 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.185	0.108 + 0.039*SL	0.090 + 0.043*SL	0.056 + 0.044*SL
	t_{PLH}	0.117	0.076 + 0.020*SL	0.088 + 0.017*SL	0.085 + 0.017*SL
	t_{PHL}	0.110	0.062 + 0.024*SL	0.074 + 0.021*SL	0.071 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Logic Symbol



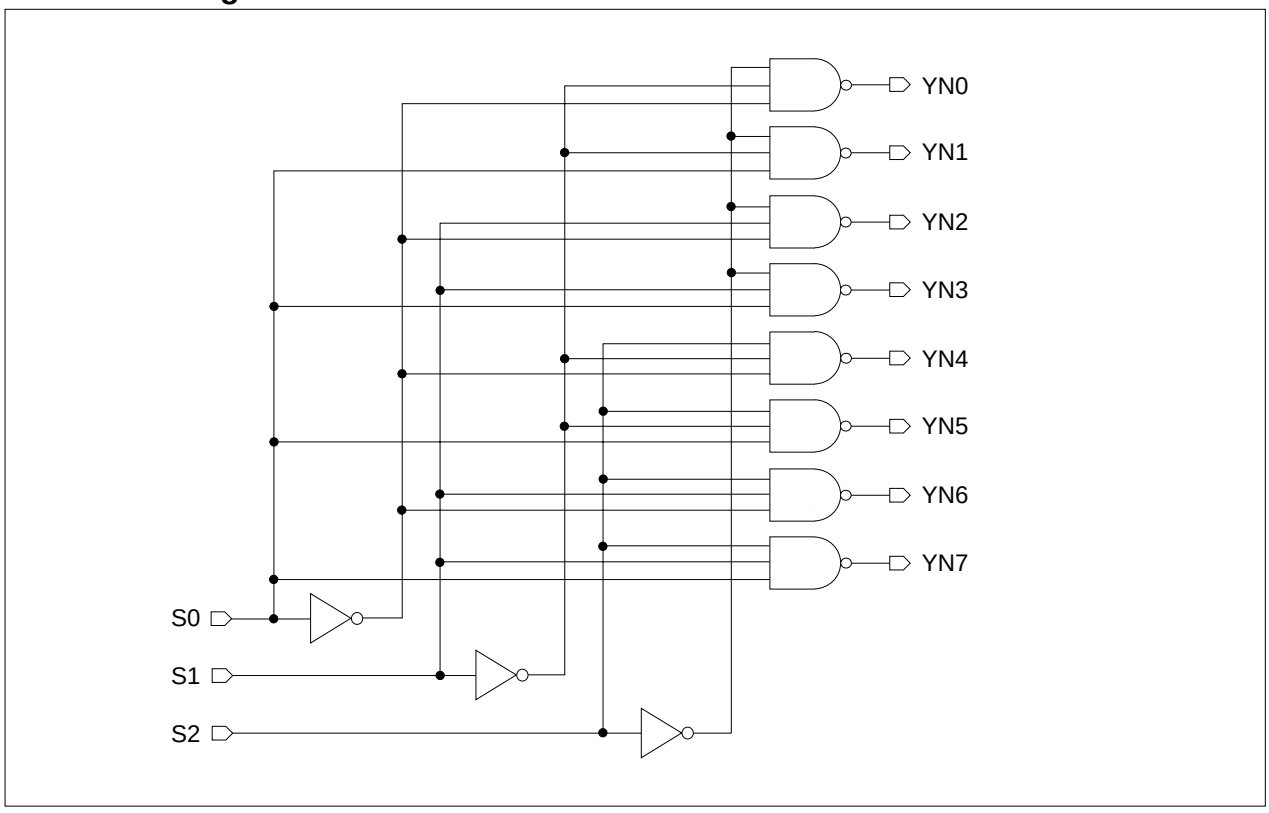
Truth Table

S2	S1	S0	YN0	YN1	YN2	YN3	YN4	YN5	YN6	YN7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Cell Data

Input Load (SL)			Gate Count
S0	S1	S2	
5.4	5.0	5.6	10.00

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	t_R	0.190	0.111 + 0.039*SL	0.102 + 0.042*SL	0.080 + 0.042*SL
	t_F	0.232	0.131 + 0.050*SL	0.123 + 0.052*SL	0.104 + 0.053*SL
	t_{PLH}	0.260	0.218 + 0.021*SL	0.226 + 0.019*SL	0.228 + 0.019*SL
	t_{PHL}	0.294	0.243 + 0.026*SL	0.250 + 0.024*SL	0.251 + 0.024*SL
S1 to YN0	t_R	0.216	0.138 + 0.039*SL	0.127 + 0.041*SL	0.101 + 0.042*SL
	t_F	0.232	0.133 + 0.050*SL	0.123 + 0.052*SL	0.105 + 0.053*SL
	t_{PLH}	0.298	0.256 + 0.021*SL	0.263 + 0.019*SL	0.266 + 0.019*SL
	t_{PHL}	0.312	0.261 + 0.026*SL	0.267 + 0.024*SL	0.269 + 0.024*SL
S2 to YN0	t_R	0.233	0.157 + 0.038*SL	0.142 + 0.041*SL	0.117 + 0.042*SL
	t_F	0.225	0.124 + 0.050*SL	0.116 + 0.052*SL	0.105 + 0.053*SL
	t_{PLH}	0.286	0.245 + 0.020*SL	0.251 + 0.019*SL	0.252 + 0.019*SL
	t_{PHL}	0.288	0.238 + 0.025*SL	0.241 + 0.024*SL	0.244 + 0.024*SL
S0 to YN1	t_R	0.200	0.128 + 0.036*SL	0.106 + 0.041*SL	0.077 + 0.042*SL
	t_F	0.241	0.146 + 0.048*SL	0.128 + 0.052*SL	0.103 + 0.053*SL
	t_{PLH}	0.135	0.093 + 0.021*SL	0.101 + 0.019*SL	0.098 + 0.019*SL
	t_{PHL}	0.133	0.082 + 0.025*SL	0.088 + 0.024*SL	0.084 + 0.024*SL
S1 to YN1	t_R	0.217	0.139 + 0.039*SL	0.129 + 0.041*SL	0.104 + 0.042*SL
	t_F	0.234	0.134 + 0.050*SL	0.124 + 0.052*SL	0.106 + 0.053*SL
	t_{PLH}	0.300	0.258 + 0.021*SL	0.265 + 0.019*SL	0.268 + 0.019*SL
	t_{PHL}	0.313	0.262 + 0.026*SL	0.268 + 0.024*SL	0.271 + 0.024*SL
S2 to YN1	t_R	0.235	0.160 + 0.038*SL	0.145 + 0.041*SL	0.120 + 0.042*SL
	t_F	0.226	0.125 + 0.050*SL	0.117 + 0.052*SL	0.105 + 0.053*SL
	t_{PLH}	0.288	0.248 + 0.020*SL	0.253 + 0.019*SL	0.254 + 0.019*SL
	t_{PHL}	0.290	0.240 + 0.025*SL	0.243 + 0.024*SL	0.246 + 0.024*SL
S0 to YN2	t_R	0.191	0.112 + 0.039*SL	0.103 + 0.042*SL	0.081 + 0.042*SL
	t_F	0.234	0.134 + 0.050*SL	0.126 + 0.052*SL	0.106 + 0.053*SL
	t_{PLH}	0.260	0.218 + 0.021*SL	0.226 + 0.019*SL	0.228 + 0.019*SL
	t_{PHL}	0.295	0.243 + 0.026*SL	0.251 + 0.024*SL	0.253 + 0.024*SL
S1 to YN2	t_R	0.220	0.148 + 0.036*SL	0.126 + 0.041*SL	0.097 + 0.042*SL
	t_F	0.238	0.142 + 0.048*SL	0.126 + 0.052*SL	0.098 + 0.053*SL
	t_{PLH}	0.152	0.113 + 0.020*SL	0.116 + 0.019*SL	0.114 + 0.019*SL
	t_{PHL}	0.131	0.080 + 0.026*SL	0.086 + 0.024*SL	0.082 + 0.024*SL
S2 to YN2	t_R	0.235	0.160 + 0.038*SL	0.145 + 0.041*SL	0.119 + 0.042*SL
	t_F	0.226	0.125 + 0.050*SL	0.117 + 0.052*SL	0.105 + 0.053*SL
	t_{PLH}	0.288	0.247 + 0.020*SL	0.252 + 0.019*SL	0.254 + 0.019*SL
	t_{PHL}	0.289	0.239 + 0.025*SL	0.243 + 0.024*SL	0.245 + 0.024*SL
S0 to YN3	t_R	0.200	0.128 + 0.036*SL	0.106 + 0.041*SL	0.077 + 0.042*SL
	t_F	0.241	0.146 + 0.048*SL	0.128 + 0.052*SL	0.102 + 0.053*SL
	t_{PLH}	0.135	0.094 + 0.021*SL	0.101 + 0.019*SL	0.099 + 0.019*SL
	t_{PHL}	0.134	0.083 + 0.025*SL	0.089 + 0.024*SL	0.086 + 0.024*SL
S1 to YN3	t_R	0.219	0.147 + 0.036*SL	0.125 + 0.041*SL	0.097 + 0.042*SL
	t_F	0.235	0.138 + 0.048*SL	0.122 + 0.052*SL	0.102 + 0.053*SL
	t_{PLH}	0.158	0.119 + 0.020*SL	0.121 + 0.019*SL	0.119 + 0.019*SL
	t_{PHL}	0.139	0.088 + 0.025*SL	0.093 + 0.024*SL	0.091 + 0.024*SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

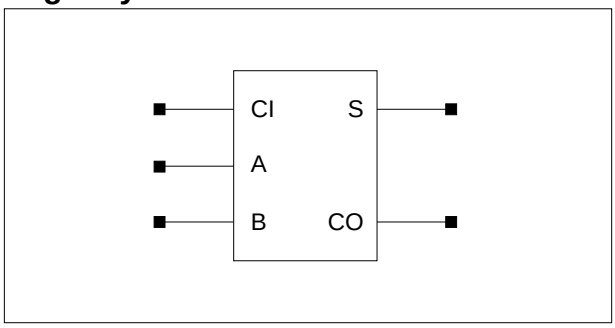
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S2 to YN3	t_R	0.233	0.157 + 0.038*SL	0.143 + 0.041*SL	0.118 + 0.042*SL
	t_F	0.225	0.125 + 0.050*SL	0.116 + 0.052*SL	0.104 + 0.053*SL
	t_{PLH}	0.287	0.247 + 0.020*SL	0.252 + 0.019*SL	0.253 + 0.019*SL
	t_{PHL}	0.288	0.238 + 0.025*SL	0.242 + 0.024*SL	0.244 + 0.024*SL
S0 to YN4	t_R	0.190	0.111 + 0.040*SL	0.103 + 0.042*SL	0.081 + 0.042*SL
	t_F	0.232	0.132 + 0.050*SL	0.124 + 0.052*SL	0.104 + 0.053*SL
	t_{PLH}	0.260	0.218 + 0.021*SL	0.226 + 0.019*SL	0.228 + 0.019*SL
	t_{PHL}	0.295	0.243 + 0.026*SL	0.250 + 0.024*SL	0.251 + 0.024*SL
S1 to YN4	t_R	0.216	0.139 + 0.039*SL	0.127 + 0.041*SL	0.102 + 0.042*SL
	t_F	0.234	0.135 + 0.049*SL	0.124 + 0.052*SL	0.106 + 0.053*SL
	t_{PLH}	0.300	0.258 + 0.021*SL	0.265 + 0.019*SL	0.268 + 0.019*SL
	t_{PHL}	0.313	0.261 + 0.026*SL	0.267 + 0.024*SL	0.270 + 0.024*SL
S2 to YN4	t_R	0.242	0.171 + 0.036*SL	0.148 + 0.041*SL	0.115 + 0.042*SL
	t_F	0.229	0.133 + 0.048*SL	0.117 + 0.052*SL	0.094 + 0.053*SL
	t_{PLH}	0.160	0.121 + 0.019*SL	0.123 + 0.019*SL	0.120 + 0.019*SL
	t_{PHL}	0.124	0.074 + 0.025*SL	0.079 + 0.024*SL	0.072 + 0.024*SL
S0 to YN5	t_R	0.199	0.127 + 0.036*SL	0.106 + 0.041*SL	0.077 + 0.042*SL
	t_F	0.240	0.145 + 0.048*SL	0.127 + 0.052*SL	0.101 + 0.053*SL
	t_{PLH}	0.135	0.094 + 0.021*SL	0.101 + 0.019*SL	0.098 + 0.019*SL
	t_{PHL}	0.133	0.082 + 0.025*SL	0.088 + 0.024*SL	0.085 + 0.024*SL
S1 to YN5	t_R	0.216	0.139 + 0.038*SL	0.127 + 0.041*SL	0.102 + 0.042*SL
	t_F	0.232	0.133 + 0.050*SL	0.123 + 0.052*SL	0.105 + 0.053*SL
	t_{PLH}	0.300	0.258 + 0.021*SL	0.265 + 0.019*SL	0.268 + 0.019*SL
	t_{PHL}	0.313	0.262 + 0.026*SL	0.268 + 0.024*SL	0.270 + 0.024*SL
S2 to YN5	t_R	0.241	0.170 + 0.036*SL	0.147 + 0.041*SL	0.114 + 0.042*SL
	t_F	0.228	0.130 + 0.049*SL	0.117 + 0.052*SL	0.100 + 0.053*SL
	t_{PLH}	0.160	0.121 + 0.019*SL	0.122 + 0.019*SL	0.120 + 0.019*SL
	t_{PHL}	0.123	0.073 + 0.025*SL	0.077 + 0.024*SL	0.075 + 0.024*SL
S0 to YN6	t_R	0.191	0.112 + 0.039*SL	0.104 + 0.042*SL	0.082 + 0.042*SL
	t_F	0.235	0.135 + 0.050*SL	0.126 + 0.052*SL	0.106 + 0.053*SL
	t_{PLH}	0.261	0.219 + 0.021*SL	0.227 + 0.019*SL	0.229 + 0.019*SL
	t_{PHL}	0.296	0.244 + 0.026*SL	0.251 + 0.024*SL	0.253 + 0.024*SL
S1 to YN6	t_R	0.221	0.149 + 0.036*SL	0.128 + 0.041*SL	0.100 + 0.042*SL
	t_F	0.237	0.142 + 0.048*SL	0.124 + 0.052*SL	0.099 + 0.053*SL
	t_{PLH}	0.177	0.137 + 0.020*SL	0.140 + 0.019*SL	0.139 + 0.019*SL
	t_{PHL}	0.158	0.108 + 0.025*SL	0.113 + 0.024*SL	0.109 + 0.024*SL
S2 to YN6	t_R	0.243	0.171 + 0.036*SL	0.149 + 0.041*SL	0.116 + 0.042*SL
	t_F	0.230	0.132 + 0.049*SL	0.118 + 0.052*SL	0.097 + 0.053*SL
	t_{PLH}	0.161	0.122 + 0.019*SL	0.123 + 0.019*SL	0.121 + 0.019*SL
	t_{PHL}	0.125	0.074 + 0.025*SL	0.079 + 0.024*SL	0.074 + 0.024*SL
S0 to YN7	t_R	0.201	0.129 + 0.036*SL	0.107 + 0.041*SL	0.078 + 0.042*SL
	t_F	0.242	0.147 + 0.048*SL	0.129 + 0.052*SL	0.103 + 0.053*SL
	t_{PLH}	0.136	0.094 + 0.021*SL	0.101 + 0.019*SL	0.099 + 0.019*SL
	t_{PHL}	0.134	0.083 + 0.025*SL	0.089 + 0.024*SL	0.086 + 0.024*SL

ADDERS

Cell List

Cell Name	Function Description
FADH	Full Adder with 0.5X Drive
FA	Full Adder with 1X Drive
FAD2	Full Adder with 2X Drive
HADH	Half Adder with 0.5X Drive
HA	Half Adder with 1x Drive
HAD2	Half Adder with 2X Drive
SCG23	Full Adder with one inverted input

Logic Symbol



Truth Table

CI	A	B	S	CO
0	0	0	0	0
1	0	0	1	0
0	0	1	1	0
1	0	1	0	1
0	1	0	1	0
1	1	0	0	1
0	1	1	0	1
1	1	1	1	1

Cell Data

Input Load (SL)									Gate Count		
FADH			*FA*			*FAD2*			*FADH*	*FA*	*FAD2*
CI	A	B	CI	A	B	CI	A	B			
0.8	0.8	0.8	1.1	1.1	1.0	1.0	1.1	1.0	6.33	6.33	6.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FADH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.213	0.080 + 0.066*SL	0.065 + 0.070*SL	0.048 + 0.071*SL
	t_F	0.172	0.068 + 0.052*SL	0.061 + 0.054*SL	0.036 + 0.055*SL
	t_{PLH}	0.466	0.399 + 0.034*SL	0.405 + 0.032*SL	0.405 + 0.032*SL
	t_{PHL}	0.425	0.359 + 0.033*SL	0.374 + 0.029*SL	0.379 + 0.029*SL
B to S	t_R	0.212	0.079 + 0.066*SL	0.065 + 0.070*SL	0.048 + 0.071*SL
	t_F	0.174	0.071 + 0.052*SL	0.062 + 0.054*SL	0.036 + 0.055*SL
	t_{PLH}	0.543	0.476 + 0.034*SL	0.483 + 0.032*SL	0.482 + 0.032*SL
	t_{PHL}	0.514	0.447 + 0.033*SL	0.463 + 0.029*SL	0.468 + 0.029*SL
CI to S	t_R	0.209	0.076 + 0.067*SL	0.062 + 0.070*SL	0.048 + 0.071*SL
	t_F	0.181	0.078 + 0.052*SL	0.069 + 0.054*SL	0.038 + 0.055*SL
	t_{PLH}	0.375	0.308 + 0.034*SL	0.314 + 0.032*SL	0.313 + 0.032*SL
	t_{PHL}	0.374	0.305 + 0.034*SL	0.325 + 0.029*SL	0.331 + 0.029*SL
A to CO	t_R	0.213	0.080 + 0.067*SL	0.066 + 0.070*SL	0.048 + 0.071*SL
	t_F	0.175	0.068 + 0.053*SL	0.066 + 0.054*SL	0.039 + 0.055*SL
	t_{PLH}	0.445	0.377 + 0.034*SL	0.385 + 0.032*SL	0.385 + 0.032*SL
	t_{PHL}	0.417	0.349 + 0.034*SL	0.367 + 0.029*SL	0.375 + 0.029*SL
B to CO	t_R	0.213	0.079 + 0.067*SL	0.066 + 0.070*SL	0.048 + 0.071*SL
	t_F	0.180	0.076 + 0.052*SL	0.070 + 0.054*SL	0.039 + 0.055*SL
	t_{PLH}	0.538	0.471 + 0.034*SL	0.478 + 0.032*SL	0.478 + 0.032*SL
	t_{PHL}	0.521	0.453 + 0.034*SL	0.471 + 0.029*SL	0.480 + 0.029*SL
CI to CO	t_R	0.214	0.081 + 0.066*SL	0.066 + 0.070*SL	0.048 + 0.071*SL
	t_F	0.181	0.077 + 0.052*SL	0.069 + 0.054*SL	0.037 + 0.055*SL
	t_{PLH}	0.283	0.215 + 0.034*SL	0.223 + 0.032*SL	0.224 + 0.032*SL
	t_{PHL}	0.277	0.209 + 0.034*SL	0.228 + 0.029*SL	0.234 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.158	0.088 + 0.035*SL	0.077 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.142	0.077 + 0.032*SL	0.076 + 0.033*SL	0.048 + 0.033*SL
	t_{PLH}	0.473	0.434 + 0.020*SL	0.443 + 0.017*SL	0.445 + 0.017*SL
	t_{PHL}	0.413	0.369 + 0.022*SL	0.385 + 0.018*SL	0.397 + 0.018*SL
B to S	t_R	0.156	0.086 + 0.035*SL	0.075 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.151	0.085 + 0.033*SL	0.086 + 0.032*SL	0.055 + 0.033*SL
	t_{PLH}	0.561	0.521 + 0.020*SL	0.530 + 0.017*SL	0.532 + 0.017*SL
	t_{PHL}	0.548	0.502 + 0.023*SL	0.521 + 0.018*SL	0.537 + 0.018*SL
CI to S	t_R	0.150	0.079 + 0.036*SL	0.069 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.150	0.085 + 0.033*SL	0.085 + 0.033*SL	0.055 + 0.033*SL
	t_{PLH}	0.346	0.306 + 0.020*SL	0.316 + 0.018*SL	0.318 + 0.017*SL
	t_{PHL}	0.365	0.319 + 0.023*SL	0.339 + 0.018*SL	0.356 + 0.018*SL
A to CO	t_R	0.162	0.092 + 0.035*SL	0.081 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.140	0.073 + 0.034*SL	0.076 + 0.033*SL	0.052 + 0.033*SL
	t_{PLH}	0.459	0.419 + 0.020*SL	0.429 + 0.018*SL	0.432 + 0.017*SL
	t_{PHL}	0.398	0.354 + 0.022*SL	0.370 + 0.018*SL	0.386 + 0.018*SL
B to CO	t_R	0.164	0.092 + 0.036*SL	0.085 + 0.038*SL	0.058 + 0.039*SL
	t_F	0.147	0.082 + 0.033*SL	0.082 + 0.033*SL	0.054 + 0.033*SL
	t_{PLH}	0.568	0.527 + 0.021*SL	0.539 + 0.018*SL	0.546 + 0.017*SL
	t_{PHL}	0.531	0.487 + 0.022*SL	0.503 + 0.018*SL	0.519 + 0.018*SL
CI to CO	t_R	0.155	0.084 + 0.036*SL	0.075 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.146	0.081 + 0.033*SL	0.080 + 0.033*SL	0.051 + 0.033*SL
	t_{PLH}	0.252	0.212 + 0.020*SL	0.222 + 0.018*SL	0.227 + 0.017*SL
	t_{PHL}	0.267	0.222 + 0.023*SL	0.240 + 0.018*SL	0.255 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

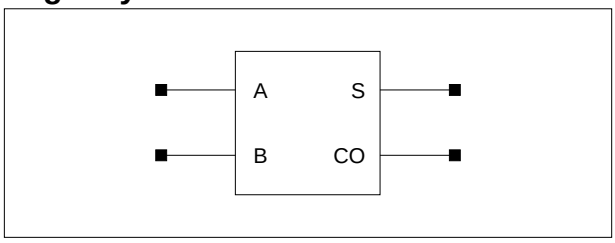
(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

FAD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.128	0.092 + 0.018*SL	0.087 + 0.019*SL	0.047 + 0.019*SL
	t_F	0.133	0.098 + 0.017*SL	0.103 + 0.016*SL	0.067 + 0.017*SL
	t_{PLH}	0.477	0.452 + 0.012*SL	0.465 + 0.009*SL	0.477 + 0.009*SL
	t_{PHL}	0.433	0.404 + 0.014*SL	0.424 + 0.009*SL	0.464 + 0.009*SL
B to S	t_R	0.124	0.089 + 0.017*SL	0.083 + 0.019*SL	0.047 + 0.019*SL
	t_F	0.134	0.099 + 0.018*SL	0.104 + 0.016*SL	0.066 + 0.017*SL
	t_{PLH}	0.566	0.542 + 0.012*SL	0.554 + 0.009*SL	0.566 + 0.009*SL
	t_{PHL}	0.572	0.543 + 0.015*SL	0.564 + 0.009*SL	0.605 + 0.009*SL
CI to S	t_R	0.119	0.084 + 0.018*SL	0.079 + 0.019*SL	0.046 + 0.019*SL
	t_F	0.129	0.093 + 0.018*SL	0.100 + 0.016*SL	0.065 + 0.017*SL
	t_{PLH}	0.369	0.345 + 0.012*SL	0.358 + 0.009*SL	0.371 + 0.009*SL
	t_{PHL}	0.389	0.359 + 0.015*SL	0.381 + 0.009*SL	0.422 + 0.009*SL
A to CO	t_R	0.131	0.097 + 0.017*SL	0.090 + 0.019*SL	0.051 + 0.019*SL
	t_F	0.115	0.080 + 0.017*SL	0.084 + 0.016*SL	0.055 + 0.017*SL
	t_{PLH}	0.459	0.434 + 0.012*SL	0.447 + 0.009*SL	0.461 + 0.009*SL
	t_{PHL}	0.400	0.373 + 0.014*SL	0.391 + 0.009*SL	0.424 + 0.009*SL
B to CO	t_R	0.134	0.099 + 0.017*SL	0.094 + 0.019*SL	0.057 + 0.019*SL
	t_F	0.122	0.088 + 0.017*SL	0.092 + 0.016*SL	0.057 + 0.017*SL
	t_{PLH}	0.573	0.547 + 0.013*SL	0.562 + 0.009*SL	0.582 + 0.009*SL
	t_{PHL}	0.528	0.500 + 0.014*SL	0.519 + 0.009*SL	0.552 + 0.009*SL
CI to CO	t_R	0.121	0.085 + 0.018*SL	0.081 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.116	0.081 + 0.017*SL	0.086 + 0.016*SL	0.053 + 0.017*SL
	t_{PLH}	0.251	0.227 + 0.012*SL	0.240 + 0.009*SL	0.255 + 0.009*SL
	t_{PHL}	0.265	0.237 + 0.014*SL	0.256 + 0.009*SL	0.289 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



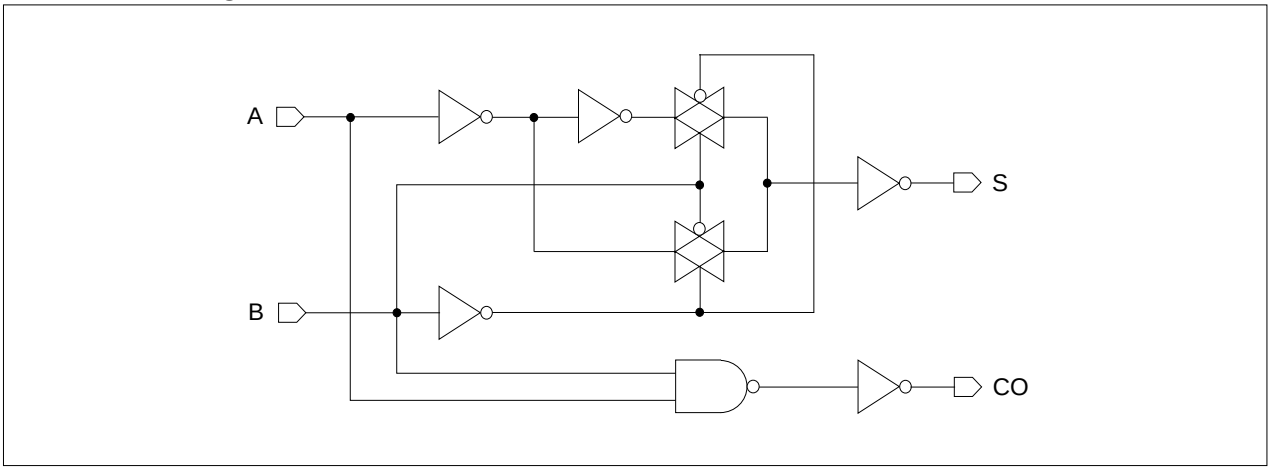
Truth Table

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Data

Input Load (SL)						Gate Count		
HADH		*HA*		*HAD2*		*HADH*	*HA*	*HAD2*
A	B	A	B	A	B			
1.1	1.5	1.9	2.5	1.9	2.5	3.67	3.67	4.33

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

HADH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.207	0.072 + 0.067*SL	0.060 + 0.070*SL	0.047 + 0.071*SL
	t_F	0.178	0.074 + 0.052*SL	0.068 + 0.054*SL	0.038 + 0.055*SL
	t_{PLH}	0.337	0.270 + 0.033*SL	0.276 + 0.032*SL	0.276 + 0.032*SL
	t_{PHL}	0.308	0.240 + 0.034*SL	0.259 + 0.029*SL	0.266 + 0.029*SL
B to S	t_R	0.208	0.073 + 0.067*SL	0.062 + 0.070*SL	0.047 + 0.071*SL
	t_F	0.175	0.069 + 0.053*SL	0.065 + 0.054*SL	0.037 + 0.055*SL
	t_{PLH}	0.266	0.198 + 0.034*SL	0.205 + 0.032*SL	0.206 + 0.032*SL
	t_{PHL}	0.250	0.182 + 0.034*SL	0.201 + 0.029*SL	0.208 + 0.029*SL
A to CO	t_R	0.203	0.069 + 0.067*SL	0.057 + 0.070*SL	0.047 + 0.071*SL
	t_F	0.155	0.052 + 0.052*SL	0.041 + 0.054*SL	0.031 + 0.055*SL
	t_{PLH}	0.195	0.129 + 0.033*SL	0.133 + 0.032*SL	0.133 + 0.032*SL
	t_{PHL}	0.214	0.153 + 0.030*SL	0.158 + 0.029*SL	0.159 + 0.029*SL
B to CO	t_R	0.204	0.069 + 0.067*SL	0.057 + 0.070*SL	0.047 + 0.071*SL
	t_F	0.155	0.052 + 0.052*SL	0.041 + 0.054*SL	0.031 + 0.055*SL
	t_{PLH}	0.206	0.140 + 0.033*SL	0.144 + 0.032*SL	0.144 + 0.032*SL
	t_{PHL}	0.202	0.141 + 0.030*SL	0.146 + 0.029*SL	0.147 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

HA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.148	0.076 + 0.036*SL	0.068 + 0.038*SL	0.048 + 0.039*SL
	t_F	0.139	0.073 + 0.033*SL	0.074 + 0.033*SL	0.048 + 0.033*SL
	t_{PLH}	0.310	0.270 + 0.020*SL	0.279 + 0.018*SL	0.282 + 0.017*SL
	t_{PHL}	0.290	0.245 + 0.023*SL	0.263 + 0.018*SL	0.276 + 0.018*SL
B to S	t_R	0.148	0.074 + 0.037*SL	0.070 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.137	0.069 + 0.034*SL	0.073 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.230	0.190 + 0.020*SL	0.201 + 0.018*SL	0.206 + 0.017*SL
	t_{PHL}	0.231	0.187 + 0.022*SL	0.204 + 0.018*SL	0.217 + 0.018*SL
A to CO	t_R	0.140	0.068 + 0.036*SL	0.060 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.117	0.055 + 0.031*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.156	0.118 + 0.019*SL	0.125 + 0.017*SL	0.125 + 0.017*SL
	t_{PHL}	0.190	0.152 + 0.019*SL	0.158 + 0.018*SL	0.160 + 0.018*SL
B to CO	t_R	0.140	0.068 + 0.036*SL	0.060 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.114	0.050 + 0.032*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.166	0.127 + 0.019*SL	0.134 + 0.017*SL	0.135 + 0.017*SL
	t_{PHL}	0.175	0.137 + 0.019*SL	0.143 + 0.018*SL	0.144 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

HAD2

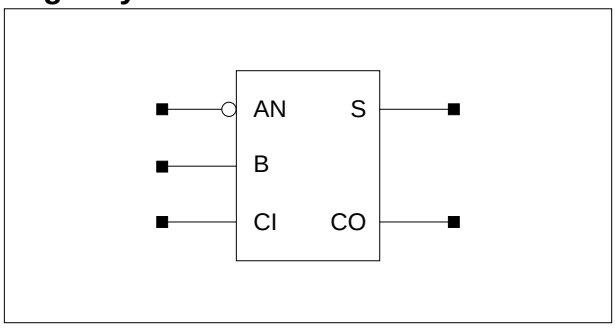
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.119	0.083 + 0.018*SL	0.079 + 0.019*SL	0.045 + 0.019*SL
	t_F	0.113	0.077 + 0.018*SL	0.084 + 0.016*SL	0.054 + 0.017*SL
	t_{PLH}	0.332	0.308 + 0.012*SL	0.321 + 0.009*SL	0.335 + 0.009*SL
	t_{PHL}	0.300	0.271 + 0.014*SL	0.291 + 0.009*SL	0.327 + 0.009*SL
B to S	t_R	0.118	0.081 + 0.019*SL	0.079 + 0.019*SL	0.048 + 0.019*SL
	t_F	0.109	0.071 + 0.019*SL	0.081 + 0.016*SL	0.054 + 0.017*SL
	t_{PLH}	0.240	0.215 + 0.013*SL	0.230 + 0.009*SL	0.248 + 0.009*SL
	t_{PHL}	0.228	0.200 + 0.014*SL	0.219 + 0.009*SL	0.255 + 0.009*SL
A to CO	t_R	0.102	0.066 + 0.018*SL	0.062 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.083	0.053 + 0.015*SL	0.047 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.157	0.135 + 0.011*SL	0.144 + 0.009*SL	0.151 + 0.009*SL
	t_{PHL}	0.187	0.164 + 0.011*SL	0.174 + 0.009*SL	0.180 + 0.009*SL
B to CO	t_R	0.102	0.065 + 0.018*SL	0.061 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.081	0.051 + 0.015*SL	0.045 + 0.017*SL	0.025 + 0.017*SL
	t_{PLH}	0.170	0.147 + 0.011*SL	0.157 + 0.009*SL	0.163 + 0.009*SL
	t_{PHL}	0.174	0.152 + 0.011*SL	0.161 + 0.009*SL	0.167 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

SCG23

Full Adder with one inverted input

Logic Symbol



Truth Table

AN	B	CI	S	CO
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	0
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

Cell Data

Input Load (SL)			Gate Count
CI	AN	B	
1.1	0.8	1.0	6.67

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

SCG23

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to S	t_R	0.158	0.088 + 0.035*SL	0.077 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.147	0.082 + 0.032*SL	0.081 + 0.033*SL	0.054 + 0.033*SL
	t_{PLH}	0.557	0.517 + 0.020*SL	0.527 + 0.017*SL	0.528 + 0.017*SL
	t_{PHL}	0.487	0.442 + 0.023*SL	0.460 + 0.018*SL	0.476 + 0.018*SL
B to S	t_R	0.156	0.085 + 0.035*SL	0.075 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.151	0.085 + 0.033*SL	0.086 + 0.032*SL	0.055 + 0.033*SL
	t_{PLH}	0.562	0.523 + 0.020*SL	0.531 + 0.017*SL	0.534 + 0.017*SL
	t_{PHL}	0.549	0.503 + 0.023*SL	0.522 + 0.018*SL	0.539 + 0.018*SL
CI to S	t_R	0.150	0.079 + 0.036*SL	0.069 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.150	0.085 + 0.032*SL	0.084 + 0.033*SL	0.055 + 0.033*SL
	t_{PLH}	0.346	0.306 + 0.020*SL	0.316 + 0.018*SL	0.319 + 0.017*SL
	t_{PHL}	0.366	0.319 + 0.023*SL	0.339 + 0.018*SL	0.357 + 0.018*SL
AN to CO	t_R	0.163	0.092 + 0.035*SL	0.081 + 0.038*SL	0.053 + 0.039*SL
	t_F	0.140	0.074 + 0.033*SL	0.075 + 0.033*SL	0.052 + 0.033*SL
	t_{PLH}	0.542	0.502 + 0.020*SL	0.512 + 0.018*SL	0.515 + 0.017*SL
	t_{PHL}	0.446	0.402 + 0.022*SL	0.418 + 0.018*SL	0.434 + 0.018*SL
B to CO	t_R	0.165	0.092 + 0.036*SL	0.086 + 0.038*SL	0.058 + 0.039*SL
	t_F	0.147	0.082 + 0.033*SL	0.083 + 0.033*SL	0.054 + 0.033*SL
	t_{PLH}	0.570	0.529 + 0.021*SL	0.541 + 0.018*SL	0.548 + 0.017*SL
	t_{PHL}	0.533	0.488 + 0.022*SL	0.505 + 0.018*SL	0.521 + 0.018*SL
CI to CO	t_R	0.155	0.084 + 0.036*SL	0.075 + 0.038*SL	0.052 + 0.039*SL
	t_F	0.146	0.081 + 0.033*SL	0.080 + 0.033*SL	0.051 + 0.033*SL
	t_{PLH}	0.252	0.212 + 0.020*SL	0.222 + 0.018*SL	0.227 + 0.017*SL
	t_{PHL}	0.267	0.222 + 0.023*SL	0.241 + 0.018*SL	0.255 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

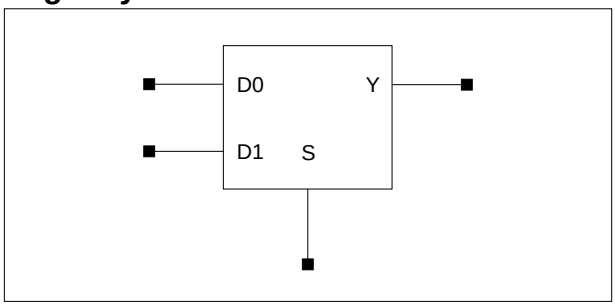
Cell List

Cell Name	Function Description
MX2DH	2 > 1 Non-Inverting Mux with 0.5X Drive
MX2	2 > 1 Non-Inverting Mux
MX2D2	2 > 1 Non-Inverting Mux with 2X Drive
MX2D4	2 > 1 Non-Inverting Mux with 4X Drive
MX2X4	4-Bit 2 > 1 Non-Inverting Mux
MX2IDH	2 > 1 Inverting Mux with 0.5X Drive
MX2I	2 > 1 Inverting Mux
MX2ID2	2 > 1 Inverting Mux with 2X Drive
MX2ID4	2 > 1 Inverting Mux with 4X Drive
MX2IDHA	2 > 1 Inverting Mux with Separate S and SN Inputs, 0.5X Drive
MX2IA	2 > 1 Inverting Mux with Separate S and SN Inputs
MX2ID2A	2 > 1 Inverting Mux with Separate S and SN Inputs, 2X Drive
MX2ID4A	2 > 1 Inverting Mux with Separate S and SN Inputs, 4X Drive
MX2IX4	4-Bit 2 > 1 Inverting Mux
MX3I	3 > 1 Inverting Mux
MX3ID2	3 > 1 Inverting Mux with 2X Drive
MX3ID4	3 > 1 Inverting Mux with 4X Drive
MX4	4 > 1 Non-Inverting Mux
MX4D2	4 > 1 Non-Inverting Mux with 2X Drive
MX4D4	4 > 1 Non-Inverting Mux with 4X Drive
MX8	8 > 1 Non-Inverting Mux
MX8D2	8 > 1 Non-Inverting Mux with 2X Drive
MX8D4	8 > 1 Non-inverting Mux with 4X Drive

MX2DH/MX2/MX2D2/MX2D4

2 > 1 Non-Inverting MUX with 0.5X/1X/2X/4X Drive

Logic Symbol



Truth Table

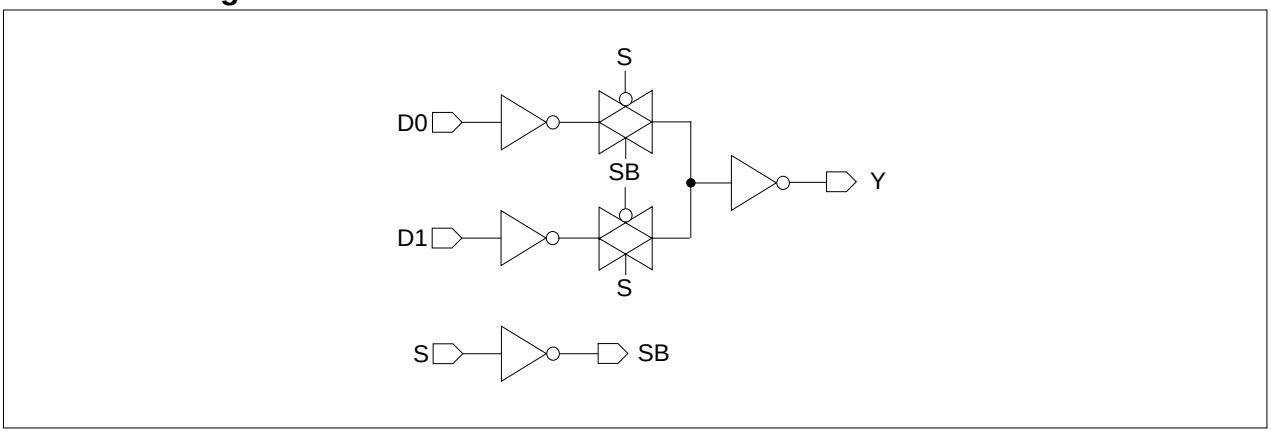
D0	D1	S	Y
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

Cell Data

Input Load (SL)											
MX2DH			*MX2*			*MX2D2*			*MX2D4*		
D0	D1	S	D0	D1	S	D0	D1	S	D0	D1	S
0.5	0.5	0.9	0.8	0.8	1.3	0.8	0.8	1.3	0.8	0.8	1.3

Gate Count			
MX2DH	*MX2*	*MX2D2*	*MX2D4*
2.33	2.33	2.67	3.33

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

MX2DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.208	0.071 + 0.069*SL	0.059 + 0.072*SL	0.046 + 0.072*SL
	t_F	0.177	0.074 + 0.051*SL	0.065 + 0.054*SL	0.036 + 0.055*SL
	t_{PLH}	0.245	0.178 + 0.034*SL	0.183 + 0.033*SL	0.182 + 0.033*SL
	t_{PHL}	0.261	0.194 + 0.034*SL	0.212 + 0.029*SL	0.218 + 0.029*SL
D1 to Y	t_R	0.208	0.071 + 0.068*SL	0.058 + 0.072*SL	0.046 + 0.072*SL
	t_F	0.176	0.072 + 0.052*SL	0.066 + 0.054*SL	0.035 + 0.055*SL
	t_{PLH}	0.244	0.176 + 0.034*SL	0.181 + 0.033*SL	0.181 + 0.033*SL
	t_{PHL}	0.261	0.193 + 0.034*SL	0.212 + 0.029*SL	0.217 + 0.029*SL
S to Y	t_R	0.208	0.071 + 0.069*SL	0.058 + 0.072*SL	0.046 + 0.072*SL
	t_F	0.172	0.067 + 0.052*SL	0.061 + 0.054*SL	0.035 + 0.055*SL
	t_{PLH}	0.268	0.200 + 0.034*SL	0.205 + 0.033*SL	0.205 + 0.033*SL
	t_{PHL}	0.245	0.177 + 0.034*SL	0.195 + 0.029*SL	0.201 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

MX2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.151	0.079 + 0.036*SL	0.071 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.139	0.073 + 0.033*SL	0.074 + 0.033*SL	0.046 + 0.033*SL
	t_{PLH}	0.229	0.190 + 0.020*SL	0.199 + 0.018*SL	0.202 + 0.017*SL
	t_{PHL}	0.237	0.193 + 0.022*SL	0.209 + 0.018*SL	0.220 + 0.018*SL
D1 to Y	t_R	0.151	0.079 + 0.036*SL	0.071 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.139	0.074 + 0.033*SL	0.074 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.228	0.188 + 0.020*SL	0.197 + 0.017*SL	0.200 + 0.017*SL
	t_{PHL}	0.237	0.193 + 0.022*SL	0.210 + 0.018*SL	0.221 + 0.018*SL
S to Y	t_R	0.150	0.077 + 0.036*SL	0.070 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.134	0.067 + 0.033*SL	0.070 + 0.033*SL	0.046 + 0.033*SL
	t_{PLH}	0.239	0.199 + 0.020*SL	0.209 + 0.018*SL	0.212 + 0.017*SL
	t_{PHL}	0.229	0.185 + 0.022*SL	0.201 + 0.018*SL	0.213 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

MX2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.120	0.084 + 0.018*SL	0.080 + 0.019*SL	0.047 + 0.019*SL
	t_F	0.115	0.080 + 0.018*SL	0.085 + 0.016*SL	0.055 + 0.017*SL
	t_{PLH}	0.239	0.215 + 0.012*SL	0.227 + 0.009*SL	0.241 + 0.009*SL
	t_{PHL}	0.244	0.216 + 0.014*SL	0.235 + 0.009*SL	0.268 + 0.009*SL
D1 to Y	t_R	0.120	0.084 + 0.018*SL	0.080 + 0.019*SL	0.047 + 0.019*SL
	t_F	0.116	0.080 + 0.018*SL	0.086 + 0.016*SL	0.054 + 0.017*SL
	t_{PLH}	0.239	0.215 + 0.012*SL	0.228 + 0.009*SL	0.241 + 0.009*SL
	t_{PHL}	0.244	0.216 + 0.014*SL	0.235 + 0.009*SL	0.268 + 0.009*SL
S to Y	t_R	0.119	0.083 + 0.018*SL	0.078 + 0.019*SL	0.047 + 0.019*SL
	t_F	0.111	0.074 + 0.018*SL	0.082 + 0.016*SL	0.054 + 0.017*SL
	t_{PLH}	0.241	0.217 + 0.012*SL	0.229 + 0.009*SL	0.244 + 0.009*SL
	t_{PHL}	0.231	0.203 + 0.014*SL	0.222 + 0.009*SL	0.255 + 0.009*SL

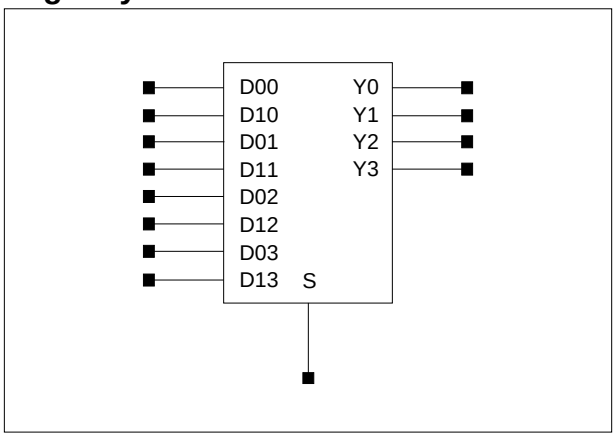
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

MX2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.137	0.119 + 0.009*SL	0.117 + 0.009*SL	0.096 + 0.010*SL
	t_F	0.132	0.112 + 0.010*SL	0.119 + 0.008*SL	0.122 + 0.008*SL
	t_{PLH}	0.296	0.280 + 0.008*SL	0.293 + 0.005*SL	0.329 + 0.004*SL
	t_{PHL}	0.298	0.280 + 0.009*SL	0.294 + 0.005*SL	0.354 + 0.005*SL
D1 to Y	t_R	0.136	0.119 + 0.009*SL	0.117 + 0.009*SL	0.095 + 0.010*SL
	t_F	0.133	0.113 + 0.010*SL	0.120 + 0.008*SL	0.122 + 0.008*SL
	t_{PLH}	0.295	0.279 + 0.008*SL	0.291 + 0.005*SL	0.328 + 0.004*SL
	t_{PHL}	0.299	0.281 + 0.009*SL	0.295 + 0.005*SL	0.355 + 0.005*SL
S to Y	t_R	0.136	0.119 + 0.009*SL	0.117 + 0.009*SL	0.095 + 0.010*SL
	t_F	0.130	0.111 + 0.010*SL	0.117 + 0.008*SL	0.121 + 0.008*SL
	t_{PLH}	0.290	0.274 + 0.008*SL	0.286 + 0.005*SL	0.323 + 0.004*SL
	t_{PHL}	0.281	0.263 + 0.009*SL	0.277 + 0.005*SL	0.338 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

S	Y0	Y1	Y2	Y3
0	D00	D01	D02	D03
1	D10	D11	D12	D13

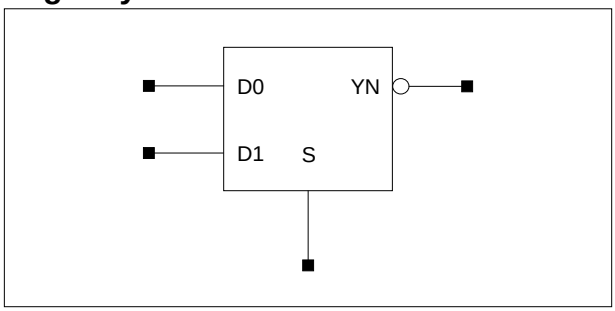
Cell Data

Input Load (SL)									Gate Count
D00	D01	D02	D03	D10	D11	D12	D13	S	
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	3.7	8.33

MX2X4 Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to Y0	t_R	0.152	0.080 + 0.036*SL	0.072 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.139	0.073 + 0.033*SL	0.075 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.230	0.190 + 0.020*SL	0.200 + 0.018*SL	0.202 + 0.017*SL
	t_{PHL}	0.238	0.194 + 0.022*SL	0.210 + 0.018*SL	0.221 + 0.018*SL
D10 to Y0	t_R	0.152	0.080 + 0.036*SL	0.072 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.140	0.074 + 0.033*SL	0.075 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.229	0.189 + 0.020*SL	0.198 + 0.017*SL	0.201 + 0.017*SL
	t_{PHL}	0.238	0.194 + 0.022*SL	0.210 + 0.018*SL	0.222 + 0.018*SL
S to Y0	t_R	0.155	0.084 + 0.036*SL	0.074 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.140	0.075 + 0.033*SL	0.074 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.280	0.241 + 0.020*SL	0.250 + 0.018*SL	0.253 + 0.017*SL
	t_{PHL}	0.276	0.232 + 0.022*SL	0.249 + 0.018*SL	0.260 + 0.018*SL
D01 to Y1	t_R	0.152	0.080 + 0.036*SL	0.072 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.139	0.073 + 0.033*SL	0.075 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.230	0.190 + 0.020*SL	0.200 + 0.018*SL	0.202 + 0.017*SL
	t_{PHL}	0.238	0.194 + 0.022*SL	0.210 + 0.018*SL	0.221 + 0.018*SL
D11 to Y1	t_R	0.152	0.080 + 0.036*SL	0.072 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.140	0.074 + 0.033*SL	0.075 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.229	0.189 + 0.020*SL	0.198 + 0.017*SL	0.201 + 0.017*SL
	t_{PHL}	0.238	0.194 + 0.022*SL	0.211 + 0.018*SL	0.222 + 0.018*SL
S to Y1	t_R	0.155	0.084 + 0.036*SL	0.074 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.140	0.076 + 0.032*SL	0.075 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.280	0.241 + 0.020*SL	0.250 + 0.018*SL	0.253 + 0.017*SL
	t_{PHL}	0.276	0.232 + 0.022*SL	0.248 + 0.018*SL	0.259 + 0.018*SL
D02 to Y2	t_R	0.152	0.080 + 0.036*SL	0.072 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.139	0.073 + 0.033*SL	0.075 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.230	0.190 + 0.020*SL	0.200 + 0.018*SL	0.202 + 0.017*SL
	t_{PHL}	0.238	0.194 + 0.022*SL	0.210 + 0.018*SL	0.221 + 0.018*SL
D12 to Y2	t_R	0.152	0.080 + 0.036*SL	0.072 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.140	0.074 + 0.033*SL	0.075 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.229	0.189 + 0.020*SL	0.198 + 0.017*SL	0.201 + 0.017*SL
	t_{PHL}	0.238	0.194 + 0.022*SL	0.210 + 0.018*SL	0.222 + 0.018*SL
S to Y2	t_R	0.155	0.084 + 0.036*SL	0.074 + 0.038*SL	0.051 + 0.039*SL
	t_F	0.140	0.076 + 0.032*SL	0.074 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.280	0.241 + 0.020*SL	0.250 + 0.018*SL	0.253 + 0.017*SL
	t_{PHL}	0.276	0.232 + 0.022*SL	0.248 + 0.018*SL	0.259 + 0.018*SL
D03 to Y3	t_R	0.151	0.079 + 0.036*SL	0.071 + 0.038*SL	0.050 + 0.039*SL
	t_F	0.139	0.073 + 0.033*SL	0.074 + 0.033*SL	0.046 + 0.033*SL
	t_{PLH}	0.229	0.189 + 0.020*SL	0.199 + 0.018*SL	0.201 + 0.017*SL
	t_{PHL}	0.237	0.193 + 0.022*SL	0.209 + 0.018*SL	0.220 + 0.018*SL
D13 to Y3	t_R	0.151	0.078 + 0.036*SL	0.071 + 0.038*SL	0.049 + 0.039*SL
	t_F	0.139	0.074 + 0.033*SL	0.074 + 0.033*SL	0.047 + 0.033*SL
	t_{PLH}	0.228	0.188 + 0.020*SL	0.197 + 0.017*SL	0.200 + 0.017*SL
	t_{PHL}	0.237	0.193 + 0.022*SL	0.210 + 0.018*SL	0.221 + 0.018*SL

Logic Symbol



Truth Table

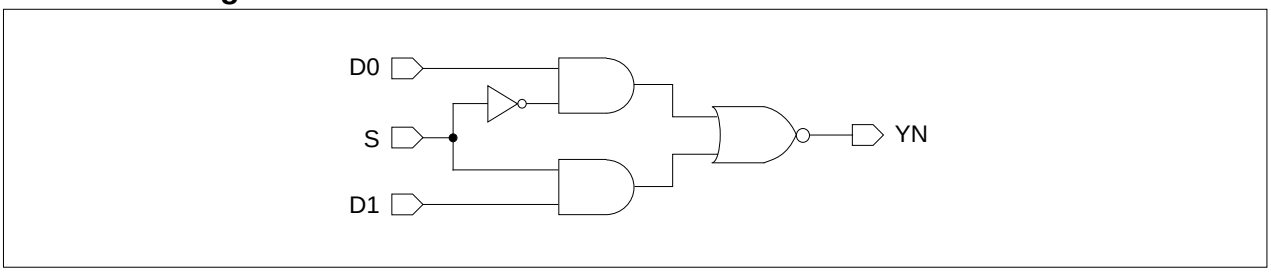
D0	D1	S	YN
0	x	0	1
1	x	0	0
x	0	1	1
x	1	1	0

Cell Data

Input Load (SL)											
MX2IDH			*MX2I*			*MX2ID2*			*MX2ID4*		
D0	D1	S	D0	D1	S	D0	D1	S	D0	D1	S
0.5	0.5	1.0	0.6	0.6	1.3	0.6	0.6	1.3	0.6	0.6	1.3

Gate Count			
MX2IDH	*MX2I*	*MX2ID2*	*MX2ID4*
2.67	2.67	3.00	3.67

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

MX2IDH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.196	0.057 + 0.070*SL	0.048 + 0.072*SL	0.045 + 0.072*SL
	t_F	0.152	0.048 + 0.052*SL	0.037 + 0.054*SL	0.030 + 0.055*SL
	t_{PLH}	0.324	0.258 + 0.033*SL	0.259 + 0.033*SL	0.259 + 0.033*SL
	t_{PHL}	0.283	0.223 + 0.030*SL	0.227 + 0.029*SL	0.228 + 0.029*SL
D1 to YN	t_R	0.196	0.057 + 0.070*SL	0.048 + 0.072*SL	0.045 + 0.072*SL
	t_F	0.151	0.046 + 0.052*SL	0.038 + 0.054*SL	0.030 + 0.055*SL
	t_{PLH}	0.326	0.260 + 0.033*SL	0.261 + 0.033*SL	0.261 + 0.033*SL
	t_{PHL}	0.284	0.223 + 0.030*SL	0.228 + 0.029*SL	0.228 + 0.029*SL
S to YN	t_R	0.196	0.056 + 0.070*SL	0.048 + 0.072*SL	0.045 + 0.072*SL
	t_F	0.151	0.046 + 0.052*SL	0.037 + 0.054*SL	0.030 + 0.055*SL
	t_{PLH}	0.343	0.277 + 0.033*SL	0.278 + 0.033*SL	0.278 + 0.033*SL
	t_{PHL}	0.364	0.303 + 0.030*SL	0.308 + 0.029*SL	0.308 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

MX2I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.053 + 0.031*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.322	0.285 + 0.018*SL	0.288 + 0.017*SL	0.288 + 0.017*SL
	t_{PHL}	0.283	0.244 + 0.019*SL	0.250 + 0.018*SL	0.252 + 0.018*SL
D1 to YN	t_R	0.136	0.065 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.115	0.052 + 0.032*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.323	0.286 + 0.018*SL	0.290 + 0.017*SL	0.290 + 0.017*SL
	t_{PHL}	0.283	0.245 + 0.019*SL	0.251 + 0.018*SL	0.252 + 0.018*SL
S to YN	t_R	0.136	0.065 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.053 + 0.031*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.343	0.306 + 0.018*SL	0.310 + 0.017*SL	0.310 + 0.017*SL
	t_{PHL}	0.350	0.311 + 0.019*SL	0.318 + 0.018*SL	0.320 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25°C, 3V, t_R/t_F = 0.26ns, SL: Standard Load)

MX2ID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.101	0.067 + 0.017*SL	0.059 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.084	0.051 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.332	0.310 + 0.011*SL	0.318 + 0.009*SL	0.321 + 0.009*SL
	t_{PHL}	0.286	0.263 + 0.011*SL	0.273 + 0.009*SL	0.280 + 0.009*SL
D1 to YN	t_R	0.101	0.067 + 0.017*SL	0.059 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.083	0.050 + 0.016*SL	0.049 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.333	0.312 + 0.011*SL	0.319 + 0.009*SL	0.322 + 0.009*SL
	t_{PHL}	0.286	0.264 + 0.011*SL	0.274 + 0.009*SL	0.281 + 0.009*SL
S to YN	t_R	0.101	0.067 + 0.017*SL	0.059 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.084	0.052 + 0.016*SL	0.050 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.353	0.332 + 0.011*SL	0.339 + 0.009*SL	0.342 + 0.009*SL
	t_{PHL}	0.353	0.331 + 0.011*SL	0.340 + 0.009*SL	0.348 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

MX2ID4

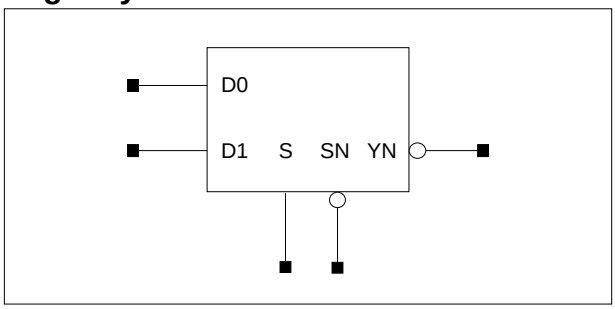
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.108	0.091 + 0.008*SL	0.087 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.089	0.072 + 0.008*SL	0.074 + 0.008*SL	0.051 + 0.008*SL
	t_{PLH}	0.385	0.372 + 0.007*SL	0.380 + 0.005*SL	0.395 + 0.004*SL
	t_{PHL}	0.330	0.316 + 0.007*SL	0.325 + 0.005*SL	0.346 + 0.004*SL
D1 to YN	t_R	0.108	0.091 + 0.008*SL	0.088 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.089	0.072 + 0.008*SL	0.074 + 0.008*SL	0.051 + 0.008*SL
	t_{PLH}	0.387	0.373 + 0.007*SL	0.382 + 0.005*SL	0.396 + 0.004*SL
	t_{PHL}	0.330	0.316 + 0.007*SL	0.325 + 0.005*SL	0.346 + 0.004*SL
S to YN	t_R	0.108	0.091 + 0.008*SL	0.088 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.089	0.072 + 0.008*SL	0.074 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.407	0.393 + 0.007*SL	0.402 + 0.005*SL	0.416 + 0.004*SL
	t_{PHL}	0.397	0.383 + 0.007*SL	0.392 + 0.005*SL	0.413 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

MX2IDHA/MX2IA/MX2ID2A/MX2ID4A

2 > 1 Inverting MUX with Separate S and SN Inputs, 0.5X/1X/2X/4X Drive

Logic Symbol



Truth Table

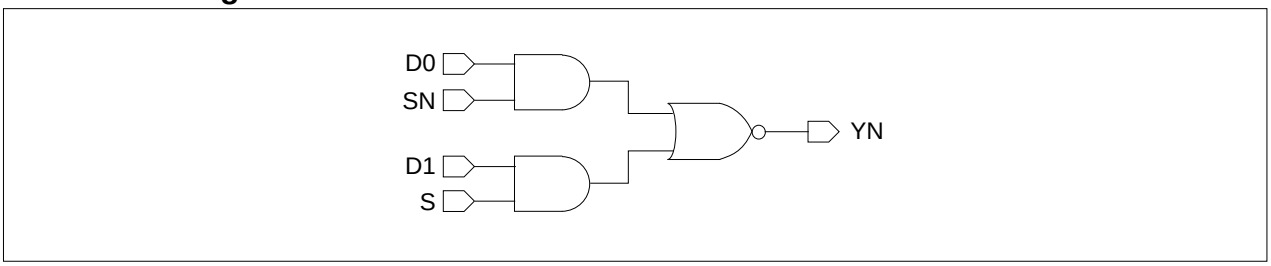
D0	D1	S	SN	YN
0	x	0	1	1
1	x	0	1	0
x	0	1	0	1
x	1	1	0	0

Cell Data

Input Load (SL)															
MX2IDHA				*MX2IA*				*MX2ID2A*				*MX2ID4A*			
D0	D1	S	SN	D0	D1	S	SN	D0	D1	S	SN	D0	D1	S	SN
0.5	0.5	0.6	0.5	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

Gate Count			
MX2IDHA	*MX2IA*	*MX2ID2A*	*MX2ID4A*
1.67	1.67	3.00	3.33

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

MX2IDHA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.446	0.179 + 0.133*SL	0.157 + 0.139*SL	0.156 + 0.139*SL
	t_F	0.269	0.122 + 0.074*SL	0.094 + 0.081*SL	0.075 + 0.081*SL
	t_{PLH}	0.238	0.118 + 0.060*SL	0.113 + 0.061*SL	0.111 + 0.062*SL
	t_{PHL}	0.158	0.077 + 0.040*SL	0.082 + 0.039*SL	0.081 + 0.039*SL
D1 to YN	t_R	0.446	0.176 + 0.135*SL	0.160 + 0.139*SL	0.156 + 0.139*SL
	t_F	0.329	0.180 + 0.075*SL	0.156 + 0.081*SL	0.138 + 0.081*SL
	t_{PLH}	0.281	0.156 + 0.062*SL	0.158 + 0.062*SL	0.161 + 0.062*SL
	t_{PHL}	0.212	0.131 + 0.041*SL	0.135 + 0.039*SL	0.140 + 0.039*SL
S to YN	t_R	0.468	0.197 + 0.135*SL	0.183 + 0.139*SL	0.179 + 0.139*SL
	t_F	0.323	0.171 + 0.076*SL	0.153 + 0.081*SL	0.138 + 0.081*SL
	t_{PLH}	0.296	0.172 + 0.062*SL	0.173 + 0.062*SL	0.174 + 0.062*SL
	t_{PHL}	0.198	0.116 + 0.041*SL	0.121 + 0.039*SL	0.126 + 0.039*SL
SN to YN	t_R	0.469	0.202 + 0.133*SL	0.180 + 0.139*SL	0.179 + 0.139*SL
	t_F	0.261	0.111 + 0.075*SL	0.089 + 0.081*SL	0.075 + 0.081*SL
	t_{PLH}	0.252	0.132 + 0.060*SL	0.127 + 0.061*SL	0.123 + 0.062*SL
	t_{PHL}	0.143	0.062 + 0.040*SL	0.067 + 0.039*SL	0.066 + 0.039*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

MX2IA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.322	0.181 + 0.070*SL	0.164 + 0.075*SL	0.153 + 0.075*SL
	t_F	0.216	0.131 + 0.043*SL	0.109 + 0.048*SL	0.081 + 0.049*SL
	t_{PLH}	0.179	0.115 + 0.032*SL	0.111 + 0.033*SL	0.109 + 0.033*SL
	t_{PHL}	0.126	0.075 + 0.026*SL	0.085 + 0.023*SL	0.084 + 0.023*SL
D1 to YN	t_R	0.321	0.179 + 0.071*SL	0.165 + 0.075*SL	0.153 + 0.075*SL
	t_F	0.286	0.196 + 0.045*SL	0.182 + 0.048*SL	0.155 + 0.049*SL
	t_{PLH}	0.221	0.154 + 0.034*SL	0.157 + 0.033*SL	0.160 + 0.033*SL
	t_{PHL}	0.191	0.142 + 0.025*SL	0.146 + 0.024*SL	0.152 + 0.023*SL
S to YN	t_R	0.345	0.202 + 0.072*SL	0.189 + 0.075*SL	0.178 + 0.075*SL
	t_F	0.280	0.189 + 0.046*SL	0.177 + 0.048*SL	0.155 + 0.049*SL
	t_{PLH}	0.238	0.171 + 0.033*SL	0.172 + 0.033*SL	0.174 + 0.033*SL
	t_{PHL}	0.177	0.127 + 0.025*SL	0.132 + 0.024*SL	0.139 + 0.023*SL
SN to YN	t_R	0.347	0.207 + 0.070*SL	0.188 + 0.075*SL	0.178 + 0.075*SL
	t_F	0.207	0.119 + 0.044*SL	0.101 + 0.048*SL	0.081 + 0.049*SL
	t_{PLH}	0.195	0.131 + 0.032*SL	0.127 + 0.033*SL	0.122 + 0.033*SL
	t_{PHL}	0.113	0.063 + 0.025*SL	0.070 + 0.023*SL	0.070 + 0.023*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

MX2ID2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.103	0.069 + 0.017*SL	0.062 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.083	0.051 + 0.016*SL	0.051 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.315	0.294 + 0.011*SL	0.301 + 0.009*SL	0.304 + 0.009*SL
	t_{PHL}	0.252	0.230 + 0.011*SL	0.239 + 0.009*SL	0.246 + 0.009*SL
D1 to YN	t_R	0.103	0.069 + 0.017*SL	0.061 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.084	0.052 + 0.016*SL	0.052 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.354	0.333 + 0.011*SL	0.340 + 0.009*SL	0.343 + 0.009*SL
	t_{PHL}	0.324	0.301 + 0.011*SL	0.311 + 0.009*SL	0.318 + 0.009*SL
S to YN	t_R	0.103	0.069 + 0.017*SL	0.062 + 0.019*SL	0.037 + 0.019*SL
	t_F	0.085	0.053 + 0.016*SL	0.052 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.374	0.353 + 0.011*SL	0.360 + 0.009*SL	0.363 + 0.009*SL
	t_{PHL}	0.309	0.286 + 0.011*SL	0.296 + 0.009*SL	0.303 + 0.009*SL
SN to YN	t_R	0.103	0.070 + 0.017*SL	0.062 + 0.019*SL	0.038 + 0.019*SL
	t_F	0.085	0.054 + 0.015*SL	0.050 + 0.016*SL	0.028 + 0.017*SL
	t_{PLH}	0.336	0.315 + 0.010*SL	0.322 + 0.009*SL	0.325 + 0.009*SL
	t_{PHL}	0.240	0.218 + 0.011*SL	0.228 + 0.009*SL	0.235 + 0.009*SL

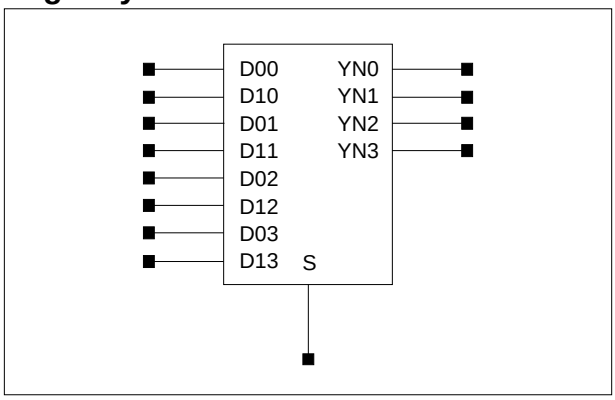
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

MX2ID4A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.107	0.091 + 0.008*SL	0.087 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.089	0.072 + 0.008*SL	0.073 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.364	0.351 + 0.007*SL	0.359 + 0.005*SL	0.373 + 0.004*SL
	t_{PHL}	0.295	0.281 + 0.007*SL	0.290 + 0.005*SL	0.312 + 0.004*SL
D1 to YN	t_R	0.107	0.091 + 0.008*SL	0.087 + 0.009*SL	0.056 + 0.010*SL
	t_F	0.089	0.073 + 0.008*SL	0.074 + 0.008*SL	0.051 + 0.008*SL
	t_{PLH}	0.403	0.389 + 0.007*SL	0.398 + 0.005*SL	0.412 + 0.004*SL
	t_{PHL}	0.368	0.354 + 0.007*SL	0.363 + 0.005*SL	0.384 + 0.004*SL
S to YN	t_R	0.108	0.092 + 0.008*SL	0.088 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.090	0.073 + 0.008*SL	0.075 + 0.008*SL	0.051 + 0.008*SL
	t_{PLH}	0.423	0.410 + 0.007*SL	0.418 + 0.005*SL	0.432 + 0.004*SL
	t_{PHL}	0.353	0.339 + 0.007*SL	0.348 + 0.005*SL	0.369 + 0.004*SL
SN to YN	t_R	0.108	0.091 + 0.008*SL	0.087 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.089	0.072 + 0.008*SL	0.074 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.385	0.372 + 0.007*SL	0.380 + 0.005*SL	0.394 + 0.004*SL
	t_{PHL}	0.284	0.270 + 0.007*SL	0.279 + 0.005*SL	0.300 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

S	YN0	YN1	YN2	YN3
0	$\overline{D00}$	$\overline{D01}$	$\overline{D02}$	$\overline{D03}$
1	$\overline{D10}$	$\overline{D11}$	$\overline{D12}$	$\overline{D13}$

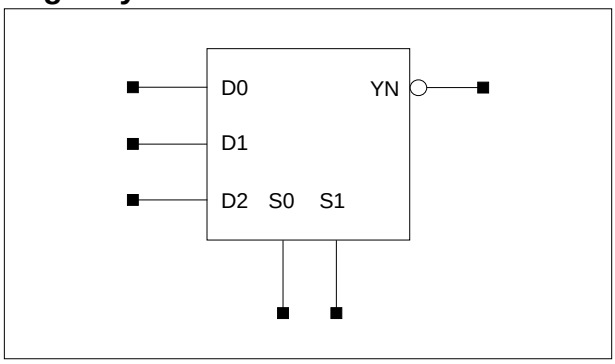
Cell Data

Input Load (SL)									Gate Count
D00	D10	D01	D11	D02	D12	D03	D13	S	
0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	3.7	10.00

MX2IX4 Switching Characteristics (Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to YN0	t_R	0.136	0.064 + 0.036*SL	0.055 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.116	0.054 + 0.031*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.322	0.286 + 0.018*SL	0.289 + 0.017*SL	0.289 + 0.017*SL
	t_{PHL}	0.283	0.245 + 0.019*SL	0.251 + 0.018*SL	0.253 + 0.018*SL
D10 to YN0	t_R	0.136	0.064 + 0.036*SL	0.055 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.116	0.054 + 0.031*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.324	0.288 + 0.018*SL	0.291 + 0.017*SL	0.291 + 0.017*SL
	t_{PHL}	0.284	0.245 + 0.019*SL	0.252 + 0.018*SL	0.253 + 0.018*SL
S to YN0	t_R	0.137	0.064 + 0.036*SL	0.055 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.053 + 0.032*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.425	0.389 + 0.018*SL	0.392 + 0.017*SL	0.392 + 0.017*SL
	t_{PHL}	0.417	0.378 + 0.019*SL	0.385 + 0.018*SL	0.387 + 0.018*SL
D01 to YN1	t_R	0.137	0.064 + 0.036*SL	0.056 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.047 + 0.033*SL	0.035 + 0.034*SL
	t_{PLH}	0.323	0.287 + 0.018*SL	0.290 + 0.017*SL	0.290 + 0.017*SL
	t_{PHL}	0.284	0.246 + 0.019*SL	0.252 + 0.018*SL	0.254 + 0.018*SL
D11 to YN1	t_R	0.137	0.065 + 0.036*SL	0.056 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.047 + 0.033*SL	0.035 + 0.034*SL
	t_{PLH}	0.325	0.288 + 0.018*SL	0.291 + 0.017*SL	0.292 + 0.017*SL
	t_{PHL}	0.284	0.246 + 0.019*SL	0.252 + 0.018*SL	0.254 + 0.018*SL
S to YN1	t_R	0.137	0.065 + 0.036*SL	0.056 + 0.038*SL	0.046 + 0.039*SL
	t_F	0.117	0.053 + 0.032*SL	0.047 + 0.033*SL	0.035 + 0.034*SL
	t_{PLH}	0.426	0.389 + 0.018*SL	0.392 + 0.017*SL	0.393 + 0.017*SL
	t_{PHL}	0.418	0.379 + 0.019*SL	0.385 + 0.018*SL	0.387 + 0.018*SL
D02 to YN2	t_R	0.136	0.064 + 0.036*SL	0.055 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.054 + 0.031*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.322	0.286 + 0.018*SL	0.289 + 0.017*SL	0.289 + 0.017*SL
	t_{PHL}	0.283	0.245 + 0.019*SL	0.251 + 0.018*SL	0.253 + 0.018*SL
D12 to YN2	t_R	0.136	0.064 + 0.036*SL	0.055 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.054 + 0.031*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.324	0.287 + 0.018*SL	0.291 + 0.017*SL	0.291 + 0.017*SL
	t_{PHL}	0.284	0.245 + 0.019*SL	0.251 + 0.018*SL	0.253 + 0.018*SL
S to YN2	t_R	0.136	0.064 + 0.036*SL	0.055 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.053 + 0.031*SL	0.046 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.424	0.388 + 0.018*SL	0.391 + 0.017*SL	0.391 + 0.017*SL
	t_{PHL}	0.416	0.378 + 0.019*SL	0.384 + 0.018*SL	0.386 + 0.018*SL
D03 to YN3	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.053 + 0.031*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.322	0.285 + 0.018*SL	0.288 + 0.017*SL	0.289 + 0.017*SL
	t_{PHL}	0.283	0.244 + 0.019*SL	0.250 + 0.018*SL	0.252 + 0.018*SL
D13 to YN3	t_R	0.136	0.064 + 0.036*SL	0.054 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.116	0.053 + 0.031*SL	0.045 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.323	0.287 + 0.018*SL	0.290 + 0.017*SL	0.290 + 0.017*SL
	t_{PHL}	0.283	0.245 + 0.019*SL	0.251 + 0.018*SL	0.253 + 0.018*SL

Logic Symbol



Truth Table

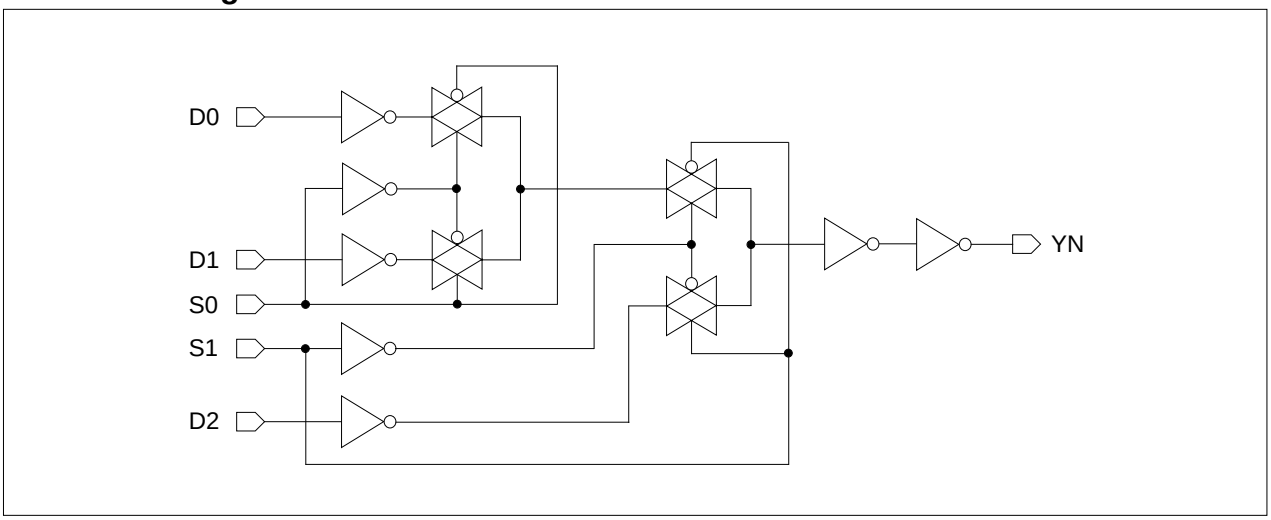
S0	S1	YN
0	0	$\overline{D0}$
1	0	$\overline{D1}$
x	1	$\overline{D2}$

Cell Data

Input Load (SL)														
MX3I					*MX3ID2*					*MX3ID4*				
D0	D1	D2	S0	S1	D0	D1	D2	S0	S1	D0	D1	D2	S0	S1
0.8	0.8	0.8	1.3	1.3	0.8	0.8	0.8	1.3	1.3	0.8	0.8	0.8	1.3	1.3

Gate Count		
MX3I	*MX3ID2*	*MX3ID4*
4.67	5.00	5.67

Schematic Diagram



Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

MX3I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.141	0.071 + 0.035*SL	0.059 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.048 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.393	0.356 + 0.018*SL	0.361 + 0.017*SL	0.360 + 0.017*SL
	t_{PHL}	0.388	0.349 + 0.019*SL	0.356 + 0.018*SL	0.358 + 0.018*SL
D1 to YN	t_R	0.141	0.071 + 0.035*SL	0.059 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.118	0.055 + 0.031*SL	0.048 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.394	0.357 + 0.018*SL	0.361 + 0.017*SL	0.361 + 0.017*SL
	t_{PHL}	0.387	0.348 + 0.019*SL	0.354 + 0.018*SL	0.356 + 0.018*SL
D2 to YN	t_R	0.135	0.063 + 0.036*SL	0.054 + 0.038*SL	0.044 + 0.039*SL
	t_F	0.113	0.049 + 0.032*SL	0.044 + 0.033*SL	0.033 + 0.034*SL
	t_{PLH}	0.300	0.263 + 0.018*SL	0.267 + 0.017*SL	0.267 + 0.017*SL
	t_{PHL}	0.288	0.249 + 0.019*SL	0.255 + 0.018*SL	0.257 + 0.018*SL
S0 to YN	t_R	0.141	0.071 + 0.035*SL	0.058 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.118	0.056 + 0.031*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.380	0.344 + 0.018*SL	0.348 + 0.017*SL	0.347 + 0.017*SL
	t_{PHL}	0.387	0.348 + 0.019*SL	0.355 + 0.018*SL	0.357 + 0.018*SL
S1 to YN	t_R	0.139	0.068 + 0.036*SL	0.057 + 0.038*SL	0.045 + 0.039*SL
	t_F	0.117	0.054 + 0.031*SL	0.047 + 0.033*SL	0.034 + 0.034*SL
	t_{PLH}	0.310	0.273 + 0.018*SL	0.277 + 0.017*SL	0.277 + 0.017*SL
	t_{PHL}	0.311	0.273 + 0.019*SL	0.279 + 0.018*SL	0.281 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

MX3ID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.108	0.075 + 0.017*SL	0.066 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.086	0.054 + 0.016*SL	0.053 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.410	0.388 + 0.011*SL	0.396 + 0.009*SL	0.399 + 0.009*SL
	t_{PHL}	0.394	0.371 + 0.012*SL	0.382 + 0.009*SL	0.389 + 0.009*SL
D1 to YN	t_R	0.108	0.075 + 0.017*SL	0.066 + 0.019*SL	0.036 + 0.020*SL
	t_F	0.087	0.055 + 0.016*SL	0.053 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.410	0.389 + 0.011*SL	0.397 + 0.009*SL	0.400 + 0.009*SL
	t_{PHL}	0.393	0.370 + 0.012*SL	0.380 + 0.009*SL	0.388 + 0.009*SL
D2 to YN	t_R	0.100	0.065 + 0.018*SL	0.059 + 0.019*SL	0.034 + 0.020*SL
	t_F	0.082	0.051 + 0.016*SL	0.047 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.310	0.289 + 0.011*SL	0.297 + 0.009*SL	0.299 + 0.009*SL
	t_{PHL}	0.290	0.267 + 0.011*SL	0.277 + 0.009*SL	0.285 + 0.009*SL
S0 to YN	t_R	0.108	0.073 + 0.017*SL	0.066 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.087	0.055 + 0.016*SL	0.053 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.397	0.375 + 0.011*SL	0.383 + 0.009*SL	0.386 + 0.009*SL
	t_{PHL}	0.393	0.370 + 0.012*SL	0.380 + 0.009*SL	0.388 + 0.009*SL
S1 to YN	t_R	0.106	0.071 + 0.017*SL	0.063 + 0.019*SL	0.035 + 0.020*SL
	t_F	0.086	0.054 + 0.016*SL	0.052 + 0.017*SL	0.026 + 0.017*SL
	t_{PLH}	0.325	0.303 + 0.011*SL	0.311 + 0.009*SL	0.314 + 0.009*SL
	t_{PHL}	0.318	0.295 + 0.012*SL	0.305 + 0.009*SL	0.313 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

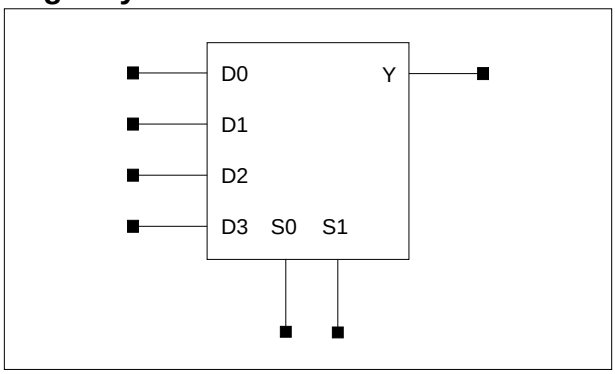
(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

MX3ID4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.116	0.100 + 0.008*SL	0.096 + 0.009*SL	0.061 + 0.010*SL
	t_F	0.093	0.076 + 0.008*SL	0.078 + 0.008*SL	0.053 + 0.008*SL
	t_{PLH}	0.470	0.456 + 0.007*SL	0.465 + 0.005*SL	0.480 + 0.004*SL
	t_{PHL}	0.443	0.428 + 0.007*SL	0.438 + 0.005*SL	0.459 + 0.004*SL
D1 to YN	t_R	0.116	0.100 + 0.008*SL	0.097 + 0.009*SL	0.061 + 0.010*SL
	t_F	0.093	0.077 + 0.008*SL	0.078 + 0.008*SL	0.052 + 0.008*SL
	t_{PLH}	0.470	0.457 + 0.007*SL	0.466 + 0.005*SL	0.481 + 0.004*SL
	t_{PHL}	0.441	0.427 + 0.007*SL	0.436 + 0.005*SL	0.458 + 0.004*SL
D2 to YN	t_R	0.107	0.091 + 0.008*SL	0.086 + 0.009*SL	0.057 + 0.010*SL
	t_F	0.088	0.071 + 0.008*SL	0.073 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.362	0.348 + 0.007*SL	0.357 + 0.005*SL	0.371 + 0.004*SL
	t_{PHL}	0.333	0.319 + 0.007*SL	0.328 + 0.005*SL	0.350 + 0.004*SL
S0 to YN	t_R	0.117	0.101 + 0.008*SL	0.096 + 0.009*SL	0.061 + 0.010*SL
	t_F	0.094	0.077 + 0.008*SL	0.078 + 0.008*SL	0.052 + 0.008*SL
	t_{PLH}	0.457	0.443 + 0.007*SL	0.452 + 0.005*SL	0.467 + 0.004*SL
	t_{PHL}	0.441	0.427 + 0.007*SL	0.437 + 0.005*SL	0.458 + 0.004*SL
S1 to YN	t_R	0.114	0.098 + 0.008*SL	0.093 + 0.009*SL	0.060 + 0.010*SL
	t_F	0.093	0.076 + 0.008*SL	0.078 + 0.008*SL	0.052 + 0.008*SL
	t_{PLH}	0.383	0.370 + 0.007*SL	0.379 + 0.005*SL	0.394 + 0.004*SL
	t_{PHL}	0.366	0.352 + 0.007*SL	0.361 + 0.005*SL	0.383 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

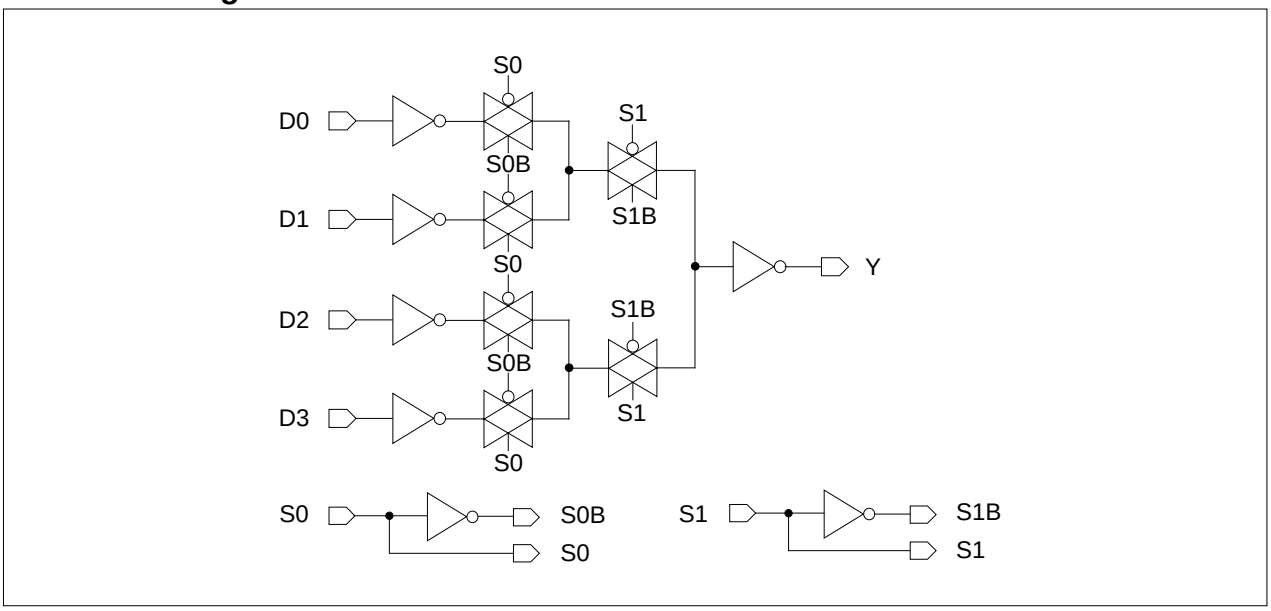
S0	S1	Y
0	0	D0
1	0	D1
0	1	D2
1	1	D3

Cell Data

Input Load (SL)																	
MX4						*MX4D2*						*MX4D4*					
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1
0.8	0.8	0.8	0.9	1.9	1.3	0.8	0.8	0.8	0.9	1.9	1.3	0.8	0.8	0.8	0.9	1.9	1.3

Gate Count		
MX4	*MX4*D2	*MX4*D4
5.67	6.00	6.67

Schematic Diagram



Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

MX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.177	0.103 + 0.037*SL	0.101 + 0.038*SL	0.068 + 0.038*SL
	t_F	0.183	0.113 + 0.035*SL	0.124 + 0.032*SL	0.098 + 0.033*SL
	t_{PLH}	0.335	0.290 + 0.022*SL	0.308 + 0.018*SL	0.323 + 0.017*SL
	t_{PHL}	0.330	0.276 + 0.027*SL	0.308 + 0.019*SL	0.355 + 0.018*SL
D1 to Y	t_R	0.177	0.103 + 0.037*SL	0.101 + 0.038*SL	0.068 + 0.038*SL
	t_F	0.184	0.114 + 0.035*SL	0.124 + 0.032*SL	0.098 + 0.033*SL
	t_{PLH}	0.334	0.289 + 0.022*SL	0.307 + 0.018*SL	0.322 + 0.017*SL
	t_{PHL}	0.331	0.278 + 0.027*SL	0.309 + 0.019*SL	0.356 + 0.018*SL
D2 to Y	t_R	0.177	0.104 + 0.037*SL	0.100 + 0.038*SL	0.067 + 0.038*SL
	t_F	0.182	0.113 + 0.035*SL	0.123 + 0.032*SL	0.096 + 0.033*SL
	t_{PLH}	0.332	0.287 + 0.022*SL	0.305 + 0.018*SL	0.319 + 0.017*SL
	t_{PHL}	0.329	0.275 + 0.027*SL	0.306 + 0.019*SL	0.352 + 0.018*SL
D3 to Y	t_R	0.177	0.105 + 0.036*SL	0.100 + 0.038*SL	0.067 + 0.038*SL
	t_F	0.183	0.114 + 0.035*SL	0.124 + 0.032*SL	0.096 + 0.033*SL
	t_{PLH}	0.332	0.288 + 0.022*SL	0.305 + 0.018*SL	0.320 + 0.017*SL
	t_{PHL}	0.332	0.278 + 0.027*SL	0.309 + 0.019*SL	0.355 + 0.018*SL
S0 to Y	t_R	0.178	0.105 + 0.036*SL	0.101 + 0.038*SL	0.068 + 0.038*SL
	t_F	0.182	0.112 + 0.035*SL	0.123 + 0.032*SL	0.097 + 0.033*SL
	t_{PLH}	0.354	0.309 + 0.022*SL	0.327 + 0.018*SL	0.342 + 0.017*SL
	t_{PHL}	0.339	0.285 + 0.027*SL	0.316 + 0.019*SL	0.363 + 0.018*SL
S1 to Y	t_R	0.168	0.092 + 0.038*SL	0.092 + 0.038*SL	0.066 + 0.038*SL
	t_F	0.164	0.090 + 0.037*SL	0.107 + 0.033*SL	0.090 + 0.033*SL
	t_{PLH}	0.254	0.209 + 0.022*SL	0.227 + 0.018*SL	0.243 + 0.017*SL
	t_{PHL}	0.255	0.202 + 0.026*SL	0.231 + 0.019*SL	0.276 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 36, *Group3 : 36 < SL

Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

MX4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.151	0.115 + 0.018*SL	0.113 + 0.019*SL	0.077 + 0.019*SL
	t_F	0.161	0.121 + 0.020*SL	0.137 + 0.016*SL	0.122 + 0.016*SL
	t_{PLH}	0.348	0.320 + 0.014*SL	0.339 + 0.009*SL	0.376 + 0.009*SL
	t_{PHL}	0.338	0.304 + 0.017*SL	0.332 + 0.010*SL	0.416 + 0.009*SL
D1 to Y	t_R	0.151	0.115 + 0.018*SL	0.113 + 0.019*SL	0.077 + 0.019*SL
	t_F	0.162	0.122 + 0.020*SL	0.137 + 0.016*SL	0.122 + 0.016*SL
	t_{PLH}	0.347	0.319 + 0.014*SL	0.338 + 0.009*SL	0.374 + 0.009*SL
	t_{PHL}	0.340	0.306 + 0.017*SL	0.333 + 0.010*SL	0.417 + 0.009*SL
D2 to Y	t_R	0.151	0.115 + 0.018*SL	0.112 + 0.019*SL	0.076 + 0.019*SL
	t_F	0.161	0.120 + 0.020*SL	0.137 + 0.016*SL	0.120 + 0.016*SL
	t_{PLH}	0.345	0.317 + 0.014*SL	0.336 + 0.009*SL	0.372 + 0.009*SL
	t_{PHL}	0.337	0.303 + 0.017*SL	0.331 + 0.010*SL	0.414 + 0.009*SL
D3 to Y	t_R	0.151	0.115 + 0.018*SL	0.112 + 0.019*SL	0.076 + 0.019*SL
	t_F	0.162	0.121 + 0.020*SL	0.137 + 0.016*SL	0.121 + 0.016*SL
	t_{PLH}	0.346	0.318 + 0.014*SL	0.337 + 0.009*SL	0.372 + 0.009*SL
	t_{PHL}	0.340	0.306 + 0.017*SL	0.334 + 0.010*SL	0.417 + 0.009*SL
S0 to Y	t_R	0.151	0.115 + 0.018*SL	0.113 + 0.019*SL	0.077 + 0.019*SL
	t_F	0.161	0.120 + 0.020*SL	0.137 + 0.016*SL	0.122 + 0.016*SL
	t_{PLH}	0.366	0.338 + 0.014*SL	0.357 + 0.009*SL	0.393 + 0.009*SL
	t_{PHL}	0.347	0.313 + 0.017*SL	0.341 + 0.010*SL	0.424 + 0.009*SL
S1 to Y	t_R	0.145	0.107 + 0.019*SL	0.106 + 0.019*SL	0.075 + 0.019*SL
	t_F	0.146	0.103 + 0.021*SL	0.122 + 0.016*SL	0.116 + 0.017*SL
	t_{PLH}	0.265	0.237 + 0.014*SL	0.256 + 0.009*SL	0.294 + 0.009*SL
	t_{PHL}	0.259	0.224 + 0.017*SL	0.252 + 0.010*SL	0.335 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Switching Characteristics

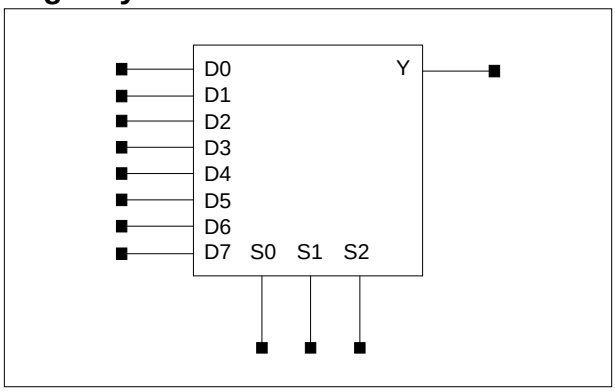
(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

MX4D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.181	0.163 + 0.009*SL	0.163 + 0.009*SL	0.149 + 0.009*SL
	t_F	0.194	0.170 + 0.012*SL	0.184 + 0.008*SL	0.216 + 0.008*SL
	t_{PLH}	0.420	0.401 + 0.009*SL	0.417 + 0.005*SL	0.477 + 0.004*SL
	t_{PHL}	0.413	0.391 + 0.011*SL	0.410 + 0.006*SL	0.505 + 0.005*SL
D1 to Y	t_R	0.181	0.163 + 0.009*SL	0.162 + 0.009*SL	0.149 + 0.009*SL
	t_F	0.194	0.170 + 0.012*SL	0.184 + 0.008*SL	0.216 + 0.008*SL
	t_{PLH}	0.418	0.400 + 0.009*SL	0.416 + 0.005*SL	0.475 + 0.004*SL
	t_{PHL}	0.414	0.393 + 0.011*SL	0.411 + 0.006*SL	0.507 + 0.005*SL
D2 to Y	t_R	0.180	0.163 + 0.009*SL	0.161 + 0.009*SL	0.148 + 0.009*SL
	t_F	0.193	0.169 + 0.012*SL	0.183 + 0.008*SL	0.215 + 0.008*SL
	t_{PLH}	0.416	0.398 + 0.009*SL	0.414 + 0.005*SL	0.473 + 0.004*SL
	t_{PHL}	0.412	0.390 + 0.011*SL	0.409 + 0.006*SL	0.504 + 0.005*SL
D3 to Y	t_R	0.180	0.162 + 0.009*SL	0.161 + 0.009*SL	0.148 + 0.009*SL
	t_F	0.194	0.170 + 0.012*SL	0.184 + 0.008*SL	0.216 + 0.008*SL
	t_{PLH}	0.417	0.398 + 0.009*SL	0.414 + 0.005*SL	0.474 + 0.004*SL
	t_{PHL}	0.415	0.393 + 0.011*SL	0.412 + 0.006*SL	0.507 + 0.005*SL
S0 to Y	t_R	0.181	0.163 + 0.009*SL	0.163 + 0.009*SL	0.149 + 0.009*SL
	t_F	0.193	0.170 + 0.012*SL	0.183 + 0.008*SL	0.216 + 0.008*SL
	t_{PLH}	0.436	0.417 + 0.009*SL	0.433 + 0.005*SL	0.493 + 0.004*SL
	t_{PHL}	0.421	0.400 + 0.011*SL	0.418 + 0.006*SL	0.514 + 0.005*SL
S1 to Y	t_R	0.179	0.161 + 0.009*SL	0.161 + 0.009*SL	0.147 + 0.009*SL
	t_F	0.186	0.162 + 0.012*SL	0.176 + 0.009*SL	0.211 + 0.008*SL
	t_{PLH}	0.333	0.314 + 0.009*SL	0.330 + 0.005*SL	0.391 + 0.004*SL
	t_{PHL}	0.332	0.311 + 0.011*SL	0.329 + 0.006*SL	0.426 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 69, *Group3 : 69 < SL

Logic Symbol



Truth Table

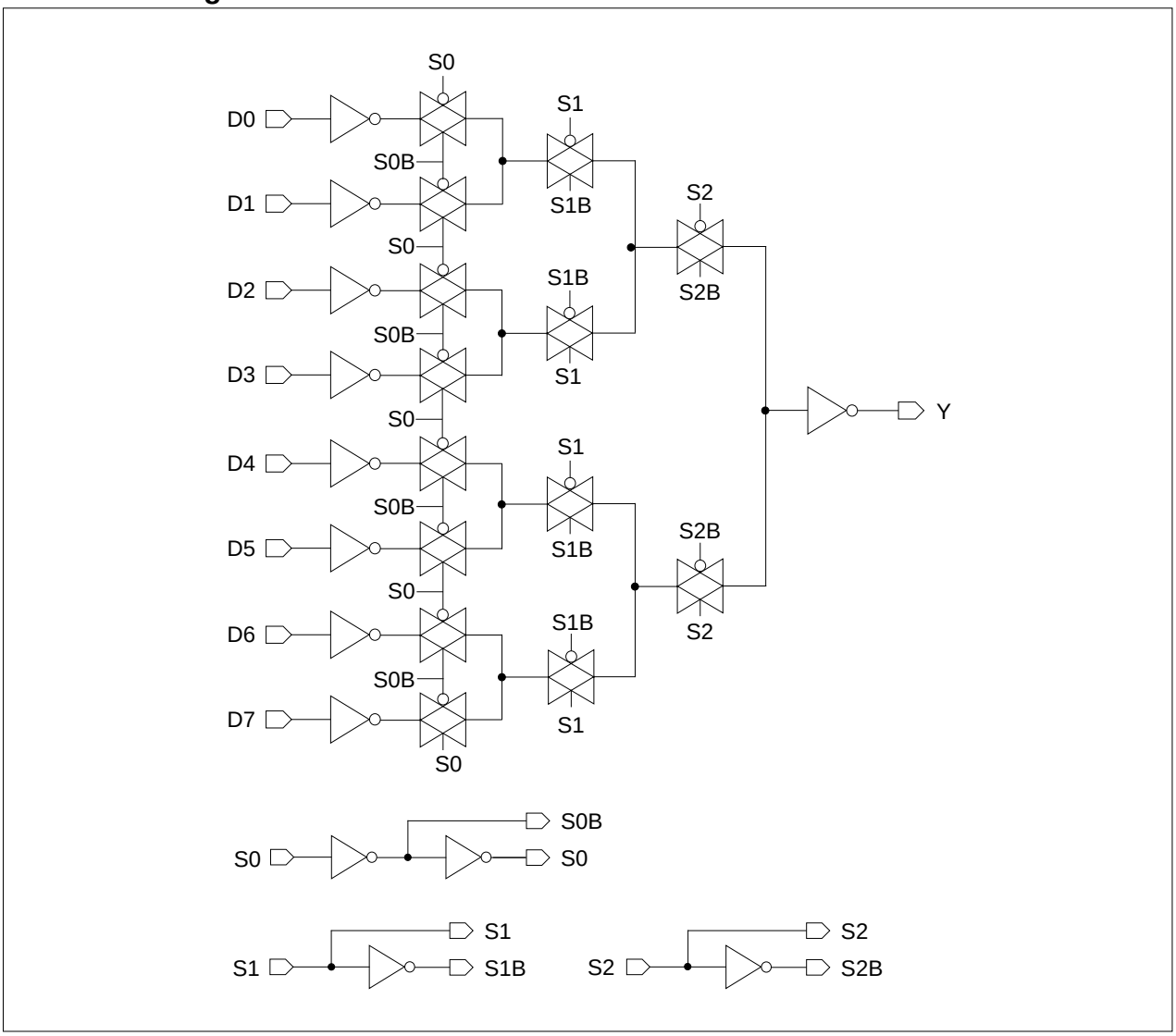
S0	S1	S2	Y
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D7

Cell Data

Input Load (SL)											Gate Count
MX8											*MX8*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.8	0.7	0.7	0.7	0.7	0.8	0.7	0.8	3.1	1.9	1.3	9.67
MX8D2											*MX8D2*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.8	0.7	0.7	0.7	0.7	0.8	0.7	0.8	3.1	1.9	1.3	10.00
MX8D4											*MX8D4*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.8	0.7	0.7	0.7	0.7	0.8	0.7	0.8	3.1	1.9	1.3	10.67

8 > 1 Non-Inverting MUX with 1X/2X/4X Drive

Schematic Diagram



MX8 Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.26ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.221	0.147 + 0.037*SL	0.147 + 0.037*SL	0.109 + 0.038*SL
	t_F	0.246	0.172 + 0.037*SL	0.192 + 0.032*SL	0.180 + 0.032*SL
	t_{PLH}	0.485	0.434 + 0.025*SL	0.461 + 0.019*SL	0.500 + 0.017*SL
	t_{PHL}	0.496	0.434 + 0.031*SL	0.477 + 0.020*SL	0.568 + 0.018*SL
D1 to Y	t_R	0.221	0.147 + 0.037*SL	0.147 + 0.037*SL	0.109 + 0.038*SL
	t_F	0.247	0.172 + 0.037*SL	0.193 + 0.032*SL	0.180 + 0.032*SL
	t_{PLH}	0.483	0.433 + 0.025*SL	0.459 + 0.019*SL	0.498 + 0.017*SL
	t_{PHL}	0.498	0.435 + 0.031*SL	0.479 + 0.020*SL	0.570 + 0.018*SL
D2 to Y	t_R	0.221	0.147 + 0.037*SL	0.146 + 0.037*SL	0.109 + 0.038*SL
	t_F	0.245	0.171 + 0.037*SL	0.192 + 0.032*SL	0.179 + 0.032*SL
	t_{PLH}	0.481	0.431 + 0.025*SL	0.457 + 0.019*SL	0.496 + 0.017*SL
	t_{PHL}	0.494	0.432 + 0.031*SL	0.475 + 0.020*SL	0.566 + 0.018*SL
D3 to Y	t_R	0.221	0.147 + 0.037*SL	0.146 + 0.037*SL	0.109 + 0.038*SL
	t_F	0.246	0.171 + 0.037*SL	0.192 + 0.032*SL	0.180 + 0.032*SL
	t_{PLH}	0.480	0.430 + 0.025*SL	0.456 + 0.019*SL	0.495 + 0.017*SL
	t_{PHL}	0.496	0.433 + 0.031*SL	0.476 + 0.020*SL	0.567 + 0.018*SL
D4 to Y	t_R	0.220	0.146 + 0.037*SL	0.146 + 0.037*SL	0.108 + 0.038*SL
	t_F	0.244	0.170 + 0.037*SL	0.190 + 0.032*SL	0.178 + 0.032*SL
	t_{PLH}	0.476	0.426 + 0.025*SL	0.452 + 0.018*SL	0.490 + 0.017*SL
	t_{PHL}	0.488	0.426 + 0.031*SL	0.469 + 0.020*SL	0.559 + 0.018*SL
D5 to Y	t_R	0.220	0.146 + 0.037*SL	0.146 + 0.037*SL	0.108 + 0.038*SL
	t_F	0.244	0.170 + 0.037*SL	0.190 + 0.032*SL	0.178 + 0.032*SL
	t_{PLH}	0.475	0.425 + 0.025*SL	0.452 + 0.018*SL	0.489 + 0.017*SL
	t_{PHL}	0.490	0.427 + 0.031*SL	0.471 + 0.020*SL	0.561 + 0.018*SL
D6 to Y	t_R	0.220	0.146 + 0.037*SL	0.146 + 0.037*SL	0.108 + 0.038*SL
	t_F	0.244	0.170 + 0.037*SL	0.190 + 0.032*SL	0.178 + 0.032*SL
	t_{PLH}	0.474	0.424 + 0.025*SL	0.450 + 0.018*SL	0.488 + 0.017*SL
	t_{PHL}	0.488	0.425 + 0.031*SL	0.468 + 0.020*SL	0.558 + 0.018*SL
D7 to Y	t_R	0.220	0.145 + 0.037*SL	0.146 + 0.037*SL	0.108 + 0.038*SL
	t_F	0.244	0.170 + 0.037*SL	0.190 + 0.032*SL	0.178 + 0.032*SL
	t_{PLH}	0.473	0.423 + 0.025*SL	0.450 + 0.018*SL	0.487 + 0.017*SL
	t_{PHL}	0.489	0.427 + 0.031*SL	0.470 + 0.020*SL	0.560 + 0.018*SL
S0 to Y	t_R	0.220	0.145 + 0.037*SL	0.146 + 0.037*SL	0.108 + 0.038*SL
	t_F	0.244	0.169 + 0.037*SL	0.190 + 0.032*SL	0.178 + 0.032*SL
	t_{PLH}	0.615	0.565 + 0.025*SL	0.591 + 0.018*SL	0.629 + 0.017*SL
	t_{PHL}	0.594	0.532 + 0.031*SL	0.575 + 0.020*SL	0.665 + 0.018*SL
S1 to Y	t_R	0.213	0.138 + 0.037*SL	0.140 + 0.037*SL	0.105 + 0.038*SL
	t_F	0.225	0.148 + 0.039*SL	0.173 + 0.032*SL	0.170 + 0.032*SL
	t_{PLH}	0.397	0.346 + 0.025*SL	0.373 + 0.019*SL	0.411 + 0.017*SL
	t_{PHL}	0.368	0.306 + 0.031*SL	0.349 + 0.020*SL	0.439 + 0.018*SL
S2 to Y	t_R	0.188	0.108 + 0.040*SL	0.117 + 0.038*SL	0.099 + 0.038*SL
	t_F	0.180	0.100 + 0.040*SL	0.127 + 0.033*SL	0.145 + 0.033*SL
	t_{PLH}	0.273	0.223 + 0.025*SL	0.249 + 0.019*SL	0.288 + 0.017*SL
	t_{PHL}	0.264	0.206 + 0.029*SL	0.240 + 0.020*SL	0.321 + 0.018*SL

MX8D2 Switching Characteristics(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.200	0.162 + 0.019*SL	0.164 + 0.019*SL	0.129 + 0.019*SL
	t_F	0.228	0.183 + 0.023*SL	0.208 + 0.016*SL	0.218 + 0.016*SL
	t_{PLH}	0.507	0.474 + 0.016*SL	0.501 + 0.010*SL	0.569 + 0.009*SL
	t_{PHL}	0.518	0.478 + 0.020*SL	0.514 + 0.011*SL	0.646 + 0.009*SL
D1 to Y	t_R	0.200	0.162 + 0.019*SL	0.163 + 0.019*SL	0.129 + 0.019*SL
	t_F	0.228	0.183 + 0.023*SL	0.208 + 0.016*SL	0.218 + 0.016*SL
	t_{PLH}	0.505	0.472 + 0.016*SL	0.499 + 0.010*SL	0.567 + 0.009*SL
	t_{PHL}	0.520	0.480 + 0.020*SL	0.516 + 0.011*SL	0.648 + 0.009*SL
D2 to Y	t_R	0.199	0.161 + 0.019*SL	0.162 + 0.019*SL	0.128 + 0.019*SL
	t_F	0.228	0.183 + 0.022*SL	0.207 + 0.016*SL	0.217 + 0.016*SL
	t_{PLH}	0.503	0.470 + 0.016*SL	0.497 + 0.010*SL	0.565 + 0.009*SL
	t_{PHL}	0.516	0.477 + 0.020*SL	0.512 + 0.011*SL	0.644 + 0.009*SL
D3 to Y	t_R	0.199	0.161 + 0.019*SL	0.162 + 0.019*SL	0.128 + 0.019*SL
	t_F	0.228	0.183 + 0.022*SL	0.207 + 0.016*SL	0.217 + 0.016*SL
	t_{PLH}	0.502	0.469 + 0.016*SL	0.496 + 0.010*SL	0.564 + 0.009*SL
	t_{PHL}	0.518	0.478 + 0.020*SL	0.513 + 0.011*SL	0.646 + 0.009*SL
D4 to Y	t_R	0.198	0.159 + 0.019*SL	0.162 + 0.019*SL	0.127 + 0.019*SL
	t_F	0.226	0.182 + 0.022*SL	0.205 + 0.016*SL	0.215 + 0.016*SL
	t_{PLH}	0.497	0.464 + 0.016*SL	0.491 + 0.010*SL	0.558 + 0.009*SL
	t_{PHL}	0.510	0.471 + 0.020*SL	0.505 + 0.011*SL	0.637 + 0.009*SL
D5 to Y	t_R	0.198	0.159 + 0.019*SL	0.162 + 0.019*SL	0.126 + 0.019*SL
	t_F	0.226	0.182 + 0.022*SL	0.205 + 0.016*SL	0.215 + 0.016*SL
	t_{PLH}	0.497	0.464 + 0.016*SL	0.491 + 0.010*SL	0.558 + 0.009*SL
	t_{PHL}	0.512	0.472 + 0.020*SL	0.507 + 0.011*SL	0.639 + 0.009*SL
D6 to Y	t_R	0.198	0.160 + 0.019*SL	0.162 + 0.019*SL	0.126 + 0.019*SL
	t_F	0.226	0.181 + 0.022*SL	0.206 + 0.016*SL	0.215 + 0.016*SL
	t_{PLH}	0.495	0.462 + 0.016*SL	0.489 + 0.010*SL	0.556 + 0.009*SL
	t_{PHL}	0.509	0.470 + 0.020*SL	0.505 + 0.011*SL	0.636 + 0.009*SL
D7 to Y	t_R	0.198	0.160 + 0.019*SL	0.162 + 0.019*SL	0.126 + 0.019*SL
	t_F	0.226	0.182 + 0.022*SL	0.205 + 0.016*SL	0.215 + 0.016*SL
	t_{PLH}	0.495	0.462 + 0.016*SL	0.489 + 0.010*SL	0.555 + 0.009*SL
	t_{PHL}	0.511	0.471 + 0.020*SL	0.506 + 0.011*SL	0.638 + 0.009*SL
S0 to Y	t_R	0.199	0.161 + 0.019*SL	0.163 + 0.019*SL	0.127 + 0.019*SL
	t_F	0.226	0.182 + 0.022*SL	0.205 + 0.016*SL	0.215 + 0.016*SL
	t_{PLH}	0.636	0.603 + 0.016*SL	0.630 + 0.010*SL	0.697 + 0.009*SL
	t_{PHL}	0.615	0.576 + 0.020*SL	0.611 + 0.011*SL	0.743 + 0.009*SL
S1 to Y	t_R	0.194	0.156 + 0.019*SL	0.158 + 0.019*SL	0.125 + 0.019*SL
	t_F	0.213	0.168 + 0.022*SL	0.192 + 0.016*SL	0.209 + 0.016*SL
	t_{PLH}	0.417	0.384 + 0.016*SL	0.411 + 0.010*SL	0.478 + 0.009*SL
	t_{PHL}	0.383	0.343 + 0.020*SL	0.379 + 0.011*SL	0.512 + 0.009*SL
S2 to Y	t_R	0.175	0.135 + 0.020*SL	0.139 + 0.019*SL	0.120 + 0.019*SL
	t_F	0.168	0.121 + 0.024*SL	0.148 + 0.017*SL	0.188 + 0.016*SL
	t_{PLH}	0.291	0.258 + 0.016*SL	0.284 + 0.010*SL	0.355 + 0.009*SL
	t_{PHL}	0.270	0.232 + 0.019*SL	0.265 + 0.011*SL	0.392 + 0.009*SL

MX8D4 Switching Characteristics(Typical process, 25°C, 3.3 V, t_R/t_F = 0.26 ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.243	0.225 + 0.009*SL	0.224 + 0.009*SL	0.220 + 0.009*SL
	t_F	0.274	0.249 + 0.012*SL	0.264 + 0.009*SL	0.319 + 0.008*SL
	t_{PLH}	0.603	0.581 + 0.011*SL	0.601 + 0.006*SL	0.682 + 0.005*SL
	t_{PHL}	0.630	0.605 + 0.012*SL	0.626 + 0.007*SL	0.747 + 0.005*SL
D1 to Y	t_R	0.243	0.224 + 0.009*SL	0.224 + 0.009*SL	0.220 + 0.009*SL
	t_F	0.275	0.250 + 0.012*SL	0.264 + 0.009*SL	0.320 + 0.008*SL
	t_{PLH}	0.601	0.580 + 0.011*SL	0.599 + 0.006*SL	0.680 + 0.005*SL
	t_{PHL}	0.632	0.607 + 0.012*SL	0.628 + 0.007*SL	0.749 + 0.005*SL
D2 to Y	t_R	0.242	0.224 + 0.009*SL	0.224 + 0.009*SL	0.220 + 0.009*SL
	t_F	0.273	0.248 + 0.012*SL	0.263 + 0.009*SL	0.319 + 0.008*SL
	t_{PLH}	0.599	0.577 + 0.011*SL	0.597 + 0.006*SL	0.678 + 0.005*SL
	t_{PHL}	0.628	0.603 + 0.012*SL	0.625 + 0.007*SL	0.745 + 0.005*SL
D3 to Y	t_R	0.242	0.224 + 0.009*SL	0.224 + 0.009*SL	0.220 + 0.009*SL
	t_F	0.274	0.249 + 0.012*SL	0.263 + 0.009*SL	0.319 + 0.008*SL
	t_{PLH}	0.598	0.576 + 0.011*SL	0.596 + 0.006*SL	0.677 + 0.005*SL
	t_{PHL}	0.629	0.605 + 0.012*SL	0.626 + 0.007*SL	0.746 + 0.005*SL
D4 to Y	t_R	0.241	0.222 + 0.009*SL	0.222 + 0.009*SL	0.218 + 0.009*SL
	t_F	0.272	0.247 + 0.013*SL	0.262 + 0.009*SL	0.317 + 0.008*SL
	t_{PLH}	0.592	0.570 + 0.011*SL	0.590 + 0.006*SL	0.670 + 0.005*SL
	t_{PHL}	0.620	0.595 + 0.012*SL	0.617 + 0.007*SL	0.737 + 0.005*SL
D5 to Y	t_R	0.241	0.222 + 0.009*SL	0.222 + 0.009*SL	0.218 + 0.009*SL
	t_F	0.272	0.246 + 0.013*SL	0.262 + 0.009*SL	0.317 + 0.008*SL
	t_{PLH}	0.591	0.570 + 0.011*SL	0.590 + 0.006*SL	0.670 + 0.005*SL
	t_{PHL}	0.622	0.597 + 0.012*SL	0.619 + 0.007*SL	0.738 + 0.005*SL
D6 to Y	t_R	0.240	0.223 + 0.009*SL	0.221 + 0.009*SL	0.218 + 0.009*SL
	t_F	0.272	0.247 + 0.013*SL	0.262 + 0.009*SL	0.317 + 0.008*SL
	t_{PLH}	0.590	0.568 + 0.011*SL	0.588 + 0.006*SL	0.668 + 0.005*SL
	t_{PHL}	0.619	0.595 + 0.012*SL	0.616 + 0.007*SL	0.736 + 0.005*SL
D7 to Y	t_R	0.240	0.222 + 0.009*SL	0.221 + 0.009*SL	0.218 + 0.009*SL
	t_F	0.272	0.247 + 0.013*SL	0.262 + 0.009*SL	0.317 + 0.008*SL
	t_{PLH}	0.589	0.568 + 0.011*SL	0.588 + 0.006*SL	0.668 + 0.005*SL
	t_{PHL}	0.621	0.596 + 0.012*SL	0.618 + 0.007*SL	0.738 + 0.005*SL
S0 to Y	t_R	0.241	0.223 + 0.009*SL	0.221 + 0.009*SL	0.218 + 0.009*SL
	t_F	0.272	0.246 + 0.013*SL	0.262 + 0.009*SL	0.317 + 0.008*SL
	t_{PLH}	0.731	0.709 + 0.011*SL	0.729 + 0.006*SL	0.809 + 0.005*SL
	t_{PHL}	0.725	0.701 + 0.012*SL	0.722 + 0.007*SL	0.842 + 0.005*SL
S1 to Y	t_R	0.238	0.220 + 0.009*SL	0.220 + 0.009*SL	0.216 + 0.009*SL
	t_F	0.263	0.238 + 0.013*SL	0.253 + 0.009*SL	0.309 + 0.008*SL
	t_{PLH}	0.510	0.488 + 0.011*SL	0.508 + 0.006*SL	0.588 + 0.005*SL
	t_{PHL}	0.490	0.465 + 0.012*SL	0.486 + 0.007*SL	0.608 + 0.005*SL
S2 to Y	t_R	0.234	0.216 + 0.009*SL	0.215 + 0.009*SL	0.213 + 0.009*SL
	t_F	0.237	0.211 + 0.013*SL	0.226 + 0.009*SL	0.291 + 0.008*SL
	t_{PLH}	0.382	0.361 + 0.011*SL	0.380 + 0.006*SL	0.463 + 0.005*SL
	t_{PHL}	0.361	0.336 + 0.012*SL	0.357 + 0.007*SL	0.480 + 0.005*SL

Input/Output Cells

4

Contents

OVERVIEW

The fourth chapter describes various kinds of Input/Output cells only (3.3V / 5V-tolerant) in STD90/MDL90 library.

The switching characteristics of each cell are attached to its basic cell information. The AC characteristics of bi-directional buffers are not included in this data sheet. However, they can be derived from different combinations of input and output buffers.

There are so many possible combinations of input/output cells, therefore, the naming conventions are adopted to help you memorize and use this cell library efficiently. You can refer to the naming conventions contained in “Summary Tables” section.

The “Summary Tables” section shows the list of 3.3V and 5V-tolerant I/O cells separated by the category (input, output, bi-directional, etc.), and the more detailed description tables can be found on the leading part of each category.

All 3.3V-interface buffers use 1 I/O slot that is 314 x 70μm^2 and all 5V-tolerant interface buffers have the size of 314 x 82.9μm^2.

The default size of a regular I/O buffer is 314 x 70μm^2. All 3.3V-interface buffers use this regular I/O slot if the data sheet do not state differently. All 5V-tolerant buffers use a special size of 314 x 82.9μm^2 if not specified differently in their datasheet.

SUMMARY TABLES

Input Buffers

Cell Type	Cell Name	Page
LVCMOS Level	PIC/PICD/PICU	4-8
	PTIC/PTICD/PTICU	
LVCMOS Schmitt Trigger Level	PIS/PISD/PISU	4-11
	PTIS/PTISD/PTISU	

<Naming Convention of Input Buffers>

Pvlab					
v		**a**		**b**	
None	Normal operation	C	LVCMOS level	None	No resistor
T	5V-tolerant	S	Schmitt trigger level	D	Pull-down resistor
				U	Pull-up resistor

Output Buffers

Cell Type	Cell Name	Current Drive (mA)	Page
Normal	POBy	1/2/4/8/12/16/20/24	4-15
	POBySM	4/8/12/16/20/24	
	POBySH	12/16/20/24	
Open Drain	PODy	1/2/4/8/12/16/20/24	4-21
	PODySM	4/8/12/16/20/24	
	PODySH	12/16/20/24	
	PTODy	1/2/4/6	
	PTODySM	4/6	
Tri-State	POTy	1/2/4/8/12/16/20/24	4-30
	POTySM	4/8/12/16/20/24	
	POTySH	12/16/20/24	
	PTOTy	1/2/4/6	
	PTOTySM	4/6	

<Naming Convention of Output Buffers>

P O x y z			
None	Normal operation	**y**	
x		1	1mA drive
B	Normal buffer	2	2mA drive
D	Open drain buffer	4	4mA drive
T	Tri-state buffer	8	8mA drive
z		12	12mA drive
None	No slew-rate control	16	16mA drive
SM	Medium slew-rate control	20	20mA drive
SH	High slew-rate control	24	24mA drive
P T O x y z			
T	5V-tolerant		
x		**y**	
D	Open drain buffer	1	1mA drive
T	Tri-state buffer	2	2mA drive
z		4	4mA drive
None	No slew-rate control	6	6mA drive
SM	Medium slew-rate control		

Bi-Directional Buffers

Cell Type	Cell Name	Page
Open Drain	PBaDyz/PBaUDyz	4-44
	PTBaDyz/PTBaUDyz	
Tri-State	PBaTyz/PBaDTyz/PBaUTyz	
	PTBaTyz/PTBaDTyz/PTBaUTyz	

<Naming Convention of Bi-Directional Buffers>

P B a b x y z			
a		**y**	
C	LVCMOS level	1	1mA drive
S	LVCMOS schmitt trigger level	2	2mA drive
b		4	4mA drive
None	No resistor	8	8mA drive
D	Pull-down resistor	12	12mA drive
U	Pull-up resistor	16	16mA drive
x		20	20mA drive
D	Open drain buffer	24	24mA drive
T	Tri-state buffer	**z**	
		None	No slew-rate control
		SM	Medium slew -rate control
		SH	High slew-rate control
P T B a b x y z			
a		**y**	
C	LVCMOS level	1	1mA drive
S	LVCMOS schmitt trigger level	2	2mA drive
b		4	4mA drive
None	No resistor	6	6mA drive
D	Pull-down resistor	**z**	
U	Pull-up resistor	None	No slew-rate control
x		SM	Medium slew-rate control
D	Open drain buffer		
T	Tri-state buffer		

Input Clock Drivers with PAD

Cell Type	Cell Name	Current Drive (mA)	Page
LVCMOS level	PSCKDCaby	2/4/6/8/12	4-46
LVCMOS schmitt trigger level	PSCKDSaby	2/4/6/8/12	4-51

<Naming Convention of Input Clock Drivers>

PSCKD a b y			
a		**y**	
C	LVCMOS level	2	2mA drive
S	LVCMOS schmitt trigger level	4	4mA drive
b		6	6mA drive
None	No resistor	8	8mA drive
D	Pull-down resistor	12	12mA drive
U	Pull-up resistor		

Oscillators

Cell Type	Cell Name	Page
Oscillator	PSOSCK(1/2)	4-57
	PSOSCK(17/27)	4-60
	PSOSCM(1/2/3)	4-63
	PSOSCM(16/26/36)	4-67

PCI Buffers

Cell Type	Cell Name	Page
PCI Input	PIPCI	4-73
PCI Output	POPCI	4-74
PCI Bi-Directional	PBPCI	4-75
5V-tolerant PCI Input	PTIPCI	4-76
5V-tolerant PCI Input	PTOPCI	4-77
5V-tolerant PCI Bi-Directional	PTBPCI	4-78

USB (Universal Serial Bus) I/O Buffers

Cell Type	Cell Name	Page
Bidirectional USB Buffer	PBUSB/PBUSB1	4-81

Power Pads

Cell Type	Cell Name	Page
3.3V VDD	VDD3(I/P/O/IP/OP/T)	4-88
VSS	VSS(I/P/O/IP/OP/T)	

Analog Interface

Cell Type	Cell Name	Page
VDD Power Pad	VDDA	4-89
	VDDD	
VSS Power Pads	VSSD	
	VSSA	
	VBBA	
Analog Input with Separated Bulk-Bias	PIA_BB	
	PIAR10_BB	
	PIAR50_BB	
	PIC_BB	
	PICC_BB	
Analog Output with Separated Bulk-Bias	POA_BB	
	POAR50_BB	
	POT2_BB	
	POT4_BB	
	POT12_BB	

Cell List

Cell Name	Function Description
PIC/PICD/PICU	3.3V LVCMOS level input buffers
PIS/PISD/PISU	3.3V LVCMOS schmitt trigger level input buffers
PTIC/PTICD/PTICU	5V-tolerant LVCMOS level input buffer
PTIS/PTISD/PTISU	5V-tolerant LVCMOS schmitt trigger level input buffers

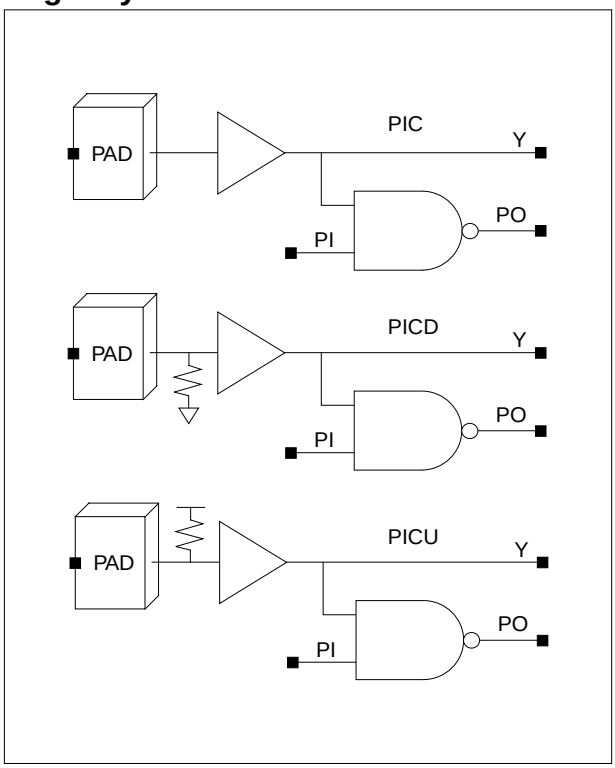
PvIC/PvICD/PvICU

LVCMOS Level Input Buffers

Cell Availability

3.3V Only	5V - tolerant
PIC/PICD/PICU	PTIC/PTICD/PTICU Note1

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
PIC/PICD/PICU	3.417
PTIC/PTICD/PTICU	3.417

NOTES:

1. 5V-tolerant input buffers have 0.2V hysterisis.
2. Fail-safe input buffers are available to receive signals from 5V devices without reducing reliability. However, if you want to use fail-safe input buffers, please contact to SEC ASIC first.

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.60ns, SL: Standard Load)

PIC

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.192	0.174 + 0.009*SL	0.173 + 0.009*SL	0.144 + 0.010*SL
	t_F	0.191	0.176 + 0.007*SL	0.176 + 0.007*SL	0.151 + 0.008*SL
	t_{PLH}	0.229	0.217 + 0.006*SL	0.221 + 0.005*SL	0.231 + 0.005*SL
	t_{PHL}	0.580	0.567 + 0.007*SL	0.572 + 0.005*SL	0.592 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 37, *Group3 : 37 < SL

PICD

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.192	0.174 + 0.009*SL	0.173 + 0.009*SL	0.142 + 0.010*SL
	t_F	0.191	0.176 + 0.007*SL	0.176 + 0.007*SL	0.152 + 0.008*SL
	t_{PLH}	0.240	0.228 + 0.006*SL	0.232 + 0.005*SL	0.241 + 0.005*SL
	t_{PHL}	0.587	0.574 + 0.007*SL	0.579 + 0.005*SL	0.598 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 37, *Group3 : 37 < SL

PICU

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.194	0.176 + 0.009*SL	0.174 + 0.009*SL	0.145 + 0.010*SL
	t_F	0.190	0.175 + 0.007*SL	0.175 + 0.007*SL	0.153 + 0.008*SL
	t_{PLH}	0.229	0.216 + 0.006*SL	0.220 + 0.005*SL	0.230 + 0.005*SL
	t_{PHL}	0.593	0.580 + 0.007*SL	0.585 + 0.005*SL	0.605 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 37, *Group3 : 37 < SL

NOTE: The delay measure point of LVCMOS input buffer is from PAD(VDD/2) to Y(VDD/2).

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.60ns, SL: Standard Load)

PTIC

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.139	0.117 + 0.011*SL	0.120 + 0.010*SL	0.103 + 0.010*SL
	t_F	0.122	0.105 + 0.009*SL	0.106 + 0.008*SL	0.097 + 0.008*SL
	t_{PLH}	0.796	0.785 + 0.006*SL	0.787 + 0.005*SL	0.792 + 0.005*SL
	t_{PHL}	1.050	1.038 + 0.006*SL	1.042 + 0.005*SL	1.055 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 37, *Group3 : 37 < SL

PTICD

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.138	0.117 + 0.010*SL	0.119 + 0.010*SL	0.103 + 0.010*SL
	t_F	0.122	0.105 + 0.008*SL	0.106 + 0.008*SL	0.097 + 0.008*SL
	t_{PLH}	0.805	0.794 + 0.006*SL	0.796 + 0.005*SL	0.801 + 0.005*SL
	t_{PHL}	1.059	1.047 + 0.006*SL	1.051 + 0.005*SL	1.063 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 37, *Group3 : 37 < SL

PTICU

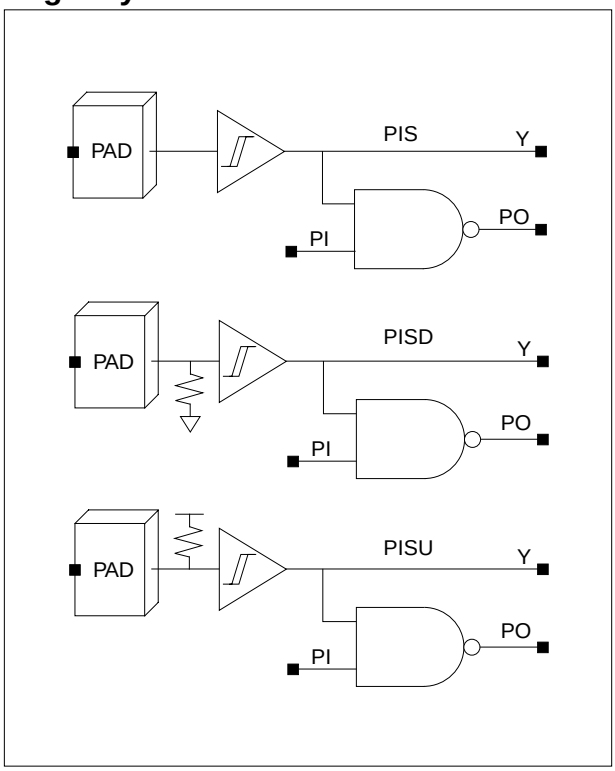
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.138	0.117 + 0.011*SL	0.119 + 0.010*SL	0.103 + 0.010*SL
	t_F	0.122	0.103 + 0.009*SL	0.107 + 0.008*SL	0.097 + 0.008*SL
	t_{PLH}	0.801	0.789 + 0.006*SL	0.792 + 0.005*SL	0.796 + 0.005*SL
	t_{PHL}	1.066	1.054 + 0.006*SL	1.058 + 0.005*SL	1.070 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 37, *Group3 : 37 < SL

Cell Availability

Only 3.3V	5V - tolerant
PIS/PISD/PISU	PTIS/PTISD/PTISU

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
PIS/PISD/PISU	3.417
PTIS/PTISD/PTISU	3.417

NOTE: Fail-safe input buffers are available to receive signals from 5V devices without reducing reliability. However, if you want to use fail-safe input buffers, please contact to SEC ASIC first.

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.60ns, SL: Standard Load)

PIS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.173	0.153 + 0.010*SL	0.154 + 0.010*SL	0.132 + 0.010*SL
	t_F	0.197	0.182 + 0.008*SL	0.182 + 0.007*SL	0.165 + 0.008*SL
	t_{PLH}	0.544	0.532 + 0.006*SL	0.535 + 0.005*SL	0.546 + 0.005*SL
	t_{PHL}	0.580	0.566 + 0.007*SL	0.572 + 0.005*SL	0.596 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 37, *Group3 : 37 < SL

PISD

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.172	0.153 + 0.010*SL	0.153 + 0.010*SL	0.132 + 0.010*SL
	t_F	0.197	0.183 + 0.007*SL	0.182 + 0.007*SL	0.166 + 0.008*SL
	t_{PLH}	0.552	0.539 + 0.006*SL	0.543 + 0.005*SL	0.553 + 0.005*SL
	t_{PHL}	0.588	0.574 + 0.007*SL	0.579 + 0.005*SL	0.604 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 37, *Group3 : 37 < SL

PISU

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.173	0.154 + 0.010*SL	0.154 + 0.010*SL	0.133 + 0.010*SL
	t_F	0.197	0.182 + 0.007*SL	0.182 + 0.007*SL	0.165 + 0.008*SL
	t_{PLH}	0.548	0.535 + 0.006*SL	0.539 + 0.005*SL	0.549 + 0.005*SL
	t_{PHL}	0.592	0.578 + 0.007*SL	0.584 + 0.005*SL	0.608 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 37, *Group3 : 37 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.60ns, SL: Standard Load)

PTIS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.138	0.117 + 0.011*SL	0.119 + 0.010*SL	0.103 + 0.010*SL
	t_F	0.123	0.104 + 0.009*SL	0.108 + 0.008*SL	0.098 + 0.008*SL
	t_{PLH}	0.830	0.819 + 0.006*SL	0.821 + 0.005*SL	0.826 + 0.005*SL
	t_{PHL}	0.838	0.826 + 0.006*SL	0.830 + 0.005*SL	0.843 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 37, *Group3 : 37 < SL

PTISD

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.139	0.117 + 0.011*SL	0.120 + 0.010*SL	0.103 + 0.010*SL
	t_F	0.123	0.106 + 0.008*SL	0.107 + 0.008*SL	0.098 + 0.008*SL
	t_{PLH}	0.838	0.826 + 0.006*SL	0.829 + 0.005*SL	0.833 + 0.005*SL
	t_{PHL}	0.847	0.835 + 0.006*SL	0.839 + 0.005*SL	0.851 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 37, *Group3 : 37 < SL

PTISU

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.138	0.117 + 0.011*SL	0.119 + 0.010*SL	0.103 + 0.010*SL
	t_F	0.123	0.106 + 0.009*SL	0.108 + 0.008*SL	0.098 + 0.008*SL
	t_{PLH}	0.838	0.827 + 0.006*SL	0.829 + 0.005*SL	0.834 + 0.005*SL
	t_{PHL}	0.858	0.846 + 0.006*SL	0.850 + 0.005*SL	0.862 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 37, *Group3 : 37 < SL

OUTPUT BUFFERS

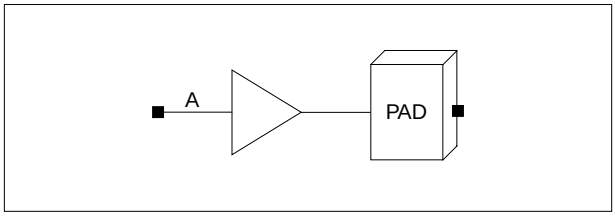
Cell List

Cell Name	Function Description
POB(1/2/4/8/12/16/20/24)	LVCMOS Normal Output Buffers
POB(4/8/12/16/20/24)SM	LVCMOS Normal Output Buffers with Medium Slew-Rate
POB(12/16/20/24)SH	LVCMOS Normal Output Buffers with High Slew-Rate
POD(1/2/4/8/12/16/20/24)	LVCMOS Open Drain Output Buffers
POD(4/8/12/16/20/24)SM	LVCMOS Open Drain Output Buffers with Medium Slew-Rate
POD(12/16/20/24)SH	LVCMOS Open Drain Output Buffers with High Slew-Rate
POT(1/2/4/8/12/16/20/24)	LVCMOS Tri-State Output Buffers
POT(4/8/12/16/20/24)SM	LVCMOS Tri-State Output Buffers with Medium Slew-Rate
POT(12/16/20/24)SH	LVCMOS Tri-State Output Buffers with High Slew-Rate
PTOD(1/2/4/6)	Open Drain Output Buffers
PTOD(4/6)SM	Open Drain Output Buffers with Medium Slew-Rate
PTOT(1/2/4/6)	Tri-State Output Buffers
PTOT(4/6)SM	Tri-State Output Buffers with Medium Slew-Rate

Cell Availability

Only 3.3V
POB(1/2/4/8/12/16/20/24)
POB(4/8/12/16/20/24)SM
POB(12/16/20/24)SH

Logic Symbol



Truth Table

A	PAD
0	0
1	1

Standard Load (SL)

Cell Name	A
POB(1/2/4/8/12/16/20/24)	3.437
POB(4/8/12/16/20/24)SM	3.437
POB(12/16/20/24)SH	3.437

PvOByz

Normal Output Buffers

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POB1

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	30.886	0.770 + 0.602*CL	0.764 + 0.602*CL	0.775 + 0.602*CL
	t_F	26.458	0.632 + 0.517*CL	0.634 + 0.516*CL	0.636 + 0.516*CL
	t_{PLH}	13.977	0.671 + 0.266*CL	0.665 + 0.266*CL	0.671 + 0.266*CL
	t_{PHL}	12.709	0.657 + 0.241*CL	0.652 + 0.241*CL	0.661 + 0.241*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	16.110	0.418 + 0.314*CL	0.421 + 0.314*CL	0.415 + 0.314*CL
	t_F	15.879	0.401 + 0.310*CL	0.398 + 0.310*CL	0.404 + 0.310*CL
	t_{PLH}	7.567	0.464 + 0.142*CL	0.461 + 0.142*CL	0.463 + 0.142*CL
	t_{PHL}	8.639	0.516 + 0.162*CL	0.521 + 0.162*CL	0.515 + 0.162*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	8.065	0.220 + 0.157*CL	0.213 + 0.157*CL	0.224 + 0.157*CL
	t_F	7.947	0.208 + 0.155*CL	0.206 + 0.155*CL	0.206 + 0.155*CL
	t_{PLH}	3.965	0.413 + 0.071*CL	0.413 + 0.071*CL	0.413 + 0.071*CL
	t_{PHL}	4.494	0.432 + 0.081*CL	0.433 + 0.081*CL	0.433 + 0.081*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB8

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.048	0.125 + 0.078*CL	0.125 + 0.078*CL	0.125 + 0.078*CL
	t_F	3.985	0.115 + 0.077*CL	0.115 + 0.077*CL	0.115 + 0.077*CL
	t_{PLH}	2.215	0.439 + 0.036*CL	0.440 + 0.036*CL	0.439 + 0.036*CL
	t_{PHL}	2.453	0.422 + 0.041*CL	0.423 + 0.041*CL	0.423 + 0.041*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POB12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.716	0.104 + 0.052*CL	0.101 + 0.052*CL	0.100 + 0.052*CL
	t_F	2.669	0.091 + 0.052*CL	0.089 + 0.052*CL	0.088 + 0.052*CL
	t_{PLH}	1.675	0.490 + 0.024*CL	0.491 + 0.024*CL	0.491 + 0.024*CL
	t_{PHL}	1.802	0.448 + 0.027*CL	0.448 + 0.027*CL	0.448 + 0.027*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB16

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.061	0.113 + 0.039*CL	0.103 + 0.039*CL	0.099 + 0.039*CL
	t_F	2.019	0.093 + 0.039*CL	0.086 + 0.039*CL	0.083 + 0.039*CL
	t_{PLH}	1.437	0.548 + 0.018*CL	0.548 + 0.018*CL	0.549 + 0.018*CL
	t_{PHL}	1.520	0.504 + 0.020*CL	0.504 + 0.020*CL	0.504 + 0.020*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB20

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.681	0.137 + 0.031*CL	0.123 + 0.031*CL	0.116 + 0.031*CL
	t_F	1.637	0.105 + 0.031*CL	0.095 + 0.031*CL	0.091 + 0.031*CL
	t_{PLH}	1.320	0.608 + 0.014*CL	0.609 + 0.014*CL	0.610 + 0.014*CL
	t_{PHL}	1.355	0.543 + 0.016*CL	0.543 + 0.016*CL	0.542 + 0.016*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB24

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.445	0.175 + 0.025*CL	0.157 + 0.026*CL	0.149 + 0.026*CL
	t_F	1.388	0.119 + 0.025*CL	0.109 + 0.026*CL	0.104 + 0.026*CL
	t_{PLH}	1.343	0.746 + 0.012*CL	0.751 + 0.012*CL	0.751 + 0.012*CL
	t_{PHL}	1.210	0.531 + 0.014*CL	0.533 + 0.014*CL	0.533 + 0.014*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

PvOByz

Normal Output Buffers

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POB4SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	10.372	2.774 + 0.152*CL	2.868 + 0.151*CL	2.888 + 0.150*CL
	t_F	12.602	4.238 + 0.167*CL	4.716 + 0.161*CL	4.957 + 0.158*CL
	t_{PLH}	9.596	5.306 + 0.086*CL	5.651 + 0.081*CL	5.832 + 0.079*CL
	t_{PHL}	12.659	6.735 + 0.118*CL	7.334 + 0.110*CL	7.676 + 0.106*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB8SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.180	1.432 + 0.075*CL	1.446 + 0.075*CL	1.437 + 0.075*CL
	t_F	5.796	1.978 + 0.076*CL	2.089 + 0.075*CL	2.134 + 0.074*CL
	t_{PLH}	5.201	3.125 + 0.042*CL	3.283 + 0.039*CL	3.363 + 0.038*CL
	t_{PHL}	6.233	3.616 + 0.052*CL	3.864 + 0.049*CL	3.997 + 0.047*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB12SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.656	2.014 + 0.053*CL	2.131 + 0.051*CL	2.184 + 0.051*CL
	t_F	4.377	1.826 + 0.051*CL	1.928 + 0.050*CL	1.968 + 0.049*CL
	t_{PLH}	5.343	3.537 + 0.036*CL	3.772 + 0.033*CL	3.902 + 0.031*CL
	t_{PHL}	4.910	3.008 + 0.038*CL	3.239 + 0.035*CL	3.358 + 0.034*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB16SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.066	1.928 + 0.043*CL	2.070 + 0.041*CL	2.144 + 0.040*CL
	t_F	3.810	1.738 + 0.041*CL	1.876 + 0.040*CL	1.946 + 0.039*CL
	t_{PLH}	5.011	3.439 + 0.031*CL	3.665 + 0.028*CL	3.791 + 0.027*CL
	t_{PHL}	4.532	2.889 + 0.033*CL	3.110 + 0.030*CL	3.231 + 0.029*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POB20SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.732	1.899 + 0.037*CL	2.047 + 0.035*CL	2.127 + 0.034*CL
	t_F	3.468	1.683 + 0.036*CL	1.830 + 0.034*CL	1.904 + 0.033*CL
	t_{PLH}	4.946	3.521 + 0.028*CL	3.737 + 0.026*CL	3.860 + 0.024*CL
	t_{PHL}	4.423	2.941 + 0.030*CL	3.153 + 0.027*CL	3.276 + 0.025*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB24SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.548	1.919 + 0.033*CL	2.068 + 0.031*CL	2.150 + 0.030*CL
	t_F	3.270	1.682 + 0.032*CL	1.829 + 0.030*CL	1.909 + 0.029*CL
	t_{PLH}	5.005	3.673 + 0.027*CL	3.885 + 0.024*CL	4.005 + 0.022*CL
	t_{PHL}	4.442	3.066 + 0.028*CL	3.273 + 0.025*CL	3.391 + 0.023*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB12SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.074	3.057 + 0.060*CL	3.291 + 0.057*CL	3.417 + 0.056*CL
	t_F	4.037	1.478 + 0.051*CL	1.564 + 0.050*CL	1.600 + 0.050*CL
	t_{PLH}	7.759	5.403 + 0.047*CL	5.762 + 0.042*CL	5.963 + 0.040*CL
	t_{PHL}	4.703	2.906 + 0.036*CL	3.089 + 0.033*CL	3.189 + 0.032*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB16SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.441	2.947 + 0.050*CL	3.182 + 0.047*CL	3.312 + 0.045*CL
	t_F	3.487	1.467 + 0.040*CL	1.575 + 0.039*CL	1.629 + 0.038*CL
	t_{PLH}	7.432	5.351 + 0.042*CL	5.689 + 0.037*CL	5.879 + 0.035*CL
	t_{PHL}	4.487	2.960 + 0.031*CL	3.145 + 0.028*CL	3.246 + 0.027*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POB20SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.120	2.940 + 0.044*CL	3.172 + 0.041*CL	3.302 + 0.039*CL
	t_F	3.205	1.493 + 0.034*CL	1.613 + 0.033*CL	1.676 + 0.032*CL
	t_{PLH}	7.461	5.541 + 0.038*CL	5.866 + 0.034*CL	6.050 + 0.032*CL
	t_{PHL}	4.484	3.106 + 0.028*CL	3.292 + 0.025*CL	3.396 + 0.024*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POB24SH

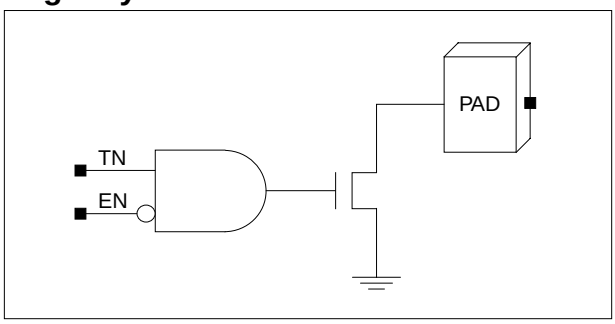
Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.973	2.999 + 0.039*CL	3.229 + 0.036*CL	3.357 + 0.035*CL
	t_F	3.058	1.544 + 0.030*CL	1.671 + 0.029*CL	1.738 + 0.028*CL
	t_{PLH}	7.645	5.821 + 0.036*CL	6.141 + 0.032*CL	6.323 + 0.030*CL
	t_{PHL}	4.570	3.278 + 0.026*CL	3.468 + 0.023*CL	3.575 + 0.022*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Cell Availability

Only 3.3V	5V - tolerant
POD(1/2/4/8/12/16/20/24) POD(4/8/12/16/20/24)SM POD(12/16/20/24)SH	PTOD(1/2/4/6) PTOD(4/6)SM

Logic Symbol



Truth Table

TN	EN	PAD
1	0	0
0	x	Hi-Z
x	1	Hi-Z

Standard Load (SL)

Cell Name	TN	EN
POD(1/2/4/8/12/16/20/24)	3.415	3.481
POD(4/8/12/16/20/24)SM	3.415	3.481
POD(12/16/20/24)SH	3.415	3.481
PTOD(1/2/4/6)	3.415	3.481
PTOD(4/6)SM	3.415	3.481

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POD1

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	26.622	0.664 + 0.519*CL	0.661 + 0.519*CL	0.661 + 0.519*CL
	t_{PHL}	12.612	0.544 + 0.241*CL	0.541 + 0.241*CL	0.547 + 0.241*CL
	t_{PLZ}	0.187	0.187 + 0.000*CL	0.187 + 0.000*CL	0.187 + 0.000*CL
EN to PAD	t_F	26.622	0.664 + 0.519*CL	0.661 + 0.519*CL	0.661 + 0.519*CL
	t_{PHL}	12.681	0.613 + 0.241*CL	0.617 + 0.241*CL	0.615 + 0.241*CL
	t_{PLZ}	0.199	0.199 + 0.000*CL	0.199 + 0.000*CL	0.200 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POD2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	15.920	0.402 + 0.310*CL	0.399 + 0.310*CL	0.399 + 0.310*CL
	t_{PHL}	8.537	0.409 + 0.163*CL	0.406 + 0.163*CL	0.406 + 0.163*CL
	t_{PLZ}	0.168	0.168 + 0.000*CL	0.168 + 0.000*CL	0.168 + 0.000*CL
EN to PAD	t_F	15.920	0.402 + 0.310*CL	0.399 + 0.310*CL	0.399 + 0.310*CL
	t_{PHL}	8.606	0.477 + 0.163*CL	0.475 + 0.163*CL	0.481 + 0.163*CL
	t_{PLZ}	0.179	0.179 + 0.000*CL	0.179 + 0.000*CL	0.179 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POD4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	7.957	0.207 + 0.155*CL	0.207 + 0.155*CL	0.213 + 0.155*CL
	t_{PHL}	4.386	0.323 + 0.081*CL	0.323 + 0.081*CL	0.323 + 0.081*CL
	t_{PLZ}	0.188	0.188 + 0.000*CL	0.188 + 0.000*CL	0.188 + 0.000*CL
EN to PAD	t_F	7.957	0.207 + 0.155*CL	0.207 + 0.155*CL	0.213 + 0.155*CL
	t_{PHL}	4.454	0.392 + 0.081*CL	0.391 + 0.081*CL	0.392 + 0.081*CL
	t_{PLZ}	0.200	0.200 + 0.000*CL	0.200 + 0.000*CL	0.200 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POD8

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.987	0.115 + 0.077*CL	0.115 + 0.077*CL	0.116 + 0.077*CL
	t_{PHL}	2.344	0.313 + 0.041*CL	0.313 + 0.041*CL	0.314 + 0.041*CL
	t_{PLZ}	0.227	0.227 + 0.000*CL	0.227 + 0.000*CL	0.227 + 0.000*CL
EN to PAD	t_F	3.987	0.115 + 0.077*CL	0.115 + 0.077*CL	0.116 + 0.077*CL
	t_{PHL}	2.413	0.382 + 0.041*CL	0.382 + 0.041*CL	0.382 + 0.041*CL
	t_{PLZ}	0.238	0.238 + 0.000*CL	0.238 + 0.000*CL	0.238 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POD12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.670	0.092 + 0.052*CL	0.090 + 0.052*CL	0.088 + 0.052*CL
	t_{PHL}	1.692	0.338 + 0.027*CL	0.339 + 0.027*CL	0.339 + 0.027*CL
	t_{PLZ}	0.264	0.264 + 0.000*CL	0.264 + 0.000*CL	0.264 + 0.000*CL
EN to PAD	t_F	2.670	0.092 + 0.052*CL	0.090 + 0.052*CL	0.088 + 0.052*CL
	t_{PHL}	1.761	0.407 + 0.027*CL	0.406 + 0.027*CL	0.407 + 0.027*CL
	t_{PLZ}	0.275	0.275 + 0.000*CL	0.275 + 0.000*CL	0.275 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POD16

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.020	0.094 + 0.039*CL	0.087 + 0.039*CL	0.084 + 0.039*CL
	t_{PHL}	1.410	0.394 + 0.020*CL	0.394 + 0.020*CL	0.394 + 0.020*CL
	t_{PLZ}	0.254	0.254 + 0.000*CL	0.254 + 0.000*CL	0.254 + 0.000*CL
EN to PAD	t_F	2.020	0.094 + 0.039*CL	0.087 + 0.039*CL	0.084 + 0.039*CL
	t_{PHL}	1.478	0.462 + 0.020*CL	0.462 + 0.020*CL	0.463 + 0.020*CL
	t_{PLZ}	0.265	0.265 + 0.000*CL	0.265 + 0.000*CL	0.265 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

PvODyz

Open Drain Output Buffers

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POD20

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.639	0.108 + 0.031*CL	0.097 + 0.031*CL	0.093 + 0.031*CL
	t_{PHL}	1.243	0.430 + 0.016*CL	0.430 + 0.016*CL	0.431 + 0.016*CL
	t_{PLZ}	0.279	0.279 + 0.000*CL	0.279 + 0.000*CL	0.279 + 0.000*CL
EN to PAD	t_F	1.639	0.109 + 0.031*CL	0.097 + 0.031*CL	0.093 + 0.031*CL
	t_{PHL}	1.312	0.498 + 0.016*CL	0.500 + 0.016*CL	0.499 + 0.016*CL
	t_{PLZ}	0.289	0.289 + 0.000*CL	0.287 + 0.000*CL	0.290 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POD24

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.391	0.125 + 0.025*CL	0.113 + 0.025*CL	0.107 + 0.026*CL
	t_{PHL}	1.101	0.421 + 0.014*CL	0.424 + 0.014*CL	0.425 + 0.014*CL
	t_{PLZ}	0.593	0.593 + 0.000*CL	0.593 + 0.000*CL	0.593 + 0.000*CL
EN to PAD	t_F	1.391	0.125 + 0.025*CL	0.113 + 0.025*CL	0.107 + 0.026*CL
	t_{PHL}	1.170	0.490 + 0.014*CL	0.493 + 0.014*CL	0.493 + 0.014*CL
	t_{PLZ}	0.605	0.605 + 0.000*CL	0.605 + 0.000*CL	0.605 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POD4SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	12.636	4.270 + 0.167*CL	4.744 + 0.161*CL	4.982 + 0.158*CL
	t_{PHL}	12.547	6.617 + 0.119*CL	7.217 + 0.111*CL	7.563 + 0.107*CL
	t_{PLZ}	0.426	0.402 + 0.000*CL	0.432 + 0.000*CL	0.438 + 0.000*CL
EN to PAD	t_F	12.636	4.270 + 0.167*CL	4.744 + 0.161*CL	4.982 + 0.158*CL
	t_{PHL}	12.617	6.687 + 0.119*CL	7.294 + 0.111*CL	7.632 + 0.107*CL
	t_{PLZ}	0.442	0.418 + 0.000*CL	0.451 + 0.000*CL	0.455 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POD8SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	5.817	2.003 + 0.076*CL	2.111 + 0.075*CL	2.154 + 0.074*CL
	t_{PHL}	6.120	3.500 + 0.052*CL	3.749 + 0.049*CL	3.882 + 0.048*CL
	t_{PLZ}	0.304	0.304 + 0.000*CL	0.304 + 0.000*CL	0.304 + 0.000*CL
EN to PAD	t_F	5.817	2.003 + 0.076*CL	2.111 + 0.075*CL	2.155 + 0.074*CL
	t_{PHL}	6.189	3.570 + 0.052*CL	3.818 + 0.049*CL	3.952 + 0.047*CL
	t_{PLZ}	0.317	0.317 + 0.000*CL	0.317 + 0.000*CL	0.317 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POD12SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	4.402	1.864 + 0.051*CL	1.955 + 0.050*CL	1.994 + 0.049*CL
	t_{PHL}	4.799	2.903 + 0.038*CL	3.122 + 0.035*CL	3.243 + 0.034*CL
	t_{PLZ}	0.301	0.301 + 0.000*CL	0.301 + 0.000*CL	0.301 + 0.000*CL
EN to PAD	t_F	4.401	1.862 + 0.051*CL	1.955 + 0.050*CL	1.994 + 0.049*CL
	t_{PHL}	4.866	2.966 + 0.038*CL	3.191 + 0.035*CL	3.311 + 0.034*CL
	t_{PLZ}	0.314	0.314 + 0.000*CL	0.314 + 0.000*CL	0.314 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POD16SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.837	1.775 + 0.041*CL	1.908 + 0.039*CL	1.975 + 0.039*CL
	t_{PHL}	4.417	2.770 + 0.033*CL	2.992 + 0.030*CL	3.115 + 0.029*CL
	t_{PLZ}	0.320	0.320 + 0.000*CL	0.320 + 0.000*CL	0.320 + 0.000*CL
EN to PAD	t_F	3.837	1.775 + 0.041*CL	1.909 + 0.039*CL	1.976 + 0.039*CL
	t_{PHL}	4.486	2.838 + 0.033*CL	3.061 + 0.030*CL	3.184 + 0.029*CL
	t_{PLZ}	0.332	0.332 + 0.000*CL	0.332 + 0.000*CL	0.332 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POD20SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.498	1.725 + 0.035*CL	1.866 + 0.034*CL	1.941 + 0.033*CL
	t_{PHL}	4.307	2.821 + 0.030*CL	3.034 + 0.027*CL	3.154 + 0.025*CL
	t_{PLZ}	0.339	0.339 + 0.000*CL	0.339 + 0.000*CL	0.339 + 0.000*CL
EN to PAD	t_F	3.499	1.725 + 0.035*CL	1.866 + 0.034*CL	1.941 + 0.033*CL
	t_{PHL}	4.375	2.889 + 0.030*CL	3.103 + 0.027*CL	3.222 + 0.025*CL
	t_{PLZ}	0.351	0.351 + 0.000*CL	0.351 + 0.000*CL	0.351 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POD24SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.305	1.729 + 0.032*CL	1.872 + 0.030*CL	1.949 + 0.029*CL
	t_{PHL}	4.325	2.944 + 0.028*CL	3.153 + 0.025*CL	3.272 + 0.023*CL
	t_{PLZ}	0.358	0.358 + 0.000*CL	0.358 + 0.000*CL	0.358 + 0.000*CL
EN to PAD	t_F	3.305	1.729 + 0.032*CL	1.871 + 0.030*CL	1.948 + 0.029*CL
	t_{PHL}	4.394	3.013 + 0.028*CL	3.222 + 0.025*CL	3.340 + 0.023*CL
	t_{PLZ}	0.369	0.368 + 0.000*CL	0.368 + 0.000*CL	0.369 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POD12SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	5.975	3.028 + 0.059*CL	3.245 + 0.056*CL	3.366 + 0.055*CL
	t_{PHL}	7.057	4.519 + 0.051*CL	4.890 + 0.046*CL	5.098 + 0.043*CL
	t_{PLZ}	0.366	0.364 + 0.000*CL	0.366 + 0.000*CL	0.366 + 0.000*CL
EN to PAD	t_F	5.975	3.027 + 0.059*CL	3.245 + 0.056*CL	3.365 + 0.055*CL
	t_{PHL}	7.127	4.589 + 0.051*CL	4.959 + 0.046*CL	5.167 + 0.043*CL
	t_{PLZ}	0.379	0.378 + 0.000*CL	0.380 + 0.000*CL	0.380 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POD16SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	5.302	2.838 + 0.049*CL	3.071 + 0.046*CL	3.198 + 0.045*CL
	t_{PHL}	6.569	4.341 + 0.045*CL	4.689 + 0.040*CL	4.885 + 0.038*CL
	t_{PLZ}	0.385	0.384 + 0.000*CL	0.386 + 0.000*CL	0.386 + 0.000*CL
EN to PAD	t_F	5.302	2.838 + 0.049*CL	3.070 + 0.046*CL	3.198 + 0.045*CL
	t_{PHL}	6.638	4.411 + 0.045*CL	4.758 + 0.040*CL	4.953 + 0.038*CL
	t_{PLZ}	0.398	0.397 + 0.000*CL	0.399 + 0.000*CL	0.399 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POD20SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	4.927	2.764 + 0.043*CL	2.997 + 0.040*CL	3.124 + 0.039*CL
	t_{PHL}	6.503	4.468 + 0.041*CL	4.801 + 0.036*CL	4.989 + 0.034*CL
	t_{PLZ}	0.404	0.399 + 0.000*CL	0.406 + 0.000*CL	0.406 + 0.000*CL
EN to PAD	t_F	4.927	2.764 + 0.043*CL	2.996 + 0.040*CL	3.125 + 0.039*CL
	t_{PHL}	6.573	4.537 + 0.041*CL	4.871 + 0.036*CL	5.059 + 0.034*CL
	t_{PLZ}	0.416	0.412 + 0.000*CL	0.419 + 0.000*CL	0.419 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POD24SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	4.739	2.781 + 0.039*CL	3.012 + 0.036*CL	3.140 + 0.035*CL
	t_{PHL}	6.620	4.700 + 0.038*CL	5.028 + 0.034*CL	5.213 + 0.032*CL
	t_{PLZ}	0.421	0.413 + 0.000*CL	0.425 + 0.000*CL	0.425 + 0.000*CL
EN to PAD	t_F	4.739	2.781 + 0.039*CL	3.012 + 0.036*CL	3.140 + 0.035*CL
	t_{PHL}	6.690	4.769 + 0.038*CL	5.098 + 0.034*CL	5.283 + 0.032*CL
	t_{PLZ}	0.433	0.424 + 0.000*CL	0.437 + 0.000*CL	0.437 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PTOD1

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	27.282	1.322 + 0.519*CL	1.329 + 0.519*CL	1.321 + 0.519*CL
	t_{PHL}	12.728	0.642 + 0.242*CL	0.659 + 0.241*CL	0.656 + 0.242*CL
	t_{PLZ}	0.175	0.174 + 0.000*CL	0.175 + 0.000*CL	0.175 + 0.000*CL
EN to PAD	t_F	27.282	1.322 + 0.519*CL	1.329 + 0.519*CL	1.321 + 0.519*CL
	t_{PHL}	12.796	0.710 + 0.242*CL	0.719 + 0.242*CL	0.730 + 0.241*CL
	t_{PLZ}	0.187	0.187 + 0.000*CL	0.187 + 0.000*CL	0.188 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

PTOD2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	13.682	0.734 + 0.259*CL	0.731 + 0.259*CL	0.737 + 0.259*CL
	t_{PHL}	6.510	0.456 + 0.121*CL	0.471 + 0.121*CL	0.472 + 0.121*CL
	t_{PLZ}	0.202	0.202 + 0.000*CL	0.202 + 0.000*CL	0.202 + 0.000*CL
EN to PAD	t_F	13.682	0.734 + 0.259*CL	0.731 + 0.259*CL	0.737 + 0.259*CL
	t_{PHL}	6.579	0.525 + 0.121*CL	0.534 + 0.121*CL	0.547 + 0.121*CL
	t_{PLZ}	0.213	0.213 + 0.000*CL	0.213 + 0.000*CL	0.213 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

PTOD4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.893	0.426 + 0.129*CL	0.430 + 0.129*CL	0.427 + 0.129*CL
	t_{PHL}	3.444	0.410 + 0.061*CL	0.418 + 0.061*CL	0.422 + 0.061*CL
	t_{PLZ}	0.251	0.251 + 0.000*CL	0.251 + 0.000*CL	0.251 + 0.000*CL
EN to PAD	t_F	6.893	0.426 + 0.129*CL	0.430 + 0.129*CL	0.427 + 0.129*CL
	t_{PHL}	3.512	0.479 + 0.061*CL	0.486 + 0.061*CL	0.491 + 0.061*CL
	t_{PLZ}	0.264	0.264 + 0.000*CL	0.264 + 0.000*CL	0.264 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PTOD6

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	4.627	0.322 + 0.086*CL	0.320 + 0.086*CL	0.318 + 0.086*CL
	t_{PHL}	2.458	0.433 + 0.040*CL	0.439 + 0.040*CL	0.442 + 0.040*CL
	t_{PLZ}	0.300	0.300 + 0.000*CL	0.299 + 0.000*CL	0.299 + 0.000*CL
EN to PAD	t_F	4.627	0.322 + 0.086*CL	0.320 + 0.086*CL	0.318 + 0.086*CL
	t_{PHL}	2.526	0.502 + 0.040*CL	0.507 + 0.040*CL	0.510 + 0.040*CL
	t_{PLZ}	0.311	0.311 + 0.000*CL	0.311 + 0.000*CL	0.311 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

PTOD4SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	10.257	3.425 + 0.137*CL	3.721 + 0.133*CL	3.871 + 0.131*CL
	t_{PHL}	11.241	6.905 + 0.087*CL	7.364 + 0.081*CL	7.613 + 0.078*CL
	t_{PLZ}	0.449	0.408 + 0.001*CL	0.459 + 0.000*CL	0.470 + 0.000*CL
EN to PAD	t_F	10.257	3.425 + 0.137*CL	3.721 + 0.133*CL	3.871 + 0.131*CL
	t_{PHL}	11.311	6.977 + 0.087*CL	7.425 + 0.081*CL	7.683 + 0.078*CL
	t_{PLZ}	0.465	0.424 + 0.001*CL	0.477 + 0.000*CL	0.486 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

PTOD6SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	8.361	3.435 + 0.099*CL	3.736 + 0.095*CL	3.904 + 0.093*CL
	t_{PHL}	11.191	7.639 + 0.071*CL	8.114 + 0.065*CL	8.384 + 0.062*CL
	t_{PLZ}	0.464	0.401 + 0.001*CL	0.474 + 0.000*CL	0.498 + 0.000*CL
EN to PAD	t_F	8.361	3.435 + 0.099*CL	3.736 + 0.095*CL	3.904 + 0.093*CL
	t_{PHL}	11.261	7.709 + 0.071*CL	8.185 + 0.065*CL	8.454 + 0.062*CL
	t_{PLZ}	0.480	0.417 + 0.001*CL	0.492 + 0.000*CL	0.513 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

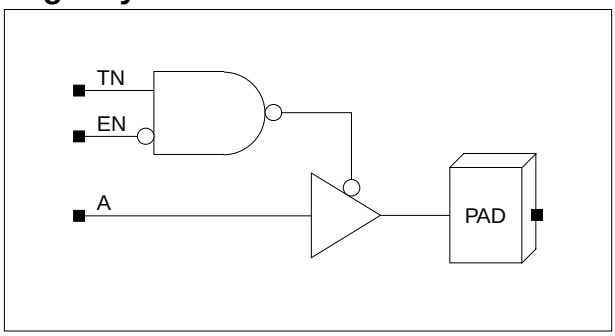
PvOTyz

Tri-State Output Buffers

Cell Availability

Only 3.3V	5V - tolerant
POT(1/2/4/8/12/16/20/24) POT(4/8/12/16/20/24)SM POT(12/16/20/24)SH	PTOT(1/2/4/6) PTOT(4/6)SM

Logic Symbol



Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi-Z
0	x	x	Hi-Z

Standard Load (SL)

Cell Name	TN	EN	A
POT(1/2/4/8/12/16/20/24)	3.393	3.481	3.441
POT(4/8/12/16/20/24)SM	3.393	3.481	3.441
POT(12/16/20/24)SH	3.393	3.481	3.441
PTOT(1/2/4/6)	3.393	3.481	3.441
PTOT(4/6)SM	3.393	3.481	3.441

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT1

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	30.886	0.770 + 0.602*CL	0.764 + 0.602*CL	0.775 + 0.602*CL
	t_F	26.458	0.632 + 0.517*CL	0.634 + 0.516*CL	0.636 + 0.516*CL
	t_{PLH}	13.977	0.671 + 0.266*CL	0.665 + 0.266*CL	0.671 + 0.266*CL
	t_{PHL}	12.709	0.657 + 0.241*CL	0.652 + 0.241*CL	0.661 + 0.241*CL
TN to PAD	t_R	31.080	0.774 + 0.606*CL	0.776 + 0.606*CL	0.773 + 0.606*CL
	t_F	26.593	0.635 + 0.519*CL	0.632 + 0.519*CL	0.638 + 0.519*CL
	t_{PLH}	14.072	0.746 + 0.267*CL	0.748 + 0.266*CL	0.745 + 0.267*CL
	t_{PHL}	12.798	0.730 + 0.241*CL	0.735 + 0.241*CL	0.732 + 0.241*CL
	t_{PLZ}	0.368	0.368 + 0.000*CL	0.368 + 0.000*CL	0.368 + 0.000*CL
	t_{PHZ}	0.317	0.317 + 0.000*CL	0.317 + 0.000*CL	0.317 + 0.000*CL
EN to PAD	t_R	31.080	0.774 + 0.606*CL	0.776 + 0.606*CL	0.773 + 0.606*CL
	t_F	26.593	0.635 + 0.519*CL	0.632 + 0.519*CL	0.638 + 0.519*CL
	t_{PLH}	14.142	0.816 + 0.267*CL	0.818 + 0.266*CL	0.815 + 0.267*CL
	t_{PHL}	12.867	0.799 + 0.241*CL	0.803 + 0.241*CL	0.795 + 0.241*CL
	t_{PLZ}	0.379	0.379 + 0.000*CL	0.379 + 0.000*CL	0.379 + 0.000*CL
	t_{PHZ}	0.329	0.329 + 0.000*CL	0.329 + 0.000*CL	0.329 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POT2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	16.110	0.418 + 0.314*CL	0.421 + 0.314*CL	0.415 + 0.314*CL
	t_F	15.879	0.401 + 0.310*CL	0.398 + 0.310*CL	0.404 + 0.310*CL
	t_{PLH}	7.567	0.464 + 0.142*CL	0.461 + 0.142*CL	0.463 + 0.142*CL
	t_{PHL}	8.639	0.516 + 0.162*CL	0.521 + 0.162*CL	0.515 + 0.162*CL
TN to PAD	t_R	16.161	0.421 + 0.315*CL	0.413 + 0.315*CL	0.422 + 0.315*CL
	t_F	15.920	0.402 + 0.310*CL	0.399 + 0.310*CL	0.399 + 0.310*CL
	t_{PLH}	7.648	0.539 + 0.142*CL	0.538 + 0.142*CL	0.544 + 0.142*CL
	t_{PHL}	8.721	0.591 + 0.163*CL	0.598 + 0.163*CL	0.590 + 0.163*CL
	t_{PLZ}	0.321	0.321 + 0.000*CL	0.321 + 0.000*CL	0.321 + 0.000*CL
	t_{PHZ}	0.296	0.296 + 0.000*CL	0.296 + 0.000*CL	0.296 + 0.000*CL
EN to PAD	t_R	16.161	0.421 + 0.315*CL	0.413 + 0.315*CL	0.422 + 0.315*CL
	t_F	15.920	0.402 + 0.310*CL	0.399 + 0.310*CL	0.399 + 0.310*CL
	t_{PLH}	7.718	0.609 + 0.142*CL	0.615 + 0.142*CL	0.607 + 0.142*CL
	t_{PHL}	8.790	0.661 + 0.163*CL	0.660 + 0.163*CL	0.666 + 0.163*CL
	t_{PLZ}	0.335	0.335 + 0.000*CL	0.335 + 0.000*CL	0.335 + 0.000*CL
	t_{PHZ}	0.309	0.309 + 0.000*CL	0.309 + 0.000*CL	0.309 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	8.065	0.220 + 0.157*CL	0.213 + 0.157*CL	0.224 + 0.157*CL
	t_F	7.947	0.208 + 0.155*CL	0.206 + 0.155*CL	0.206 + 0.155*CL
	t_{PLH}	3.965	0.413 + 0.071*CL	0.413 + 0.071*CL	0.413 + 0.071*CL
	t_{PHL}	4.494	0.432 + 0.081*CL	0.433 + 0.081*CL	0.433 + 0.081*CL
TN to PAD	t_R	8.078	0.220 + 0.157*CL	0.217 + 0.157*CL	0.223 + 0.157*CL
	t_F	7.957	0.207 + 0.155*CL	0.207 + 0.155*CL	0.213 + 0.155*CL
	t_{PLH}	4.042	0.489 + 0.071*CL	0.489 + 0.071*CL	0.489 + 0.071*CL
	t_{PHL}	4.570	0.507 + 0.081*CL	0.507 + 0.081*CL	0.507 + 0.081*CL
	t_{PLZ}	0.366	0.366 + 0.000*CL	0.366 + 0.000*CL	0.366 + 0.000*CL
	t_{PHZ}	0.318	0.318 + 0.000*CL	0.318 + 0.000*CL	0.318 + 0.000*CL
EN to PAD	t_R	8.078	0.220 + 0.157*CL	0.217 + 0.157*CL	0.223 + 0.157*CL
	t_F	7.957	0.207 + 0.155*CL	0.207 + 0.155*CL	0.213 + 0.155*CL
	t_{PLH}	4.112	0.559 + 0.071*CL	0.559 + 0.071*CL	0.559 + 0.071*CL
	t_{PHL}	4.639	0.576 + 0.081*CL	0.576 + 0.081*CL	0.576 + 0.081*CL
	t_{PLZ}	0.378	0.378 + 0.000*CL	0.378 + 0.000*CL	0.378 + 0.000*CL
	t_{PHZ}	0.329	0.329 + 0.000*CL	0.329 + 0.000*CL	0.329 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POT8

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.048	0.125 + 0.078*CL	0.125 + 0.078*CL	0.125 + 0.078*CL
	t_F	3.985	0.115 + 0.077*CL	0.115 + 0.077*CL	0.115 + 0.077*CL
	t_{PLH}	2.215	0.439 + 0.036*CL	0.440 + 0.036*CL	0.439 + 0.036*CL
	t_{PHL}	2.453	0.422 + 0.041*CL	0.423 + 0.041*CL	0.423 + 0.041*CL
TN to PAD	t_R	4.051	0.125 + 0.079*CL	0.125 + 0.079*CL	0.125 + 0.079*CL
	t_F	3.987	0.115 + 0.077*CL	0.115 + 0.077*CL	0.115 + 0.077*CL
	t_{PLH}	2.292	0.514 + 0.036*CL	0.515 + 0.036*CL	0.516 + 0.036*CL
	t_{PHL}	2.528	0.497 + 0.041*CL	0.497 + 0.041*CL	0.497 + 0.041*CL
	t_{PLZ}	0.453	0.453 + 0.000*CL	0.453 + 0.000*CL	0.453 + 0.000*CL
	t_{PHZ}	0.356	0.356 + 0.000*CL	0.356 + 0.000*CL	0.356 + 0.000*CL
EN to PAD	t_R	4.051	0.126 + 0.079*CL	0.125 + 0.079*CL	0.125 + 0.079*CL
	t_F	3.987	0.115 + 0.077*CL	0.115 + 0.077*CL	0.115 + 0.077*CL
	t_{PLH}	2.361	0.585 + 0.036*CL	0.585 + 0.036*CL	0.585 + 0.036*CL
	t_{PHL}	2.597	0.566 + 0.041*CL	0.567 + 0.041*CL	0.566 + 0.041*CL
	t_{PLZ}	0.464	0.464 + 0.000*CL	0.464 + 0.000*CL	0.464 + 0.000*CL
	t_{PHZ}	0.369	0.369 + 0.000*CL	0.369 + 0.000*CL	0.369 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.716	0.104 + 0.052*CL	0.101 + 0.052*CL	0.100 + 0.052*CL
	t_F	2.669	0.091 + 0.052*CL	0.089 + 0.052*CL	0.088 + 0.052*CL
	t_{PLH}	1.675	0.490 + 0.024*CL	0.491 + 0.024*CL	0.491 + 0.024*CL
	t_{PHL}	1.802	0.448 + 0.027*CL	0.448 + 0.027*CL	0.448 + 0.027*CL
TN to PAD	t_R	2.717	0.104 + 0.052*CL	0.101 + 0.052*CL	0.100 + 0.052*CL
	t_F	2.670	0.091 + 0.052*CL	0.089 + 0.052*CL	0.088 + 0.052*CL
	t_{PLH}	1.752	0.566 + 0.024*CL	0.567 + 0.024*CL	0.567 + 0.024*CL
	t_{PHL}	1.876	0.521 + 0.027*CL	0.521 + 0.027*CL	0.522 + 0.027*CL
	t_{PLZ}	0.540	0.540 + 0.000*CL	0.540 + 0.000*CL	0.540 + 0.000*CL
	t_{PHZ}	0.393	0.393 + 0.000*CL	0.393 + 0.000*CL	0.394 + 0.000*CL
EN to PAD	t_R	2.717	0.104 + 0.052*CL	0.101 + 0.052*CL	0.100 + 0.052*CL
	t_F	2.670	0.091 + 0.052*CL	0.089 + 0.052*CL	0.088 + 0.052*CL
	t_{PLH}	1.821	0.636 + 0.024*CL	0.637 + 0.024*CL	0.637 + 0.024*CL
	t_{PHL}	1.945	0.591 + 0.027*CL	0.592 + 0.027*CL	0.591 + 0.027*CL
	t_{PLZ}	0.551	0.551 + 0.000*CL	0.551 + 0.000*CL	0.551 + 0.000*CL
	t_{PHZ}	0.406	0.406 + 0.000*CL	0.406 + 0.000*CL	0.406 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POT16

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.061	0.113 + 0.039*CL	0.103 + 0.039*CL	0.099 + 0.039*CL
	t_F	2.019	0.093 + 0.039*CL	0.086 + 0.039*CL	0.083 + 0.039*CL
	t_{PLH}	1.437	0.548 + 0.018*CL	0.548 + 0.018*CL	0.549 + 0.018*CL
	t_{PHL}	1.520	0.504 + 0.020*CL	0.504 + 0.020*CL	0.504 + 0.020*CL
TN to PAD	t_R	2.062	0.113 + 0.039*CL	0.103 + 0.039*CL	0.099 + 0.039*CL
	t_F	2.019	0.092 + 0.039*CL	0.086 + 0.039*CL	0.084 + 0.039*CL
	t_{PLH}	1.514	0.624 + 0.018*CL	0.626 + 0.018*CL	0.624 + 0.018*CL
	t_{PHL}	1.593	0.576 + 0.020*CL	0.577 + 0.020*CL	0.577 + 0.020*CL
	t_{PLZ}	0.627	0.627 + 0.000*CL	0.627 + 0.000*CL	0.627 + 0.000*CL
	t_{PHZ}	0.383	0.382 + 0.000*CL	0.383 + 0.000*CL	0.383 + 0.000*CL
EN to PAD	t_R	2.062	0.113 + 0.039*CL	0.103 + 0.039*CL	0.099 + 0.039*CL
	t_F	2.019	0.092 + 0.039*CL	0.086 + 0.039*CL	0.084 + 0.039*CL
	t_{PLH}	1.584	0.695 + 0.018*CL	0.695 + 0.018*CL	0.696 + 0.018*CL
	t_{PHL}	1.662	0.646 + 0.020*CL	0.646 + 0.020*CL	0.646 + 0.020*CL
	t_{PLZ}	0.638	0.638 + 0.000*CL	0.638 + 0.000*CL	0.638 + 0.000*CL
	t_{PHZ}	0.395	0.395 + 0.000*CL	0.395 + 0.000*CL	0.395 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT20

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.681	0.137 + 0.031*CL	0.123 + 0.031*CL	0.116 + 0.031*CL
	t_F	1.637	0.105 + 0.031*CL	0.095 + 0.031*CL	0.091 + 0.031*CL
	t_{PLH}	1.320	0.608 + 0.014*CL	0.609 + 0.014*CL	0.610 + 0.014*CL
	t_{PHL}	1.355	0.543 + 0.016*CL	0.543 + 0.016*CL	0.542 + 0.016*CL
TN to PAD	t_R	1.682	0.137 + 0.031*CL	0.122 + 0.031*CL	0.116 + 0.031*CL
	t_F	1.637	0.105 + 0.031*CL	0.097 + 0.031*CL	0.091 + 0.031*CL
	t_{PLH}	1.396	0.684 + 0.014*CL	0.684 + 0.014*CL	0.686 + 0.014*CL
	t_{PHL}	1.426	0.612 + 0.016*CL	0.613 + 0.016*CL	0.613 + 0.016*CL
	t_{PLZ}	0.713	0.713 + 0.000*CL	0.713 + 0.000*CL	0.713 + 0.000*CL
	t_{PHZ}	0.408	0.408 + 0.000*CL	0.408 + 0.000*CL	0.408 + 0.000*CL
EN to PAD	t_R	1.682	0.137 + 0.031*CL	0.122 + 0.031*CL	0.116 + 0.031*CL
	t_F	1.637	0.105 + 0.031*CL	0.097 + 0.031*CL	0.091 + 0.031*CL
	t_{PLH}	1.466	0.753 + 0.014*CL	0.748 + 0.014*CL	0.757 + 0.014*CL
	t_{PHL}	1.495	0.681 + 0.016*CL	0.683 + 0.016*CL	0.682 + 0.016*CL
	t_{PLZ}	0.725	0.725 + 0.000*CL	0.725 + 0.000*CL	0.725 + 0.000*CL
	t_{PHZ}	0.419	0.419 + 0.000*CL	0.419 + 0.000*CL	0.419 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POT24

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.445	0.175 + 0.025*CL	0.157 + 0.026*CL	0.149 + 0.026*CL
	t_F	1.388	0.119 + 0.025*CL	0.109 + 0.026*CL	0.104 + 0.026*CL
	t_{PLH}	1.343	0.746 + 0.012*CL	0.751 + 0.012*CL	0.751 + 0.012*CL
	t_{PHL}	1.210	0.531 + 0.014*CL	0.533 + 0.014*CL	0.533 + 0.014*CL
TN to PAD	t_R	1.446	0.176 + 0.025*CL	0.158 + 0.026*CL	0.149 + 0.026*CL
	t_F	1.389	0.120 + 0.025*CL	0.109 + 0.026*CL	0.105 + 0.026*CL
	t_{PLH}	1.419	0.822 + 0.012*CL	0.825 + 0.012*CL	0.827 + 0.012*CL
	t_{PHL}	1.284	0.604 + 0.014*CL	0.607 + 0.014*CL	0.607 + 0.014*CL
	t_{PLZ}	0.557	0.557 + 0.000*CL	0.557 + 0.000*CL	0.557 + 0.000*CL
	t_{PHZ}	0.723	0.723 + 0.000*CL	0.723 + 0.000*CL	0.723 + 0.000*CL
EN to PAD	t_R	1.446	0.176 + 0.025*CL	0.158 + 0.026*CL	0.149 + 0.026*CL
	t_F	1.389	0.120 + 0.025*CL	0.110 + 0.026*CL	0.104 + 0.026*CL
	t_{PLH}	1.489	0.893 + 0.012*CL	0.896 + 0.012*CL	0.898 + 0.012*CL
	t_{PHL}	1.353	0.674 + 0.014*CL	0.676 + 0.014*CL	0.676 + 0.014*CL
	t_{PLZ}	0.568	0.568 + 0.000*CL	0.568 + 0.000*CL	0.568 + 0.000*CL
	t_{PHZ}	0.735	0.735 + 0.000*CL	0.733 + 0.000*CL	0.735 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT4SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	10.372	2.774 + 0.152*CL	2.868 + 0.151*CL	2.888 + 0.150*CL
	t_F	12.602	4.238 + 0.167*CL	4.716 + 0.161*CL	4.957 + 0.158*CL
	t_{PLH}	9.596	5.306 + 0.086*CL	5.651 + 0.081*CL	5.832 + 0.079*CL
	t_{PHL}	12.659	6.735 + 0.118*CL	7.334 + 0.110*CL	7.676 + 0.106*CL
TN to PAD	t_R	10.387	2.779 + 0.152*CL	2.866 + 0.151*CL	2.889 + 0.151*CL
	t_F	12.619	4.247 + 0.167*CL	4.715 + 0.161*CL	4.964 + 0.158*CL
	t_{PLH}	9.678	5.387 + 0.086*CL	5.726 + 0.081*CL	5.916 + 0.079*CL
	t_{PHL}	12.739	6.813 + 0.119*CL	7.415 + 0.110*CL	7.752 + 0.107*CL
	t_{PLZ}	0.674	0.674 + 0.000*CL	0.674 + 0.000*CL	0.674 + 0.000*CL
	t_{PHZ}	0.573	0.573 + 0.000*CL	0.573 + 0.000*CL	0.573 + 0.000*CL
EN to PAD	t_R	10.387	2.779 + 0.152*CL	2.866 + 0.151*CL	2.889 + 0.151*CL
	t_F	12.619	4.247 + 0.167*CL	4.715 + 0.161*CL	4.964 + 0.158*CL
	t_{PLH}	9.749	5.459 + 0.086*CL	5.796 + 0.081*CL	5.986 + 0.079*CL
	t_{PHL}	12.808	6.882 + 0.119*CL	7.483 + 0.111*CL	7.821 + 0.107*CL
	t_{PLZ}	0.685	0.685 + 0.000*CL	0.685 + 0.000*CL	0.685 + 0.000*CL
	t_{PHZ}	0.585	0.585 + 0.000*CL	0.585 + 0.000*CL	0.585 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POT8SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.180	1.432 + 0.075*CL	1.446 + 0.075*CL	1.437 + 0.075*CL
	t_F	5.796	1.978 + 0.076*CL	2.089 + 0.075*CL	2.134 + 0.074*CL
	t_{PLH}	5.201	3.125 + 0.042*CL	3.283 + 0.039*CL	3.363 + 0.038*CL
	t_{PHL}	6.233	3.616 + 0.052*CL	3.864 + 0.049*CL	3.997 + 0.047*CL
TN to PAD	t_R	5.184	1.433 + 0.075*CL	1.446 + 0.075*CL	1.438 + 0.075*CL
	t_F	5.801	1.980 + 0.076*CL	2.091 + 0.075*CL	2.137 + 0.074*CL
	t_{PLH}	5.281	3.204 + 0.042*CL	3.361 + 0.039*CL	3.442 + 0.038*CL
	t_{PHL}	6.309	3.693 + 0.052*CL	3.942 + 0.049*CL	4.073 + 0.047*CL
	t_{PLZ}	0.565	0.565 + 0.000*CL	0.565 + 0.000*CL	0.565 + 0.000*CL
	t_{PHZ}	0.435	0.435 + 0.000*CL	0.435 + 0.000*CL	0.435 + 0.000*CL
EN to PAD	t_R	5.184	1.433 + 0.075*CL	1.446 + 0.075*CL	1.438 + 0.075*CL
	t_F	5.801	1.980 + 0.076*CL	2.091 + 0.075*CL	2.136 + 0.074*CL
	t_{PLH}	5.351	3.273 + 0.042*CL	3.431 + 0.039*CL	3.511 + 0.038*CL
	t_{PHL}	6.379	3.763 + 0.052*CL	4.010 + 0.049*CL	4.143 + 0.047*CL
	t_{PLZ}	0.578	0.578 + 0.000*CL	0.578 + 0.000*CL	0.578 + 0.000*CL
	t_{PHZ}	0.447	0.447 + 0.000*CL	0.447 + 0.000*CL	0.447 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT12SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.656	2.014 + 0.053*CL	2.131 + 0.051*CL	2.184 + 0.051*CL
	t_F	4.377	1.826 + 0.051*CL	1.928 + 0.050*CL	1.968 + 0.049*CL
	t_{PLH}	5.343	3.537 + 0.036*CL	3.772 + 0.033*CL	3.902 + 0.031*CL
	t_{PHL}	4.910	3.008 + 0.038*CL	3.239 + 0.035*CL	3.358 + 0.034*CL
TN to PAD	t_R	4.659	2.016 + 0.053*CL	2.132 + 0.051*CL	2.185 + 0.051*CL
	t_F	4.380	1.831 + 0.051*CL	1.924 + 0.050*CL	1.970 + 0.049*CL
	t_{PLH}	5.423	3.616 + 0.036*CL	3.851 + 0.033*CL	3.982 + 0.031*CL
	t_{PHL}	4.987	3.091 + 0.038*CL	3.294 + 0.035*CL	3.436 + 0.034*CL
	t_{PLZ}	0.631	0.631 + 0.000*CL	0.631 + 0.000*CL	0.631 + 0.000*CL
	t_{PHZ}	0.431	0.431 + 0.000*CL	0.431 + 0.000*CL	0.431 + 0.000*CL
EN to PAD	t_R	4.659	2.015 + 0.053*CL	2.132 + 0.051*CL	2.186 + 0.051*CL
	t_F	4.380	1.831 + 0.051*CL	1.929 + 0.050*CL	1.970 + 0.049*CL
	t_{PLH}	5.493	3.687 + 0.036*CL	3.922 + 0.033*CL	4.051 + 0.031*CL
	t_{PHL}	5.059	3.163 + 0.038*CL	3.387 + 0.035*CL	3.506 + 0.034*CL
	t_{PLZ}	0.643	0.643 + 0.000*CL	0.643 + 0.000*CL	0.643 + 0.000*CL
	t_{PHZ}	0.444	0.444 + 0.000*CL	0.444 + 0.000*CL	0.444 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POT16SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.066	1.928 + 0.043*CL	2.070 + 0.041*CL	2.144 + 0.040*CL
	t_F	3.810	1.738 + 0.041*CL	1.876 + 0.040*CL	1.946 + 0.039*CL
	t_{PLH}	5.011	3.439 + 0.031*CL	3.665 + 0.028*CL	3.791 + 0.027*CL
	t_{PHL}	4.532	2.889 + 0.033*CL	3.110 + 0.030*CL	3.231 + 0.029*CL
TN to PAD	t_R	4.067	1.929 + 0.043*CL	2.071 + 0.041*CL	2.145 + 0.040*CL
	t_F	3.812	1.741 + 0.041*CL	1.886 + 0.039*CL	1.941 + 0.039*CL
	t_{PLH}	5.090	3.517 + 0.031*CL	3.744 + 0.028*CL	3.870 + 0.027*CL
	t_{PHL}	4.611	2.969 + 0.033*CL	3.203 + 0.030*CL	3.298 + 0.029*CL
	t_{PLZ}	0.664	0.664 + 0.000*CL	0.664 + 0.000*CL	0.663 + 0.000*CL
	t_{PHZ}	0.451	0.451 + 0.000*CL	0.451 + 0.000*CL	0.451 + 0.000*CL
EN to PAD	t_R	4.068	1.929 + 0.043*CL	2.072 + 0.041*CL	2.145 + 0.040*CL
	t_F	3.812	1.741 + 0.041*CL	1.885 + 0.040*CL	1.946 + 0.039*CL
	t_{PLH}	5.160	3.588 + 0.031*CL	3.813 + 0.028*CL	3.940 + 0.027*CL
	t_{PHL}	4.680	3.038 + 0.033*CL	3.273 + 0.030*CL	3.379 + 0.028*CL
	t_{PLZ}	0.675	0.675 + 0.000*CL	0.675 + 0.000*CL	0.675 + 0.000*CL
	t_{PHZ}	0.462	0.462 + 0.000*CL	0.462 + 0.000*CL	0.462 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT20SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.732	1.899 + 0.037*CL	2.047 + 0.035*CL	2.127 + 0.034*CL
	t_F	3.468	1.683 + 0.036*CL	1.830 + 0.034*CL	1.904 + 0.033*CL
	t_{PLH}	4.946	3.521 + 0.028*CL	3.737 + 0.026*CL	3.860 + 0.024*CL
	t_{PHL}	4.423	2.941 + 0.030*CL	3.153 + 0.027*CL	3.276 + 0.025*CL
TN to PAD	t_R	3.734	1.900 + 0.037*CL	2.049 + 0.035*CL	2.127 + 0.034*CL
	t_F	3.471	1.686 + 0.036*CL	1.832 + 0.034*CL	1.910 + 0.033*CL
	t_{PLH}	5.025	3.601 + 0.028*CL	3.814 + 0.026*CL	3.941 + 0.024*CL
	t_{PHL}	4.502	3.022 + 0.030*CL	3.234 + 0.027*CL	3.352 + 0.025*CL
	t_{PLZ}	0.696	0.696 + 0.000*CL	0.696 + 0.000*CL	0.696 + 0.000*CL
	t_{PHZ}	0.468	0.468 + 0.000*CL	0.468 + 0.000*CL	0.468 + 0.000*CL
EN to PAD	t_R	3.734	1.900 + 0.037*CL	2.048 + 0.035*CL	2.128 + 0.034*CL
	t_F	3.471	1.686 + 0.036*CL	1.832 + 0.034*CL	1.910 + 0.033*CL
	t_{PLH}	5.095	3.671 + 0.028*CL	3.886 + 0.026*CL	4.009 + 0.024*CL
	t_{PHL}	4.571	3.091 + 0.030*CL	3.303 + 0.027*CL	3.421 + 0.025*CL
	t_{PLZ}	0.708	0.707 + 0.000*CL	0.708 + 0.000*CL	0.708 + 0.000*CL
	t_{PHZ}	0.481	0.481 + 0.000*CL	0.481 + 0.000*CL	0.481 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POT24SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.548	1.919 + 0.033*CL	2.068 + 0.031*CL	2.150 + 0.030*CL
	t_F	3.270	1.682 + 0.032*CL	1.829 + 0.030*CL	1.909 + 0.029*CL
	t_{PLH}	5.005	3.673 + 0.027*CL	3.885 + 0.024*CL	4.005 + 0.022*CL
	t_{PHL}	4.442	3.066 + 0.028*CL	3.273 + 0.025*CL	3.391 + 0.023*CL
TN to PAD	t_R	3.550	1.920 + 0.033*CL	2.070 + 0.031*CL	2.151 + 0.030*CL
	t_F	3.273	1.685 + 0.032*CL	1.831 + 0.030*CL	1.911 + 0.029*CL
	t_{PLH}	5.084	3.752 + 0.027*CL	3.965 + 0.024*CL	4.084 + 0.022*CL
	t_{PHL}	4.523	3.149 + 0.027*CL	3.355 + 0.025*CL	3.472 + 0.023*CL
	t_{PLZ}	0.729	0.729 + 0.000*CL	0.728 + 0.000*CL	0.728 + 0.000*CL
	t_{PHZ}	0.487	0.487 + 0.000*CL	0.487 + 0.000*CL	0.487 + 0.000*CL
EN to PAD	t_R	3.550	1.921 + 0.033*CL	2.068 + 0.031*CL	2.152 + 0.030*CL
	t_F	3.273	1.685 + 0.032*CL	1.831 + 0.030*CL	1.912 + 0.029*CL
	t_{PLH}	5.154	3.823 + 0.027*CL	4.034 + 0.024*CL	4.154 + 0.022*CL
	t_{PHL}	4.592	3.218 + 0.027*CL	3.425 + 0.025*CL	3.541 + 0.023*CL
	t_{PLZ}	0.740	0.740 + 0.000*CL	0.740 + 0.000*CL	0.740 + 0.000*CL
	t_{PHZ}	0.500	0.500 + 0.000*CL	0.500 + 0.000*CL	0.500 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT12SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.074	3.057 + 0.060*CL	3.291 + 0.057*CL	3.417 + 0.056*CL
	t_F	4.037	1.478 + 0.051*CL	1.564 + 0.050*CL	1.600 + 0.050*CL
	t_{PLH}	7.759	5.403 + 0.047*CL	5.762 + 0.042*CL	5.963 + 0.040*CL
	t_{PHL}	4.703	2.906 + 0.036*CL	3.089 + 0.033*CL	3.189 + 0.032*CL
TN to PAD	t_R	6.077	3.059 + 0.060*CL	3.293 + 0.057*CL	3.420 + 0.056*CL
	t_F	4.039	1.479 + 0.051*CL	1.565 + 0.050*CL	1.601 + 0.050*CL
	t_{PLH}	7.838	5.481 + 0.047*CL	5.840 + 0.042*CL	6.042 + 0.040*CL
	t_{PHL}	4.780	2.983 + 0.036*CL	3.167 + 0.033*CL	3.265 + 0.032*CL
	t_{PLZ}	0.765	0.765 + 0.000*CL	0.765 + 0.000*CL	0.765 + 0.000*CL
	t_{PHZ}	0.500	0.500 + 0.000*CL	0.500 + 0.000*CL	0.500 + 0.000*CL
EN to PAD	t_R	6.077	3.059 + 0.060*CL	3.293 + 0.057*CL	3.420 + 0.056*CL
	t_F	4.039	1.480 + 0.051*CL	1.565 + 0.050*CL	1.601 + 0.050*CL
	t_{PLH}	7.908	5.551 + 0.047*CL	5.911 + 0.042*CL	6.110 + 0.040*CL
	t_{PHL}	4.850	3.055 + 0.036*CL	3.238 + 0.033*CL	3.334 + 0.032*CL
	t_{PLZ}	0.778	0.778 + 0.000*CL	0.778 + 0.000*CL	0.777 + 0.000*CL
	t_{PHZ}	0.512	0.512 + 0.000*CL	0.512 + 0.000*CL	0.512 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POT16SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.441	2.947 + 0.050*CL	3.182 + 0.047*CL	3.312 + 0.045*CL
	t_F	3.487	1.467 + 0.040*CL	1.575 + 0.039*CL	1.629 + 0.038*CL
	t_{PLH}	7.432	5.351 + 0.042*CL	5.689 + 0.037*CL	5.879 + 0.035*CL
	t_{PHL}	4.487	2.960 + 0.031*CL	3.145 + 0.028*CL	3.246 + 0.027*CL
TN to PAD	t_R	5.444	2.950 + 0.050*CL	3.184 + 0.047*CL	3.314 + 0.045*CL
	t_F	3.489	1.467 + 0.040*CL	1.577 + 0.039*CL	1.631 + 0.038*CL
	t_{PLH}	7.511	5.430 + 0.042*CL	5.767 + 0.037*CL	5.957 + 0.035*CL
	t_{PHL}	4.564	3.037 + 0.031*CL	3.226 + 0.028*CL	3.327 + 0.027*CL
	t_{PLZ}	0.799	0.799 + 0.000*CL	0.799 + 0.000*CL	0.799 + 0.000*CL
	t_{PHZ}	0.520	0.520 + 0.000*CL	0.520 + 0.000*CL	0.520 + 0.000*CL
EN to PAD	t_R	5.444	2.950 + 0.050*CL	3.184 + 0.047*CL	3.314 + 0.045*CL
	t_F	3.489	1.468 + 0.040*CL	1.575 + 0.039*CL	1.631 + 0.038*CL
	t_{PLH}	7.581	5.499 + 0.042*CL	5.837 + 0.037*CL	6.028 + 0.035*CL
	t_{PHL}	4.634	3.109 + 0.031*CL	3.292 + 0.028*CL	3.394 + 0.027*CL
	t_{PLZ}	0.810	0.810 + 0.000*CL	0.810 + 0.000*CL	0.810 + 0.000*CL
	t_{PHZ}	0.532	0.532 + 0.000*CL	0.532 + 0.000*CL	0.532 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT20SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.120	2.940 + 0.044*CL	3.172 + 0.041*CL	3.302 + 0.039*CL
	t_F	3.205	1.493 + 0.034*CL	1.613 + 0.033*CL	1.676 + 0.032*CL
	t_{PLH}	7.461	5.541 + 0.038*CL	5.866 + 0.034*CL	6.050 + 0.032*CL
	t_{PHL}	4.484	3.106 + 0.028*CL	3.292 + 0.025*CL	3.396 + 0.024*CL
TN to PAD	t_R	5.123	2.943 + 0.044*CL	3.174 + 0.041*CL	3.304 + 0.039*CL
	t_F	3.205	1.494 + 0.034*CL	1.613 + 0.033*CL	1.676 + 0.032*CL
	t_{PLH}	7.540	5.620 + 0.038*CL	5.944 + 0.034*CL	6.129 + 0.032*CL
	t_{PHL}	4.561	3.186 + 0.028*CL	3.372 + 0.025*CL	3.474 + 0.024*CL
	t_{PLZ}	0.832	0.832 + 0.000*CL	0.831 + 0.000*CL	0.831 + 0.000*CL
	t_{PHZ}	0.539	0.539 + 0.000*CL	0.539 + 0.000*CL	0.539 + 0.000*CL
EN to PAD	t_R	5.123	2.943 + 0.044*CL	3.174 + 0.041*CL	3.304 + 0.039*CL
	t_F	3.206	1.494 + 0.034*CL	1.613 + 0.033*CL	1.676 + 0.032*CL
	t_{PLH}	7.610	5.689 + 0.038*CL	6.016 + 0.034*CL	6.199 + 0.032*CL
	t_{PHL}	4.630	3.255 + 0.028*CL	3.440 + 0.025*CL	3.544 + 0.024*CL
	t_{PLZ}	0.843	0.843 + 0.000*CL	0.843 + 0.000*CL	0.843 + 0.000*CL
	t_{PHZ}	0.551	0.551 + 0.000*CL	0.551 + 0.000*CL	0.551 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POT24SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.973	2.999 + 0.039*CL	3.229 + 0.036*CL	3.357 + 0.035*CL
	t_F	3.058	1.544 + 0.030*CL	1.671 + 0.029*CL	1.738 + 0.028*CL
	t_{PLH}	7.645	5.821 + 0.036*CL	6.141 + 0.032*CL	6.323 + 0.030*CL
	t_{PHL}	4.570	3.278 + 0.026*CL	3.468 + 0.023*CL	3.575 + 0.022*CL
TN to PAD	t_R	4.976	3.002 + 0.039*CL	3.231 + 0.036*CL	3.359 + 0.035*CL
	t_F	3.059	1.545 + 0.030*CL	1.670 + 0.029*CL	1.739 + 0.028*CL
	t_{PLH}	7.724	5.900 + 0.036*CL	6.221 + 0.032*CL	6.402 + 0.030*CL
	t_{PHL}	4.651	3.362 + 0.026*CL	3.550 + 0.023*CL	3.656 + 0.022*CL
	t_{PLZ}	0.864	0.864 + 0.000*CL	0.864 + 0.000*CL	0.864 + 0.000*CL
	t_{PHZ}	0.557	0.557 + 0.000*CL	0.557 + 0.000*CL	0.557 + 0.000*CL
EN to PAD	t_R	4.976	3.002 + 0.039*CL	3.231 + 0.036*CL	3.359 + 0.035*CL
	t_F	3.059	1.544 + 0.030*CL	1.671 + 0.029*CL	1.739 + 0.028*CL
	t_{PLH}	7.795	5.970 + 0.036*CL	6.291 + 0.032*CL	6.473 + 0.030*CL
	t_{PHL}	4.718	3.426 + 0.026*CL	3.620 + 0.023*CL	3.725 + 0.022*CL
	t_{PLZ}	0.876	0.876 + 0.000*CL	0.876 + 0.000*CL	0.876 + 0.000*CL
	t_{PHZ}	0.570	0.570 + 0.000*CL	0.570 + 0.000*CL	0.570 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PTOT1

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	31.676	1.300 + 0.608*CL	1.316 + 0.607*CL	1.336 + 0.607*CL
	t_F	27.159	1.335 + 0.516*CL	1.334 + 0.516*CL	1.331 + 0.517*CL
	t_{PLH}	15.327	1.213 + 0.282*CL	1.211 + 0.282*CL	1.220 + 0.282*CL
	t_{PHL}	12.839	0.767 + 0.241*CL	0.785 + 0.241*CL	0.785 + 0.241*CL
TN to PAD	t_R	31.867	1.307 + 0.611*CL	1.329 + 0.611*CL	1.338 + 0.611*CL
	t_F	27.299	1.341 + 0.519*CL	1.345 + 0.519*CL	1.337 + 0.519*CL
	t_{PLH}	15.426	1.288 + 0.283*CL	1.300 + 0.283*CL	1.294 + 0.283*CL
	t_{PHL}	12.950	0.864 + 0.242*CL	0.880 + 0.242*CL	0.878 + 0.242*CL
	t_{PLZ}	0.464	0.464 + 0.000*CL	0.464 + 0.000*CL	0.464 + 0.000*CL
	t_{PHZ}	0.305	0.305 + 0.000*CL	0.305 + 0.000*CL	0.305 + 0.000*CL
EN to PAD	t_R	31.867	1.307 + 0.611*CL	1.329 + 0.611*CL	1.338 + 0.611*CL
	t_F	27.299	1.341 + 0.519*CL	1.345 + 0.519*CL	1.337 + 0.519*CL
	t_{PLH}	15.496	1.360 + 0.283*CL	1.362 + 0.283*CL	1.364 + 0.283*CL
	t_{PHL}	13.019	0.933 + 0.242*CL	0.950 + 0.241*CL	0.947 + 0.242*CL
	t_{PLZ}	0.475	0.475 + 0.000*CL	0.475 + 0.000*CL	0.475 + 0.000*CL
	t_{PHZ}	0.317	0.317 + 0.000*CL	0.317 + 0.000*CL	0.317 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

PTOT2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	15.957	0.747 + 0.304*CL	0.754 + 0.304*CL	0.769 + 0.304*CL
	t_F	13.657	0.743 + 0.258*CL	0.742 + 0.258*CL	0.744 + 0.258*CL
	t_{PLH}	8.002	0.937 + 0.141*CL	0.945 + 0.141*CL	0.951 + 0.141*CL
	t_{PHL}	6.629	0.581 + 0.121*CL	0.595 + 0.121*CL	0.599 + 0.121*CL
TN to PAD	t_R	16.005	0.747 + 0.305*CL	0.767 + 0.305*CL	0.775 + 0.305*CL
	t_F	13.692	0.746 + 0.259*CL	0.740 + 0.259*CL	0.746 + 0.259*CL
	t_{PLH}	8.085	1.014 + 0.141*CL	1.023 + 0.141*CL	1.026 + 0.141*CL
	t_{PHL}	6.728	0.677 + 0.121*CL	0.687 + 0.121*CL	0.695 + 0.121*CL
	t_{PLZ}	0.541	0.541 + 0.000*CL	0.541 + 0.000*CL	0.541 + 0.000*CL
	t_{PHZ}	0.332	0.332 + 0.000*CL	0.332 + 0.000*CL	0.332 + 0.000*CL
EN to PAD	t_R	16.005	0.747 + 0.305*CL	0.767 + 0.305*CL	0.775 + 0.305*CL
	t_F	13.692	0.746 + 0.259*CL	0.740 + 0.259*CL	0.746 + 0.259*CL
	t_{PLH}	8.156	1.087 + 0.141*CL	1.092 + 0.141*CL	1.095 + 0.141*CL
	t_{PHL}	6.798	0.746 + 0.121*CL	0.757 + 0.121*CL	0.764 + 0.121*CL
	t_{PLZ}	0.553	0.553 + 0.000*CL	0.552 + 0.000*CL	0.552 + 0.000*CL
	t_{PHZ}	0.344	0.344 + 0.000*CL	0.344 + 0.000*CL	0.344 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PTOT4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	8.092	0.465 + 0.153*CL	0.484 + 0.152*CL	0.486 + 0.152*CL
	t_F	6.891	0.433 + 0.129*CL	0.430 + 0.129*CL	0.436 + 0.129*CL
	t_{PLH}	4.448	0.907 + 0.071*CL	0.915 + 0.071*CL	0.919 + 0.071*CL
	t_{PHL}	3.599	0.568 + 0.061*CL	0.576 + 0.061*CL	0.580 + 0.060*CL
TN to PAD	t_R	8.105	0.466 + 0.153*CL	0.479 + 0.153*CL	0.490 + 0.152*CL
	t_F	6.901	0.436 + 0.129*CL	0.437 + 0.129*CL	0.434 + 0.129*CL
	t_{PLH}	4.527	0.984 + 0.071*CL	0.993 + 0.071*CL	0.997 + 0.071*CL
	t_{PHL}	3.693	0.661 + 0.061*CL	0.669 + 0.061*CL	0.673 + 0.060*CL
	t_{PLZ}	0.696	0.696 + 0.000*CL	0.695 + 0.000*CL	0.695 + 0.000*CL
	t_{PHZ}	0.332	0.332 + 0.000*CL	0.332 + 0.000*CL	0.332 + 0.000*CL
EN to PAD	t_R	8.105	0.466 + 0.153*CL	0.479 + 0.153*CL	0.490 + 0.152*CL
	t_F	6.901	0.436 + 0.129*CL	0.437 + 0.129*CL	0.434 + 0.129*CL
	t_{PLH}	4.597	1.055 + 0.071*CL	1.060 + 0.071*CL	1.066 + 0.071*CL
	t_{PHL}	3.762	0.730 + 0.061*CL	0.739 + 0.061*CL	0.742 + 0.060*CL
	t_{PLZ}	0.707	0.707 + 0.000*CL	0.706 + 0.000*CL	0.706 + 0.000*CL
	t_{PHZ}	0.344	0.344 + 0.000*CL	0.344 + 0.000*CL	0.344 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

PTOT6

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.486	0.404 + 0.102*CL	0.404 + 0.102*CL	0.404 + 0.102*CL
	t_F	4.628	0.325 + 0.086*CL	0.325 + 0.086*CL	0.324 + 0.086*CL
	t_{PLH}	3.358	0.990 + 0.047*CL	0.999 + 0.047*CL	1.003 + 0.047*CL
	t_{PHL}	2.571	0.547 + 0.040*CL	0.553 + 0.040*CL	0.556 + 0.040*CL
TN to PAD	t_R	5.492	0.405 + 0.102*CL	0.405 + 0.102*CL	0.408 + 0.102*CL
	t_F	4.636	0.332 + 0.086*CL	0.329 + 0.086*CL	0.328 + 0.086*CL
	t_{PLH}	3.436	1.068 + 0.047*CL	1.075 + 0.047*CL	1.080 + 0.047*CL
	t_{PHL}	2.664	0.639 + 0.041*CL	0.647 + 0.040*CL	0.649 + 0.040*CL
	t_{PLZ}	0.848	0.848 + 0.000*CL	0.847 + 0.000*CL	0.847 + 0.000*CL
	t_{PHZ}	0.508	0.508 + 0.000*CL	0.508 + 0.000*CL	0.508 + 0.000*CL
EN to PAD	t_R	5.492	0.405 + 0.102*CL	0.405 + 0.102*CL	0.408 + 0.102*CL
	t_F	4.636	0.332 + 0.086*CL	0.329 + 0.086*CL	0.328 + 0.086*CL
	t_{PLH}	3.506	1.137 + 0.047*CL	1.145 + 0.047*CL	1.149 + 0.047*CL
	t_{PHL}	2.733	0.708 + 0.041*CL	0.716 + 0.040*CL	0.719 + 0.040*CL
	t_{PLZ}	0.860	0.860 + 0.000*CL	0.859 + 0.000*CL	0.859 + 0.000*CL
	t_{PHZ}	0.521	0.521 + 0.000*CL	0.521 + 0.000*CL	0.521 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PTOT4SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	13.106	5.384 + 0.154*CL	5.724 + 0.150*CL	5.875 + 0.148*CL
	t_F	10.193	3.347 + 0.137*CL	3.648 + 0.133*CL	3.804 + 0.131*CL
	t_{PLH}	15.756	10.528 + 0.105*CL	11.170 + 0.096*CL	11.510 + 0.092*CL
	t_{PHL}	11.404	7.084 + 0.086*CL	7.527 + 0.080*CL	7.779 + 0.078*CL
TN to PAD	t_R	13.126	5.394 + 0.155*CL	5.735 + 0.150*CL	5.885 + 0.148*CL
	t_F	10.206	3.352 + 0.137*CL	3.650 + 0.133*CL	3.812 + 0.131*CL
	t_{PLH}	15.838	10.608 + 0.105*CL	11.245 + 0.096*CL	11.594 + 0.092*CL
	t_{PHL}	11.476	7.156 + 0.086*CL	7.598 + 0.081*CL	7.851 + 0.078*CL
	t_{PLZ}	0.928	0.928 + 0.000*CL	0.928 + 0.000*CL	0.927 + 0.000*CL
	t_{PHZ}	0.604	0.604 + 0.000*CL	0.604 + 0.000*CL	0.604 + 0.000*CL
EN to PAD	t_R	13.126	5.396 + 0.155*CL	5.726 + 0.150*CL	5.885 + 0.148*CL
	t_F	10.206	3.352 + 0.137*CL	3.650 + 0.133*CL	3.812 + 0.131*CL
	t_{PLH}	15.909	10.679 + 0.105*CL	11.317 + 0.096*CL	11.665 + 0.092*CL
	t_{PHL}	11.545	7.223 + 0.086*CL	7.676 + 0.080*CL	7.920 + 0.078*CL
	t_{PLZ}	0.939	0.939 + 0.000*CL	0.938 + 0.000*CL	0.938 + 0.000*CL
	t_{PHZ}	0.617	0.617 + 0.000*CL	0.617 + 0.000*CL	0.617 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

PTOT6SM

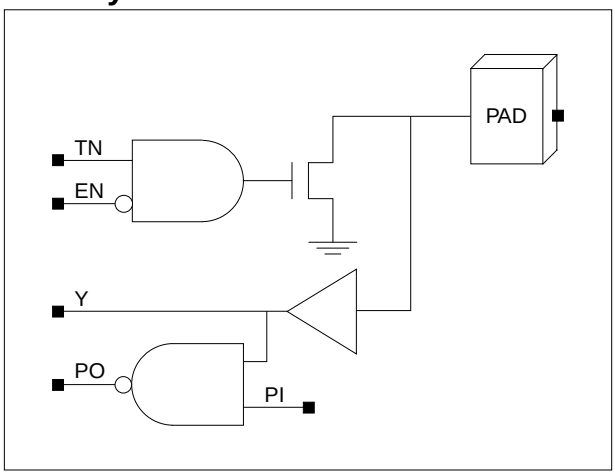
Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	12.005	5.997 + 0.120*CL	6.489 + 0.114*CL	6.761 + 0.110*CL
	t_F	8.272	3.314 + 0.099*CL	3.634 + 0.095*CL	3.812 + 0.093*CL
	t_{PLH}	15.911	11.171 + 0.095*CL	11.883 + 0.085*CL	12.283 + 0.081*CL
	t_{PHL}	11.368	7.838 + 0.071*CL	8.303 + 0.064*CL	8.558 + 0.061*CL
TN to PAD	t_R	12.018	6.004 + 0.120*CL	6.498 + 0.114*CL	6.767 + 0.111*CL
	t_F	8.280	3.318 + 0.099*CL	3.636 + 0.095*CL	3.817 + 0.093*CL
	t_{PLH}	15.994	11.252 + 0.095*CL	11.967 + 0.085*CL	12.367 + 0.081*CL
	t_{PHL}	11.438	7.908 + 0.071*CL	8.373 + 0.064*CL	8.628 + 0.061*CL
	t_{PLZ}	1.089	1.089 + 0.000*CL	1.088 + 0.000*CL	1.088 + 0.000*CL
	t_{PHZ}	0.633	0.633 + 0.000*CL	0.633 + 0.000*CL	0.633 + 0.000*CL
EN to PAD	t_R	12.018	6.004 + 0.120*CL	6.498 + 0.114*CL	6.772 + 0.110*CL
	t_F	8.280	3.318 + 0.099*CL	3.636 + 0.095*CL	3.817 + 0.093*CL
	t_{PLH}	16.064	11.322 + 0.095*CL	12.030 + 0.085*CL	12.438 + 0.081*CL
	t_{PHL}	11.507	7.975 + 0.071*CL	8.443 + 0.064*CL	8.704 + 0.061*CL
	t_{PLZ}	1.100	1.100 + 0.000*CL	1.099 + 0.000*CL	1.099 + 0.000*CL
	t_{PHZ}	0.645	0.645 + 0.000*CL	0.645 + 0.000*CL	0.645 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

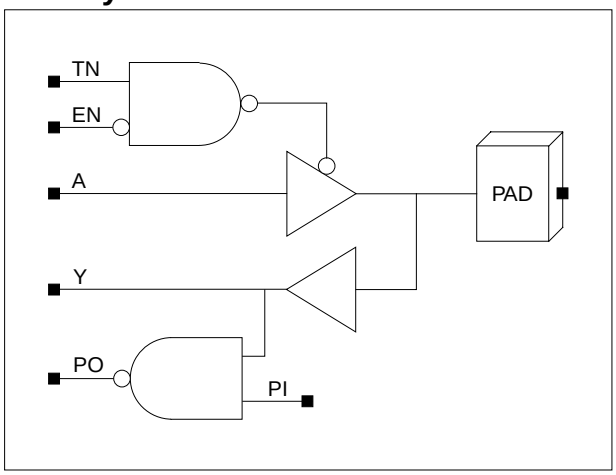
Cell List

Cell Name	Function Description
PBaDyz	3.3V Open-Drain Bi-Directional Buffers
PBaUDyz	3.3V Open-Drain Bi-Directional Buffers with Pull-Up
PBaTyz	3.3V Tri-State Bi-Directional Buffers
PBaDTyz	3.3V Tri-State Bi-Directional Buffers with Pull-Down
PBaUTyz	3.3V Tri-State Bi-Directional Buffers with Pull-Up
PTBaDy	5V - Tolerant Open-Drain Bi-Directional Buffers
PTBaUDy	5V - Tolerant Open-Drain Bi-Directional Buffers with Pull-Up
PTBaTy	5V - Tolerant Tri-State Bi-Directional Buffers
PTBaDT	5V - Tolerant Tri-State Bi-Directional Buffers with Pull-Down
PTBaUT	5V - Tolerant Tri-State Bi-Directional Buffers with Pull-Up

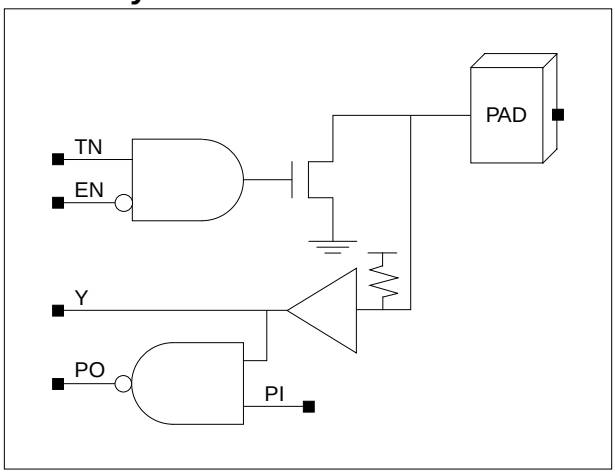
PvBaDyz



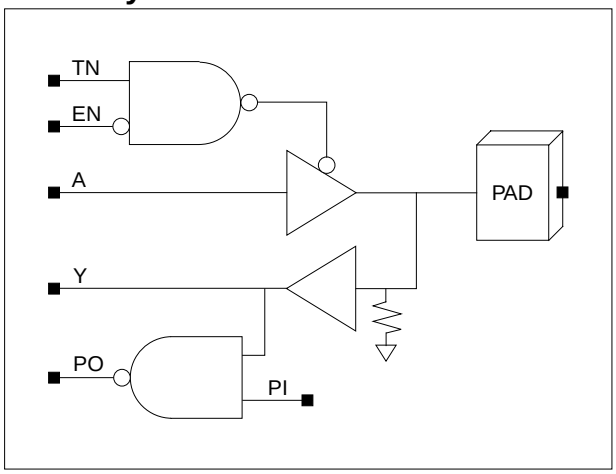
PvBaTyz



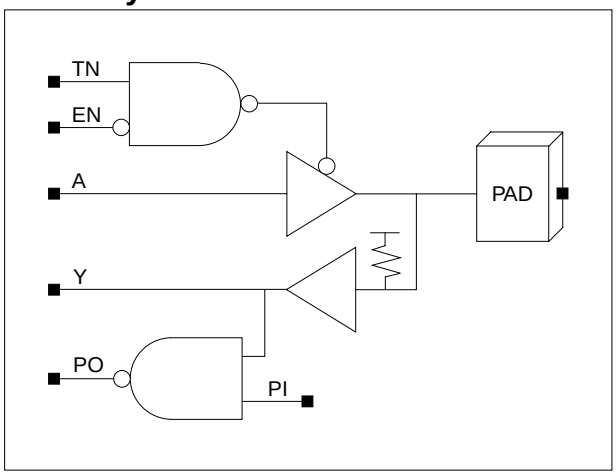
PvBaUDyz



PvBaDTyz



PvBaUTyz



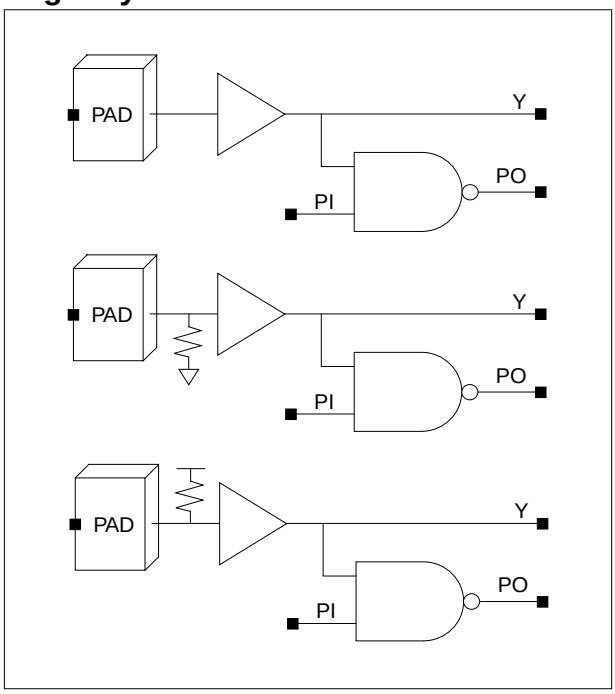
Cell List

Cell Name	Function Description
PSCKDC(2/4/6/8/12)	LVCMOS Level Input Clock Driver
PSCKDCD(2/4/6/8/12)	LVCMOS Level Input clock Driver with Pull-Down
PSCKDCU(2/4/6/8/12)	LVCMOS Level Input clock Driver with Pull-Up
PSCKDS(2/4/6/8/12)	LVCMOS-Schmitt Trigger Level Input Clock Drivers
PSCKDSD(2/4/6/8/12)	LVCMOS-Schmitt Trigger Level Input Clock Driver with Pull-Down
PSCKDSU(2/4/6/8/12)	LVCMOS-Schmitt Trigger Level Input Clock Driver with Pull-Up

PSCKDCby

LVCMOS Level Input Clock Drivers

Logic Symbol



Cell Availability

Only 3.3V
PSCKDC/PSCKDCD/PSCKDCU (2/4/6/8/12)

Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
PSCKDC/PSCKDCD/PSCKDCU (2/4/6/8/12)	3.417

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.60ns, SL: Standard Load)

PSCKDC2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.140	0.131 + 0.004*SL	0.080 + 0.005*SL	0.070 + 0.005*SL
	t_F	0.132	0.122 + 0.005*SL	0.073 + 0.005*SL	0.062 + 0.005*SL
	t_{PLH}	0.127	0.123 + 0.002*SL	0.144 + 0.002*SL	0.143 + 0.002*SL
	t_{PHL}	0.480	0.475 + 0.003*SL	0.490 + 0.003*SL	0.488 + 0.003*SL

*Group1 : SL < 205, *Group2 : 205 ≦ SL ≦ 410, *Group3 : 410 < SL

PSCKDC4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.157	0.153 + 0.002*SL	0.082 + 0.002*SL	0.063 + 0.002*SL
	t_F	0.145	0.140 + 0.002*SL	0.075 + 0.003*SL	0.059 + 0.003*SL
	t_{PLH}	0.204	0.201 + 0.001*SL	0.229 + 0.001*SL	0.227 + 0.001*SL
	t_{PHL}	0.569	0.566 + 0.001*SL	0.587 + 0.001*SL	0.584 + 0.001*SL

*Group1 : SL < 405, *Group2 : 405 ≦ SL ≦ 809, *Group3 : 809 < SL

PSCKDC6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.176	0.174 + 0.001*SL	0.093 + 0.002*SL	0.067 + 0.002*SL
	t_F	0.166	0.163 + 0.002*SL	0.090 + 0.002*SL	0.067 + 0.002*SL
	t_{PLH}	0.270	0.268 + 0.001*SL	0.305 + 0.001*SL	0.301 + 0.001*SL
	t_{PHL}	0.648	0.646 + 0.001*SL	0.675 + 0.001*SL	0.671 + 0.001*SL

*Group1 : SL < 604, *Group2 : 604 ≦ SL ≦ 1209, *Group3 : 1209 < SL

PSCKDC8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.194	0.192 + 0.001*SL	0.107 + 0.001*SL	0.076 + 0.001*SL
	t_F	0.188	0.186 + 0.001*SL	0.111 + 0.001*SL	0.079 + 0.001*SL
	t_{PLH}	0.330	0.328 + 0.001*SL	0.373 + 0.001*SL	0.369 + 0.001*SL
	t_{PHL}	0.719	0.718 + 0.001*SL	0.759 + 0.001*SL	0.753 + 0.001*SL

*Group1 : SL < 802, *Group2 : 802 ≦ SL ≦ 1603, *Group3 : 1603 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.60ns, SL: Standard Load)

PSCKDC12

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.228	0.226 + 0.001*SL	0.138 + 0.001*SL	0.099 + 0.001*SL
	t_F	0.232	0.231 + 0.001*SL	0.156 + 0.001*SL	0.110 + 0.001*SL
	t_{PLH}	0.435	0.434 + 0.000*SL	0.497 + 0.000*SL	0.493 + 0.000*SL
	t_{PHL}	0.852	0.851 + 0.001*SL	0.912 + 0.000*SL	0.906 + 0.000*SL

*Group1 : SL < 1201, *Group2 : 1201 ≦ SL ≦ 2402, *Group3 : 2402 < SL

PSCKDCD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.140	0.131 + 0.004*SL	0.079 + 0.005*SL	0.069 + 0.005*SL
	t_F	0.132	0.122 + 0.005*SL	0.074 + 0.005*SL	0.063 + 0.005*SL
	t_{PLH}	0.139	0.135 + 0.002*SL	0.155 + 0.002*SL	0.155 + 0.002*SL
	t_{PHL}	0.486	0.480 + 0.003*SL	0.495 + 0.003*SL	0.494 + 0.003*SL

*Group1 : SL < 205, *Group2 : 205 ≦SL ≦ 410, *Group3 : 410 < SL

PSCKDCD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.155	0.151 + 0.002*SL	0.081 + 0.002*SL	0.063 + 0.002*SL
	t_F	0.146	0.141 + 0.002*SL	0.075 + 0.003*SL	0.059 + 0.003*SL
	t_{PLH}	0.215	0.213 + 0.001*SL	0.240 + 0.001*SL	0.238 + 0.001*SL
	t_{PHL}	0.575	0.572 + 0.001*SL	0.593 + 0.001*SL	0.589 + 0.001*SL

*Group1 : SL < 405, *Group2 : 405 ≦ SL ≦ 809, *Group3 : 809 < SL

PSCKDCD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.175	0.172 + 0.001*SL	0.092 + 0.002*SL	0.067 + 0.002*SL
	t_F	0.167	0.164 + 0.002*SL	0.091 + 0.002*SL	0.067 + 0.002*SL
	t_{PLH}	0.281	0.279 + 0.001*SL	0.315 + 0.001*SL	0.312 + 0.001*SL
	t_{PHL}	0.654	0.652 + 0.001*SL	0.682 + 0.001*SL	0.677 + 0.001*SL

*Group1 : SL < 604, *Group2 : 604 ≦ SL ≦ 1209, *Group3 : 1209 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.60ns, SL: Standard Load)

PSCKDCD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.193	0.191 + 0.001*SL	0.106 + 0.001*SL	0.076 + 0.001*SL
	t_F	0.189	0.187 + 0.001*SL	0.111 + 0.001*SL	0.079 + 0.001*SL
	t_{PLH}	0.340	0.339 + 0.001*SL	0.383 + 0.001*SL	0.379 + 0.001*SL
	t_{PHL}	0.726	0.725 + 0.001*SL	0.765 + 0.001*SL	0.759 + 0.001*SL

*Group1 : SL < 802, *Group2 : 802 ≦SL ≦ 1603, *Group3 : 1603 < SL

PSCKDCD12

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.227	0.225 + 0.001*SL	0.138 + 0.001*SL	0.099 + 0.001*SL
	t_F	0.233	0.231 + 0.001*SL	0.157 + 0.001*SL	0.111 + 0.001*SL
	t_{PLH}	0.445	0.444 + 0.000*SL	0.507 + 0.000*SL	0.502 + 0.000*SL
	t_{PHL}	0.858	0.857 + 0.001*SL	0.919 + 0.000*SL	0.913 + 0.000*SL

*Group1 : SL < 1201, *Group2 : 1201 ≦ SL ≦ 2402, *Group3 : 2402 < SL

PSCKDCU2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.141	0.133 + 0.004*SL	0.081 + 0.005*SL	0.071 + 0.005*SL
	t_F	0.131	0.121 + 0.005*SL	0.073 + 0.005*SL	0.062 + 0.005*SL
	t_{PLH}	0.125	0.120 + 0.002*SL	0.142 + 0.002*SL	0.141 + 0.002*SL
	t_{PHL}	0.494	0.488 + 0.003*SL	0.504 + 0.003*SL	0.502 + 0.003*SL

*Group1 : SL < 205, *Group2 : 205 ≦SL ≦ 410, *Group3 : 410 < SL

PSCKDCU4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.159	0.154 + 0.002*SL	0.083 + 0.002*SL	0.064 + 0.002*SL
	t_F	0.144	0.139 + 0.002*SL	0.075 + 0.003*SL	0.059 + 0.003*SL
	t_{PLH}	0.202	0.200 + 0.001*SL	0.228 + 0.001*SL	0.226 + 0.001*SL
	t_{PHL}	0.582	0.579 + 0.001*SL	0.600 + 0.001*SL	0.597 + 0.001*SL

*Group1 : SL < 405, *Group2 : 405 ≦ SL ≦ 809, *Group3 : 809 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.60ns, SL: Standard Load)

PSCKDCU6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.178	0.175 + 0.001*SL	0.094 + 0.002*SL	0.068 + 0.002*SL
	t_F	0.166	0.163 + 0.002*SL	0.090 + 0.002*SL	0.067 + 0.002*SL
	t_{PLH}	0.269	0.267 + 0.001*SL	0.304 + 0.001*SL	0.301 + 0.001*SL
	t_{PHL}	0.661	0.659 + 0.001*SL	0.689 + 0.001*SL	0.684 + 0.001*SL

*Group1 : SL < 604, *Group2 : 604 ≦ SL ≦ 1209, *Group3 : 1209 < SL

PSCKDCU8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.196	0.194 + 0.001*SL	0.108 + 0.001*SL	0.077 + 0.001*SL
	t_F	0.188	0.186 + 0.001*SL	0.111 + 0.001*SL	0.079 + 0.001*SL
	t_{PLH}	0.329	0.328 + 0.001*SL	0.373 + 0.001*SL	0.369 + 0.001*SL
	t_{PHL}	0.733	0.731 + 0.001*SL	0.772 + 0.001*SL	0.766 + 0.001*SL

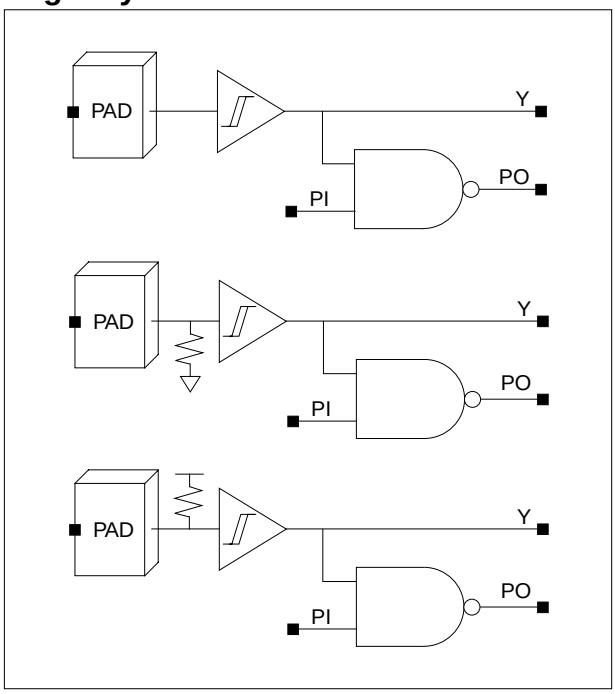
*Group1 : SL < 802, *Group2 : 802 ≦SL ≦ 1603, *Group3 : 1603 < SL

PSCKDCU12

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.229	0.228 + 0.001*SL	0.139 + 0.001*SL	0.100 + 0.001*SL
	t_F	0.232	0.231 + 0.001*SL	0.156 + 0.001*SL	0.111 + 0.001*SL
	t_{PLH}	0.436	0.435 + 0.000*SL	0.498 + 0.000*SL	0.493 + 0.000*SL
	t_{PHL}	0.865	0.864 + 0.001*SL	0.925 + 0.000*SL	0.919 + 0.000*SL

*Group1 : SL < 1201, *Group2 : 1201 ≦ SL ≦ 2402, *Group3 : 2402 < SL

Logic Symbol



Cell Availability

Only 5V
PSCKDS/PSCKDSD/PSCKDSU(2/4/6/8/12)

Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

	PI
PSCKDS/PSCKDSD/PSCKDSU (2/4/6/8/12)	3.417

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.60ns, SL: Standard Load)

PSCKDS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.122	0.113 + 0.004*SL	0.076 + 0.005*SL	0.066 + 0.005*SL
	t_F	0.130	0.120 + 0.005*SL	0.087 + 0.005*SL	0.073 + 0.005*SL
	t_{PLH}	0.500	0.496 + 0.002*SL	0.517 + 0.002*SL	0.517 + 0.002*SL
	t_{PHL}	0.508	0.503 + 0.003*SL	0.533 + 0.003*SL	0.532 + 0.003*SL

*Group1 : SL < 205, *Group2 : 205 ≦ SL ≦ 410, *Group3 : 410 < SL

PSCKDS4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.144	0.139 + 0.002*SL	0.093 + 0.002*SL	0.075 + 0.002*SL
	t_F	0.153	0.148 + 0.003*SL	0.102 + 0.003*SL	0.078 + 0.003*SL
	t_{PLH}	0.596	0.593 + 0.001*SL	0.632 + 0.001*SL	0.631 + 0.001*SL
	t_{PHL}	0.631	0.628 + 0.002*SL	0.672 + 0.001*SL	0.670 + 0.001*SL

*Group1 : SL < 405, *Group2 : 405 ≦ SL ≦ 809, *Group3 : 809 < SL

PSCKDS6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.169	0.167 + 0.001*SL	0.117 + 0.002*SL	0.092 + 0.002*SL
	t_F	0.182	0.178 + 0.002*SL	0.128 + 0.002*SL	0.097 + 0.002*SL
	t_{PLH}	0.680	0.678 + 0.001*SL	0.734 + 0.001*SL	0.734 + 0.001*SL
	t_{PHL}	0.740	0.738 + 0.001*SL	0.795 + 0.001*SL	0.794 + 0.001*SL

*Group1 : SL < 604, *Group2 : 604 ≦ SL ≦ 1209, *Group3 : 1209 < SL

PSCKDS8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.195	0.193 + 0.001*SL	0.143 + 0.001*SL	0.113 + 0.001*SL
	t_F	0.210	0.207 + 0.001*SL	0.161 + 0.001*SL	0.122 + 0.001*SL
	t_{PLH}	0.757	0.755 + 0.001*SL	0.827 + 0.001*SL	0.827 + 0.001*SL
	t_{PHL}	0.838	0.837 + 0.001*SL	0.909 + 0.001*SL	0.909 + 0.001*SL

*Group1 : SL < 802, *Group2 : 802 ≦ SL ≦ 1603, *Group3 : 1603 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.60ns, SL: Standard Load)

PSCKDS12

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.242	0.241 + 0.001*SL	0.194 + 0.001*SL	0.161 + 0.001*SL
	t_F	0.279	0.277 + 0.001*SL	0.237 + 0.001*SL	0.186 + 0.001*SL
	t_{PLH}	0.895	0.894 + 0.000*SL	0.990 + 0.000*SL	0.997 + 0.000*SL
	t_{PHL}	1.020	1.019 + 0.001*SL	1.122 + 0.000*SL	1.130 + 0.000*SL

*Group1 : SL < 1201, *Group2 : 1201 ≦ SL ≦ 2402, *Group3 : 2402 < SL

PSCKDSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.121	0.112 + 0.004*SL	0.076 + 0.005*SL	0.066 + 0.005*SL
	t_F	0.130	0.120 + 0.005*SL	0.087 + 0.005*SL	0.073 + 0.005*SL
	t_{PLH}	0.508	0.504 + 0.002*SL	0.525 + 0.002*SL	0.525 + 0.002*SL
	t_{PHL}	0.515	0.509 + 0.003*SL	0.540 + 0.003*SL	0.539 + 0.003*SL

*Group1 : SL < 205, *Group2 : 205 ≦ SL ≦ 410, *Group3 : 410 < SL

PSCKDSD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.143	0.139 + 0.002*SL	0.093 + 0.002*SL	0.074 + 0.002*SL
	t_F	0.153	0.148 + 0.003*SL	0.102 + 0.003*SL	0.078 + 0.003*SL
	t_{PLH}	0.603	0.600 + 0.001*SL	0.639 + 0.001*SL	0.638 + 0.001*SL
	t_{PHL}	0.638	0.635 + 0.002*SL	0.679 + 0.001*SL	0.677 + 0.001*SL

*Group1 : SL < 405, *Group2 : 405 ≦ SL ≦ 809, *Group3 : 809 < SL

PSCKDSD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.170	0.167 + 0.001*SL	0.117 + 0.002*SL	0.092 + 0.002*SL
	t_F	0.182	0.179 + 0.002*SL	0.128 + 0.002*SL	0.097 + 0.002*SL
	t_{PLH}	0.687	0.685 + 0.001*SL	0.742 + 0.001*SL	0.741 + 0.001*SL
	t_{PHL}	0.748	0.746 + 0.001*SL	0.803 + 0.001*SL	0.802 + 0.001*SL

*Group1 : SL < 604, *Group2 : 604 ≦ SL ≦ 1209, *Group3 : 1209 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.60ns, SL: Standard Load)

PSCKDSD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.195	0.193 + 0.001*SL	0.143 + 0.001*SL	0.113 + 0.001*SL
	t_F	0.211	0.208 + 0.001*SL	0.161 + 0.001*SL	0.123 + 0.001*SL
	t_{PLH}	0.765	0.763 + 0.001*SL	0.834 + 0.001*SL	0.834 + 0.001*SL
	t_{PHL}	0.847	0.845 + 0.001*SL	0.917 + 0.001*SL	0.918 + 0.001*SL

*Group1 : SL < 802, *Group2 : 802 ≦ SL ≦ 1603, *Group3 : 1603 < SL

PSCKDSD12

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.244	0.242 + 0.001*SL	0.194 + 0.001*SL	0.161 + 0.001*SL
	t_F	0.279	0.277 + 0.001*SL	0.237 + 0.001*SL	0.186 + 0.001*SL
	t_{PLH}	0.901	0.900 + 0.000*SL	0.997 + 0.000*SL	1.004 + 0.000*SL
	t_{PHL}	1.030	1.028 + 0.001*SL	1.131 + 0.000*SL	1.139 + 0.000*SL

*Group1 : SL < 1201, *Group2 : 1201 ≦ SL ≦ 2402, *Group3 : 2402 < SL

PSCKDSU2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.122	0.114 + 0.004*SL	0.076 + 0.005*SL	0.067 + 0.005*SL
	t_F	0.129	0.119 + 0.005*SL	0.087 + 0.005*SL	0.073 + 0.005*SL
	t_{PLH}	0.503	0.498 + 0.002*SL	0.518 + 0.002*SL	0.519 + 0.002*SL
	t_{PHL}	0.521	0.515 + 0.003*SL	0.545 + 0.003*SL	0.545 + 0.003*SL

*Group1 : SL < 205, *Group2 : 205 ≦ SL ≦ 410, *Group3 : 410 < SL

PSCKDSU4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.144	0.140 + 0.002*SL	0.094 + 0.002*SL	0.075 + 0.002*SL
	t_F	0.153	0.148 + 0.003*SL	0.101 + 0.003*SL	0.078 + 0.003*SL
	t_{PLH}	0.599	0.597 + 0.001*SL	0.636 + 0.001*SL	0.635 + 0.001*SL
	t_{PHL}	0.643	0.640 + 0.002*SL	0.684 + 0.001*SL	0.682 + 0.001*SL

*Group1 : SL < 405, *Group2 : 405 ≦ SL ≦ 809, *Group3 : 809 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.60ns, SL: Standard Load)

PSCKDSU6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.171	0.168 + 0.001*SL	0.118 + 0.002*SL	0.092 + 0.002*SL
	t_F	0.182	0.178 + 0.002*SL	0.128 + 0.002*SL	0.097 + 0.002*SL
	t_{PLH}	0.684	0.682 + 0.001*SL	0.738 + 0.001*SL	0.737 + 0.001*SL
	t_{PHL}	0.753	0.751 + 0.001*SL	0.807 + 0.001*SL	0.806 + 0.001*SL

*Group1 : SL < 604, *Group2 : 604 ≦ SL ≦ 1209, *Group3 : 1209 < SL

PSCKDSU8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.196	0.194 + 0.001*SL	0.143 + 0.001*SL	0.113 + 0.001*SL
	t_F	0.210	0.208 + 0.001*SL	0.161 + 0.001*SL	0.122 + 0.001*SL
	t_{PLH}	0.762	0.760 + 0.001*SL	0.832 + 0.001*SL	0.833 + 0.001*SL
	t_{PHL}	0.850	0.849 + 0.001*SL	0.921 + 0.001*SL	0.922 + 0.001*SL

*Group1 : SL < 802, *Group2 : 802 ≦ SL ≦ 1603, *Group3 : 1603 < SL

PSCKDSU12

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.245	0.243 + 0.001*SL	0.195 + 0.001*SL	0.161 + 0.001*SL
	t_F	0.280	0.278 + 0.001*SL	0.239 + 0.001*SL	0.187 + 0.001*SL
	t_{PLH}	0.901	0.900 + 0.000*SL	0.996 + 0.000*SL	1.003 + 0.000*SL
	t_{PHL}	1.034	1.033 + 0.001*SL	1.136 + 0.000*SL	1.144 + 0.000*SL

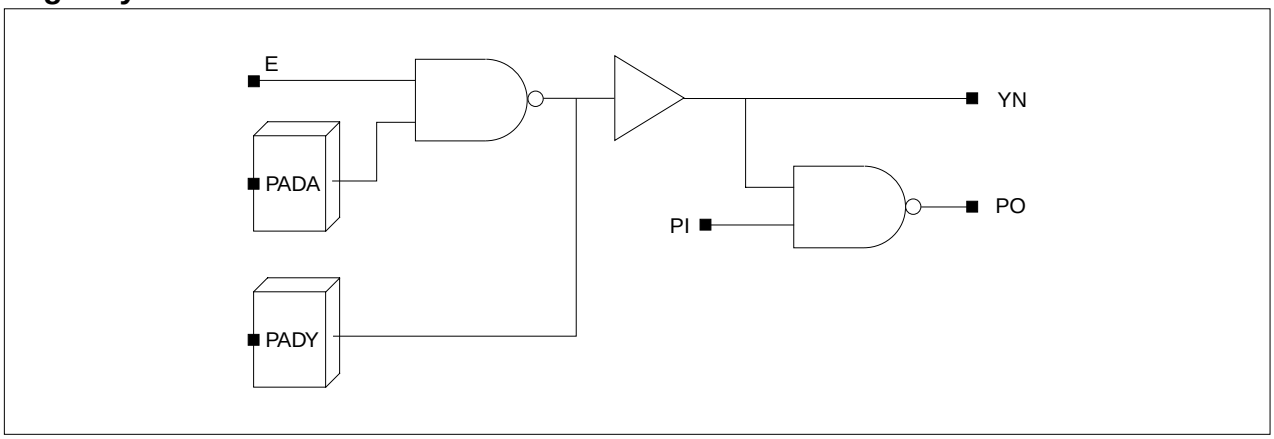
*Group1 : SL < 1201, *Group2 : 1201 ≦ SL ≦ 2402, *Group3 : 2402 < SL

OSCILLATORS

Cell List

Cell Name	Function Description
PSOSCK1	Oscillator Cell with Enable (~ 100KHz)
PSOSCK2	Oscillator Cell with Enable (100K ~ 1MHz)
PSOSCK17	Oscillator Cell with Enable and 10Mohm Resistor (~ 100KHz)
PSOSCK27	Oscillator Cell with Enable and 10Mohm Resistor (100K ~ 1MHz)
PSOSCM1	Oscillator Cell with Enable (1M ~ 10MHz)
PSOSCM2	Oscillator Cell with Enable (10M ~ 40MHz)
PSOSCM3	Oscillator Cell with Enable (40M ~ 100MHz)
PSOSCM16	Oscillator Cell with Enable and 1Mohm Resistor (1M ~ 10MHz)
PSOSCM26	Oscillator Cell with Enable and 1Mohm Resistor (10M ~ 40MHz)
PSOSCM36	Oscillator Cell with Enable and 1Mohm Resistor (40M ~ 100MHz)

Logic Symbol



Truth Table

PADA	E	PADY	YN	PI	PO
0	0	1	1	0	1
0	0	1	1	1	0
0	1	1	1	0	1
0	1	1	1	1	0
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)	I/O Sizes
PSOSCK1/2	*PSOSCK1/2*
E	
3.86	2 I/O SLOTS

PSOSCK(1/2)

Oscillator Cell with Enable

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.80ns, CL: Capacitive Load[pf])

PSOSCK1

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	tR	873.780	25.540 + 0.004*CL	25.900 + 0.004*CL	25.333 + 0.187*CL
	tF	1965.400	1895.600 + 0.000*CL	56.927 + 0.029*CL	56.933 + 0.420*CL
	tPLH	391.540	12.080 + 0.002*CL	12.095 + 0.002*CL	12.066 + 0.083*CL
	tPHL	895.870	27.810 + 0.004*CL	27.900 + 0.004*CL	27.900 + 0.191*CL
E to PADY	tR	873.770	25.510 + 0.004*CL	25.900 + 0.004*CL	25.333 + 0.187*CL
	tF	1965.400	1895.600 + 0.000*CL	56.927 + 0.029*CL	56.933 + 0.420*CL
	tPLH	391.480	12.020 + 0.002*CL	12.035 + 0.002*CL	12.006 + 0.083*CL
	tPHL	895.910	27.930 + 0.004*CL	27.900 + 0.004*CL	27.900 + 0.191*CL

*Group1 : CL < 75, *Group2 : 75 ≤ CL ≤ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.80ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADY to YN	tR	0.281	0.241 + 0.020*SL	0.241 + 0.020*SL	0.205 + 0.021*SL
	tF	0.272	0.236 + 0.018*SL	0.231 + 0.019*SL	0.187 + 0.020*SL
	tPLH	19.082	19.056 + 0.013*SL	19.067 + 0.010*SL	19.101 + 0.009*SL
	tPHL	12.083	12.055 + 0.014*SL	12.066 + 0.011*SL	12.097 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 45, *Group3 : 45 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.80ns, CL: Capacitive Load[pf])

PSOSCK2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	tR	133.070	3.930 + 0.001*CL	3.915 + 0.001*CL	3.943 + 0.028*CL
	tF	233.040	6.740 + 0.001*CL	6.740 + 0.001*CL	6.740 + 0.050*CL
	tPLH	48.351	1.995 + 0.000*CL	1.981 + 0.000*CL	2.001 + 0.010*CL
	tPHL	94.380	3.400 + 0.000*CL	3.370 + 0.000*CL	3.370 + 0.020*CL
E to PADY	tR	133.060	3.920 + 0.001*CL	3.905 + 0.001*CL	3.876 + 0.028*CL
	tF	233.040	6.740 + 0.001*CL	6.740 + 0.001*CL	6.740 + 0.050*CL
	tPLH	48.277	1.919 + 0.000*CL	1.916 + 0.000*CL	1.922 + 0.010*CL
	tPHL	94.392	3.416 + 0.000*CL	3.380 + 0.000*CL	3.380 + 0.020*CL

*Group1 : CL < 75, *Group2 : 75 ≤ CL ≤ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.80ns] **(SL : Standard Load)**

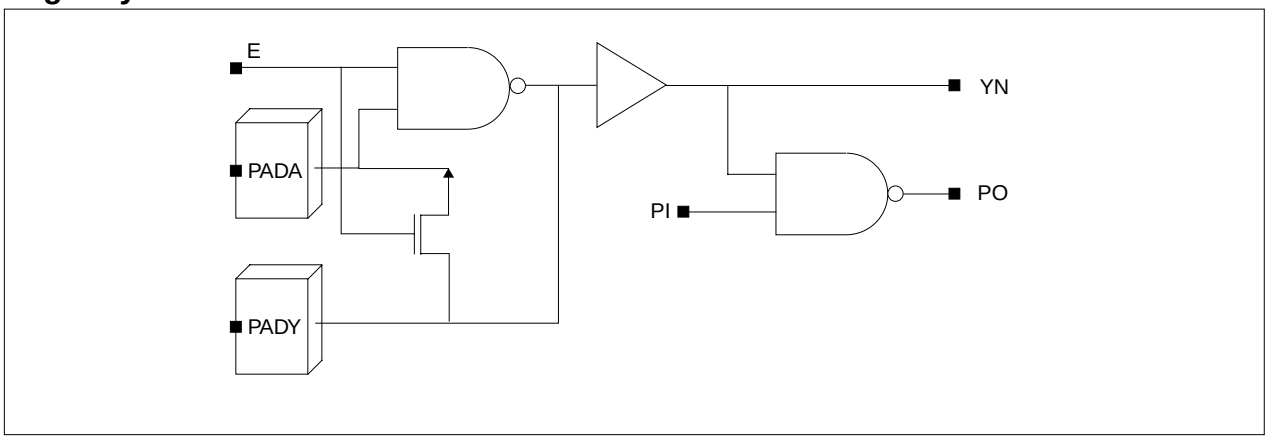
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADY to YN	tR	0.282	0.242 + 0.020*SL	0.241 + 0.020*SL	0.205 + 0.021*SL
	tF	0.282	0.246 + 0.018*SL	0.242 + 0.019*SL	0.197 + 0.020*SL
	tPLH	17.492	17.466 + 0.013*SL	17.478 + 0.010*SL	17.512 + 0.009*SL
	tPHL	17.405	17.377 + 0.014*SL	17.388 + 0.011*SL	17.418 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 45, *Group3 : 45 < SL

PSOSCK(17/27)

Oscillator Cell with Enable and 10Mohm Resistor

Logic Symbol



Truth Table

PADA	E	PADY	YN	PI	PO
0	0	1	1	0	1
0	0	1	1	1	0
0	1	1	1	0	1
0	1	1	1	1	0
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)	I/O Sizes
PSOSCK17/27	*PSOSCK17/27*
E	
3.86	2 I/O SLOTS

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.80ns, CL: Capacitive Load[pf])

PSOSCK17

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	tR	881.470	27.210 + 0.004*CL	27.600 + 0.004*CL	27.034 + 0.188*CL
	tF	2046.100	110.300 + 0.009*CL	111.000 + 0.009*CL	61.100 + 0.437*CL
	tPLH	384.840	12.200 + 0.002*CL	12.185 + 0.002*CL	12.213 + 0.082*CL
	tPHL	905.620	30.460 + 0.004*CL	30.700 + 0.004*CL	30.700 + 0.192*CL
E to PADY	tR	873.810	25.630 + 0.004*CL	25.900 + 0.004*CL	25.333 + 0.187*CL
	tF	2046.100	110.300 + 0.009*CL	111.000 + 0.009*CL	61.100 + 0.437*CL
	tPLH	384.520	11.920 + 0.002*CL	11.920 + 0.002*CL	11.920 + 0.082*CL
	tPHL	910.040	28.520 + 0.004*CL	28.551 + 0.004*CL	28.267 + 0.194*CL

*Group1 : CL < 75, *Group2 : 75 ≤ CL ≤ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.80ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADY to YN	tR	0.281	0.241 + 0.020*SL	0.241 + 0.020*SL	0.205 + 0.021*SL
	tF	0.271	0.235 + 0.018*SL	0.232 + 0.019*SL	0.187 + 0.020*SL
	tPLH	19.081	19.055 + 0.013*SL	19.066 + 0.010*SL	19.101 + 0.009*SL
	tPHL	12.087	12.059 + 0.014*SL	12.070 + 0.011*SL	12.101 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 45, *Group3 : 45 < SL

PSOSCK(17/27)

Oscillator Cell with Enable and 10Mohm Resistor

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.80ns, CL: Capacitive Load[pf])

PSOSCK27

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	tR	133.360	4.060 + 0.001*CL	4.060 + 0.001*CL	4.060 + 0.028*CL
	tF	234.130	6.870 + 0.001*CL	6.885 + 0.001*CL	6.857 + 0.050*CL
	tPLH	48.357	2.067 + 0.000*CL	2.074 + 0.000*CL	2.072 + 0.010*CL
	tPHL	94.787	3.681 + 0.000*CL	3.690 + 0.000*CL	3.690 + 0.020*CL
E to PADY	tR	133.060	3.920 + 0.001*CL	3.905 + 0.001*CL	3.876 + 0.028*CL
	tF	234.130	6.870 + 0.001*CL	6.885 + 0.001*CL	6.857 + 0.050*CL
	tPLH	48.300	2.016 + 0.000*CL	2.022 + 0.000*CL	2.022 + 0.010*CL
	tPHL	94.794	3.622 + 0.000*CL	3.580 + 0.000*CL	3.580 + 0.020*CL

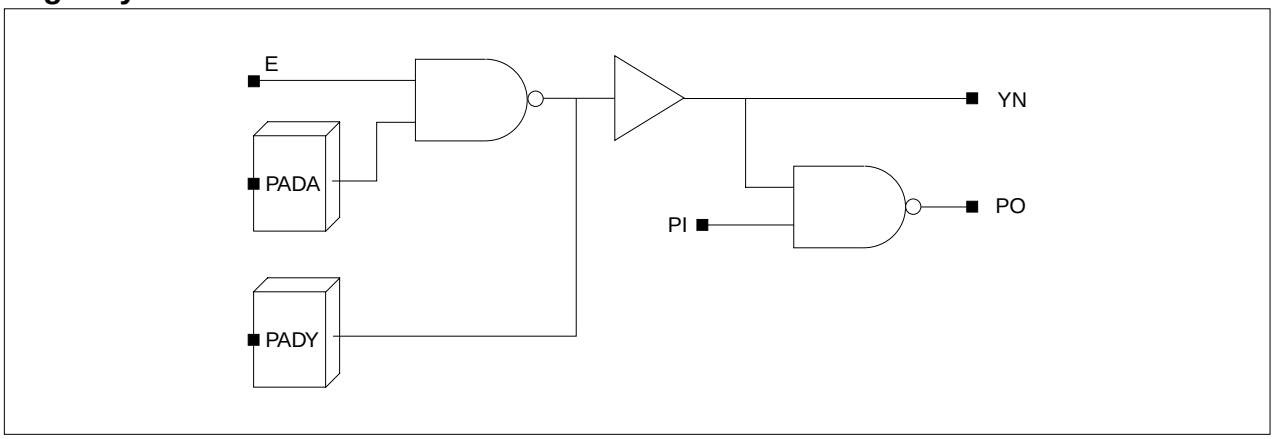
*Group1 : CL < 75, *Group2 : 75 ≤ CL ≤ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.80ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADY to YN	tR	0.282	0.242 + 0.020*SL	0.241 + 0.020*SL	0.205 + 0.021*SL
	tF	0.282	0.246 + 0.018*SL	0.242 + 0.019*SL	0.197 + 0.020*SL
	tPLH	17.493	17.467 + 0.013*SL	17.479 + 0.010*SL	17.513 + 0.009*SL
	tPHL	17.407	17.379 + 0.014*SL	17.390 + 0.011*SL	17.420 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 45, *Group3 : 45 < SL

Logic Symbol



Truth Table

PADA	E	PADY	YN	PI	PO
0	0	1	1	0	1
0	0	1	1	1	0
0	1	1	1	0	1
0	1	1	1	1	0
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)			I/O Sizes		
PSOSCM1	*PSOSCM2*	*PSOSCM3*	*PSOSCM1*	*PSOSCM2*	*PSOSCM3*
E	E	E			
3.86	3.86	3.86	2 I/O Slots	2 I/O Slots	2 I/O Slots

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.80ns, CL: Capacitive Load[pf])

PSOSCM1

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	tR	12.665	0.385 + 0.000*CL	0.385 + 0.000*CL	0.391 + 0.003*CL
	tF	17.016	0.514 + 0.000*CL	0.517 + 0.000*CL	0.517 + 0.004*CL
	tPLH	5.899	0.629 + 0.000*CL	0.629 + 0.000*CL	0.623 + 0.001*CL
	tPHL	8.258	0.640 + 0.000*CL	0.637 + 0.000*CL	0.631 + 0.002*CL
E to PADY	tR	12.658	0.378 + 0.000*CL	0.378 + 0.000*CL	0.384 + 0.003*CL
	tF	17.016	0.514 + 0.000*CL	0.517 + 0.000*CL	0.517 + 0.004*CL
	tPLH	5.858	0.584 + 0.000*CL	0.590 + 0.000*CL	0.584 + 0.001*CL
	tPHL	8.169	0.547 + 0.000*CL	0.542 + 0.000*CL	0.545 + 0.002*CL

*Group1 : CL < 75, *Group2 : 75 ≤ CL ≤ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.80ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADY to YN	tR	1.835	1.709 + 0.063*SL	1.819 + 0.035*SL	2.251 + 0.026*SL
	tF	1.075	0.985 + 0.045*SL	1.031 + 0.034*SL	1.265 + 0.028*SL
	tPLH	8.382	8.274 + 0.054*SL	8.361 + 0.032*SL	8.889 + 0.021*SL
	tPHL	3.953	3.873 + 0.040*SL	3.928 + 0.026*SL	4.263 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 45, *Group3 : 45 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.80ns, CL: Capacitive Load[pf])

PSOSCM2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	tR	3.141	0.329 + 0.000*CL	0.264 + 0.000*CL	0.245 + 0.001*CL
	tF	4.202	0.284 + 0.000*CL	0.236 + 0.000*CL	0.213 + 0.001*CL
	tPLH	1.986	0.744 + 0.000*CL	0.739 + 0.000*CL	0.737 + 0.000*CL
	tPHL	2.544	0.716 + 0.000*CL	0.705 + 0.000*CL	0.708 + 0.000*CL
E to PADY	tR	3.022	0.118 + 0.000*CL	0.109 + 0.000*CL	0.115 + 0.001*CL
	tF	4.164	0.202 + 0.000*CL	0.182 + 0.000*CL	0.180 + 0.001*CL
	tPLH	1.981	0.733 + 0.000*CL	0.730 + 0.000*CL	0.730 + 0.000*CL
	tPHL	2.460	0.618 + 0.000*CL	0.621 + 0.000*CL	0.615 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≤ CL ≤ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.80ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADY to YN	tR	0.501	0.487 + 0.007*SL	0.492 + 0.006*SL	0.543 + 0.005*SL
	tF	0.307	0.291 + 0.008*SL	0.298 + 0.007*SL	0.311 + 0.006*SL
	tPLH	1.574	1.556 + 0.009*SL	1.569 + 0.006*SL	1.659 + 0.004*SL
	tPHL	1.086	1.072 + 0.007*SL	1.080 + 0.005*SL	1.127 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 45, *Group3 : 45 < SL

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.80ns, CL: Capacitive Load[pf])

PSOSCM3

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	tR	1.665	0.551 + 0.000*CL	0.527 + 0.000*CL	0.510 + 0.000*CL
	tF	2.086	0.512 + 0.000*CL	0.480 + 0.000*CL	0.461 + 0.000*CL
	tPLH	1.577	1.003 + 0.000*CL	1.031 + 0.000*CL	1.051 + 0.000*CL
	tPHL	1.839	1.039 + 0.000*CL	1.062 + 0.000*CL	1.064 + 0.000*CL
E to PADY	tR	1.421	0.271 + 0.000*CL	0.241 + 0.000*CL	0.235 + 0.000*CL
	tF	2.030	0.422 + 0.000*CL	0.412 + 0.000*CL	0.403 + 0.000*CL
	tPLH	1.607	1.083 + 0.000*CL	1.081 + 0.000*CL	1.096 + 0.000*CL
	tPHL	1.795	0.985 + 0.000*CL	1.008 + 0.000*CL	1.022 + 0.000*CL

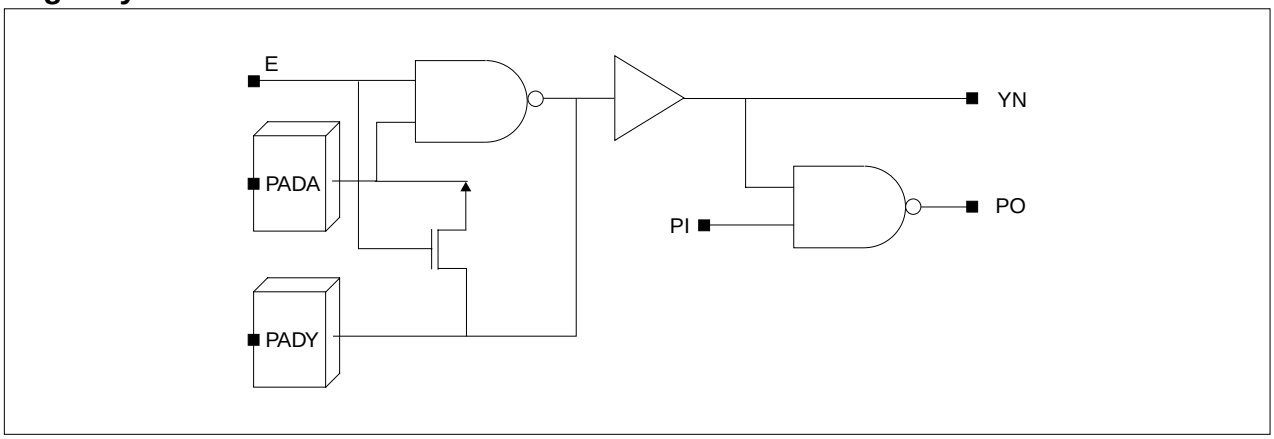
*Group1 : CL < 75, *Group2 : 75 ≤ CL ≤ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.80ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADY to YN	tR	0.278	0.274 + 0.002*SL	0.273 + 0.003*SL	0.288 + 0.002*SL
	tF	0.213	0.205 + 0.004*SL	0.208 + 0.003*SL	0.216 + 0.003*SL
	tPLH	0.697	0.691 + 0.003*SL	0.694 + 0.002*SL	0.725 + 0.002*SL
	tPHL	0.647	0.641 + 0.003*SL	0.643 + 0.002*SL	0.665 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 45, *Group3 : 45 < SL

Logic Symbol



Truth Table

PADA	E	PADY	YN	PI	PO
0	0	1	1	0	1
0	0	1	1	1	0
0	1	1	1	0	1
0	1	1	1	1	0
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)			I/O Sizes		
PSOSCM16	*PSOSCM26*	*PSOSCM36*	*PSOSCM16*	*PSOSCM26*	*PSOSCM36*
E	E	E			
3.86	3.86	3.86	2 I/O Slots	2 I/O Slots	2 I/O Slots

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.80ns, CL: Capacitive Load[pf])

PSOSCM16

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	tR	12.679	0.395 + 0.000*CL	0.386 + 0.000*CL	0.403 + 0.003*CL
	tF	17.047	0.521 + 0.000*CL	0.522 + 0.000*CL	0.520 + 0.004*CL
	tPLH	5.904	0.636 + 0.000*CL	0.633 + 0.000*CL	0.639 + 0.001*CL
	tPHL	8.277	0.655 + 0.000*CL	0.650 + 0.000*CL	0.653 + 0.002*CL
E to PADY	tR	12.658	0.378 + 0.000*CL	0.378 + 0.000*CL	0.384 + 0.003*CL
	tF	17.047	0.521 + 0.000*CL	0.522 + 0.000*CL	0.520 + 0.004*CL
	tPLH	5.890	0.618 + 0.000*CL	0.621 + 0.000*CL	0.621 + 0.001*CL
	tPHL	8.220	0.590 + 0.000*CL	0.590 + 0.000*CL	0.590 + 0.002*CL

*Group1 : CL < 75, *Group2 : 75 ≤ CL ≤ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.80ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADY to YN	tR	1.835	1.709 + 0.063*SL	1.819 + 0.035*SL	2.251 + 0.026*SL
	tF	1.075	0.985 + 0.045*SL	1.031 + 0.034*SL	1.265 + 0.028*SL
	tPLH	8.383	8.275 + 0.054*SL	8.362 + 0.032*SL	8.890 + 0.021*SL
	tPHL	3.955	3.873 + 0.041*SL	3.930 + 0.026*SL	4.265 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 45, *Group3 : 45 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.80ns, CL: Capacitive Load[pf])

PSOSCM26

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	tR	3.141	0.325 + 0.000*CL	0.266 + 0.000*CL	0.241 + 0.001*CL
	tF	4.211	0.293 + 0.000*CL	0.238 + 0.000*CL	0.223 + 0.001*CL
	tPLH	1.992	0.748 + 0.000*CL	0.746 + 0.000*CL	0.749 + 0.000*CL
	tPHL	2.555	0.725 + 0.000*CL	0.718 + 0.000*CL	0.720 + 0.000*CL
E to PADY	tR	3.022	0.118 + 0.000*CL	0.109 + 0.000*CL	0.115 + 0.001*CL
	tF	4.172	0.208 + 0.000*CL	0.199 + 0.000*CL	0.182 + 0.001*CL
	tPLH	2.015	0.767 + 0.000*CL	0.764 + 0.000*CL	0.764 + 0.000*CL
	tPHL	2.502	0.660 + 0.000*CL	0.656 + 0.000*CL	0.658 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≤ CL ≤ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.80ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADY to YN	tR	0.501	0.487 + 0.007*SL	0.492 + 0.006*SL	0.543 + 0.005*SL
	tF	0.307	0.291 + 0.008*SL	0.298 + 0.007*SL	0.311 + 0.006*SL
	tPLH	1.575	1.557 + 0.009*SL	1.570 + 0.006*SL	1.660 + 0.004*SL
	tPHL	1.087	1.073 + 0.007*SL	1.081 + 0.005*SL	1.128 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 45, *Group3 : 45 < SL

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.80ns, CL: Capacitive Load[pf])

PSOSCM36

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	tR	1.664	0.548 + 0.000*CL	0.527 + 0.000*CL	0.504 + 0.000*CL
	tF	2.094	0.520 + 0.000*CL	0.488 + 0.000*CL	0.469 + 0.000*CL
	tPLH	1.584	1.010 + 0.000*CL	1.039 + 0.000*CL	1.058 + 0.000*CL
	tPHL	1.846	1.044 + 0.000*CL	1.062 + 0.000*CL	1.073 + 0.000*CL
E to PADY	tR	1.421	0.269 + 0.000*CL	0.249 + 0.000*CL	0.235 + 0.000*CL
	tF	2.037	0.429 + 0.000*CL	0.419 + 0.000*CL	0.404 + 0.000*CL
	tPLH	1.642	1.118 + 0.000*CL	1.131 + 0.000*CL	1.123 + 0.000*CL
	tPHL	1.833	1.021 + 0.000*CL	1.047 + 0.000*CL	1.055 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≤ CL ≤ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.80ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADY to YN	tR	0.278	0.274 + 0.002*SL	0.273 + 0.003*SL	0.286 + 0.002*SL
	tF	0.213	0.205 + 0.004*SL	0.208 + 0.003*SL	0.216 + 0.003*SL
	tPLH	0.698	0.692 + 0.003*SL	0.695 + 0.002*SL	0.724 + 0.002*SL
	tPHL	0.648	0.642 + 0.003*SL	0.644 + 0.002*SL	0.666 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 45, *Group3 : 45 < SL

Overview

PCI buffers are designed for PCI local bus application which is designed for high-performance 32-bit or 64-bit bus architecture.

SEC supports PCI input, output and bi-directional buffers for 3.3V and 5V signaling environment.

Features

— Input, output, bi-directional PCI buffers.
— PCI local bus specification rev2.1 compliant.
— Operation at up to 33MHz.
— Electrically compliant interface in 3.3V and 5V bus environments.

Description

The pbpci, pipci and popci PCI buffers can only be used for 3.3V environment. To support 5V signaling environment, ptbpci3/ptbpci5, ptipci3/ptipci5 and ptopci3/ptopci5 PCI buffers should be used.

These 5V tolerant PCI buffers require 5V power for 5V environment and 3.3V power for 3.3V environment for the bulk of PMOS driver. 5V environment support is enabled when EN5V is set to low.

Although tolerant PCI buffers support 5V environment, they do not drive 5V.

NOTE: If you want to use PCI buffers, please contact SEC.

Only 3.3V Signaling PCI I/Os (note1)

Cell Name	Description	Operating Frequency	Operating Voltage
PBPCI	Bi-direction	Up to 33MHz at 3.3V signaling	3.3V
PIPCI	Receiver	Up to 33MHz at 3.3V signaling	
POPCI	Driver	Up to 33MHz at 3.3V signaling	

NOTE1: PCI I/Os in group A use normal power cells

3.3V or 5V Signaling PCI I/Os (note2, 3, 4)

Cell Name	Description	Operating Frequency	VIO Voltage	Operating Voltage
PTBPCI3	Bi-direction	Up to 33MHz at 3.3V signaling	3.3V	3.3V
PTIPCI3	Receiver	Up to 33MHz at 3.3V signaling		
PTOPCI3	Driver	Up to 33MHz at 3.3V signaling		
PTBPCI5	Bi-direction	Up to 33MHz at 5V signaling	5V	3.3V
PTIPCI5	Receiver	Up to 33MHz at 5V signaling		
PTOPCI5	Driver	Up to 33MHz at 5V signaling		

NOTE2: 3.3V signaling conditions: EN5V=high, VIO=3.3V, 5V tolerant is not supported.
5V signaling conditions: EN5V=low, VIO=5V, and 5V tolerant is supported.

NOTE3: In 3.3V signaling, the voltage level of VIO is 3.3V, which is provided through the VDD5O_S power cell.
In 5V signaling, the voltage level of VIO is 5V, which is provided through the VDD5O_S power cell.

NOTE4: For group B, following power cells should be used.

Cell Name	Description
VDD3I_S	2.5V Power cell for internal core
VDD3OP_S	3.3V Power cell for PCI I/O
VDD5O_S	VIO(3.3V or 5V) Power cell for PCI I/Os (note3)
VSSI_S	Gnd Power cell for internal core
VSSOP_S	Gnd Power cell for PCI I/O

Option (note5)

Cell Name	Description
VDET_90PCI	3.3V or 5V voltage detector

NOTE5: The Voltage detector can be used with group B PCI I/O. Voltage detector circuit will automatically set the EN5V pin either high or low according to VIO voltage level.

Electrical Characteristics

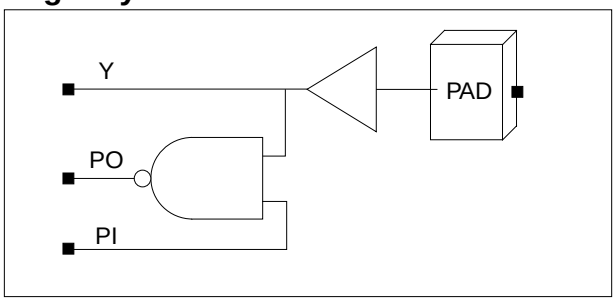
DC Characteristics

Symbol	Parameter	3.3V Signaling			5V Signaling			Unit
		Condition	Min	Max	Condition	Min	Max	
V_{CC}	Supply voltage		3.0	3.6		3.0	3.6	V
VIO	VDD5O voltage		V_{CC}			4.75	5.25	V
V_{IH}	Input high voltage		$0.47V_{CC}$	V_{CC} + 0.5		1.9	VIO+0.5	V
I_{IL}	Input low voltage		–0.5	$0.33V_{CC}$		–0.5	0.9	V
I_I	Input leakage current	$0 < V_{IN} < V_{CC}$	–10	10	$0 < V_{IN} < VIO$	–7.0	70	µA
V_{OH}	Output high voltage	I_{OUT} = –500uA	0.9Vcc		I_{OUT} = –2mA	2.4		V
V_{OL}	Output low voltage	I_{OUT} = 1500uA		0.1Vcc	I_{OUT} = 6mA		0.55	V

AC Characteristics

Symbol	Parameter	3.3V Signaling			5V Signaling			Unit
		Condition	Min	Max	Condition	Min	Max	
I_{OH} (AC)	Switching current high	$V_{OUT} = 0.3V_{CC}$	$–12V_{CC}$		V_{OUT} = 1.4V	–44		mA
		$V_{OUT} = 0.7V_{CC}$		$-32V_{CC}$	V_{OUT} = 2.4V	–2.33		
		$V_{OUT} = 0.9V_{CC}$	$–1.71V_{CC}$		V_{OUT} = 3.0V		–142	
I_{OL} (AC)	Switching current low	$V_{OUT} = 0.6V_{CC}$	$16V_{CC}$		V_{OUT} = 2.2V	95		mA
		$V_{OUT} = 0.1V_{CC}$	$2.67V_{CC}$		V_{OUT} = 0.55V	23.9		
		$V_{OUT} = 0.18V_{CC}$		$38V_{CC}$	V_{OUT} = 0.71V		206	
I_{CL}	Low clamp current	$–3 < V_{IN} \le –1$	$–25+(V_{IN}+1)/0.015$		$–5 < V_{IN} \le –1$	$–25+(V_{IN}+1)/0.015$		mA
I_{CH}	Low clamp current	$V_{CC}+1 \le V_{IN} < V_{CC}+4$	$25+(V_{IN}-V_{CC}-1)/0.015$					mA
T_R	Output rise time	$0.2V_{CC}$ to $0.6V_{CC}$	1.0	4.0	0.4V to 2.4V	1.0	5.0	V/ns
T_F	Output fall time	$0.6V_{CC}$ to $0.2V_{CC}$	1.0	4.0	2.4V to 0.4V	1.0	5.0	V/ns

Logic Symbol



Truth Table

Input Truth Table			
PAD	**PI**	**Y**	**PO**
1	1	1	0
0	x	0	1
1	0	1	1

Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.80 ns, SL: Standard Load)

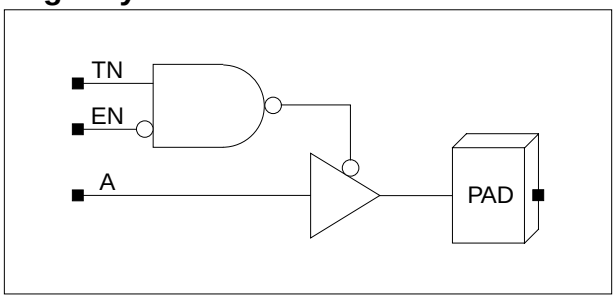
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	**Group2***	**Group3***
PAD to Y	t_R	0.202	0.134 + 0.034*SL	0.144 + 0.026*SL	0.153 + 0.026*SL
	t_F	0.157	0.117 + 0.020*SL	0.117 + 0.021*SL	0.144 + 0.019*SL
	t_{PLH}	0.209	0.177 + 0.016*SL	0.181 + 0.013*SL	0.197 + 0.012*SL
	t_{PHL}	0.304	0.276 + 0.014*SL	0.278 + 0.013*SL	0.302 + 0.011*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 17, *Group3 : 17 < SL

POPCI

PCI Output Buffers

Logic Symbol



Truth Table

Output Truth Table			
A	**EN**	**TN**	**PAD**
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

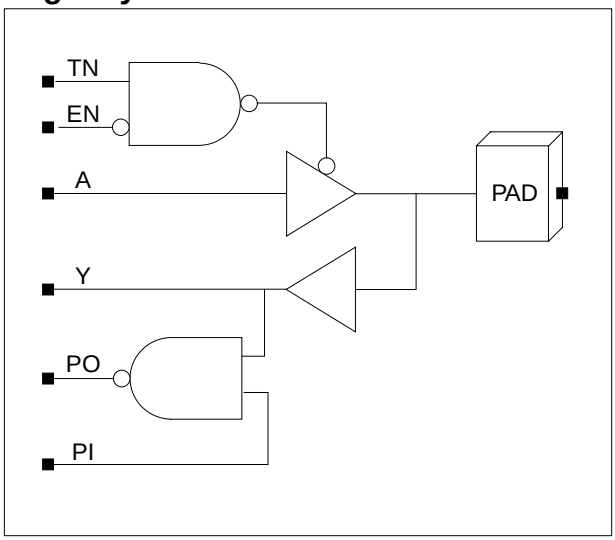
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.80ns, CL Capacitive Load(pF))

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.663	0.515 + 0.063*CL	0.407 + 0.064*CL	0.350 + 0.065*CL
	t_F	2.927	0.779 + 0.043*CL	0.761 + 0.043*CL	0.733 + 0.044*CL
	t_{PLH}	1.904	0.702 + 0.024*CL	0.705 + 0.024*CL	0.716 + 0.024*CL
	t_{PHL}	2.909	1.557 + 0.027*CL	1.628 + 0.026*CL	1.659 + 0.026*CL
TN to PAD	t_R	3.633	0.461 + 0.063*CL	0.351 + 0.065*CL	0.315 + 0.065*CL
	t_F	2.928	0.784 + 0.043*CL	0.752 + 0.043*CL	0.744 + 0.043*CL
	t_{PLH}	2.104	0.900 + 0.024*CL	0.906 + 0.024*CL	0.912 + 0.024*CL
	t_{PHL}	2.960	1.606 + 0.027*CL	1.680 + 0.026*CL	1.716 + 0.026*CL
	t_{PLZ}	0.922	0.922 + 0.000*CL	0.922 + 0.000*CL	0.922 + 0.000*CL
	t_{PHZ}	0.864	0.864 + 0.000*CL	0.864 + 0.000*CL	0.864 + 0.000*CL
EN to PAD	t_R	3.634	0.466 + 0.063*CL	0.350 + 0.065*CL	0.308 + 0.065*CL
	t_F	2.923	0.775 + 0.043*CL	0.749 + 0.043*CL	0.730 + 0.044*CL
	t_{PLH}	2.280	1.076 + 0.024*CL	1.075 + 0.024*CL	1.089 + 0.024*CL
	t_{PHL}	3.121	1.767 + 0.027*CL	1.833 + 0.026*CL	1.878 + 0.026*CL
	t_{PLZ}	0.657	0.657 + 0.000*CL	0.657 + 0.000*CL	0.657 + 0.000*CL
	t_{PHZ}	0.602	0.602 + 0.000*CL	0.587 + 0.000*CL	0.604 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Logic Symbol



Truth Table

Input Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

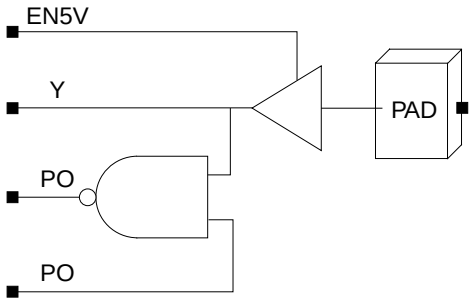
Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

(Under Development) PTIPCI

5V-tolerant PCI Input Buffers

Logic Symbol



NOTE: EN5V = High in 3.3V signaling
EN5V = Low in 5V signaling

Truth Table

Input Truth Table			
PAD	**PI**	**Y**	**PO**
1	1	1	0
0	x	0	1
1	0	1	1

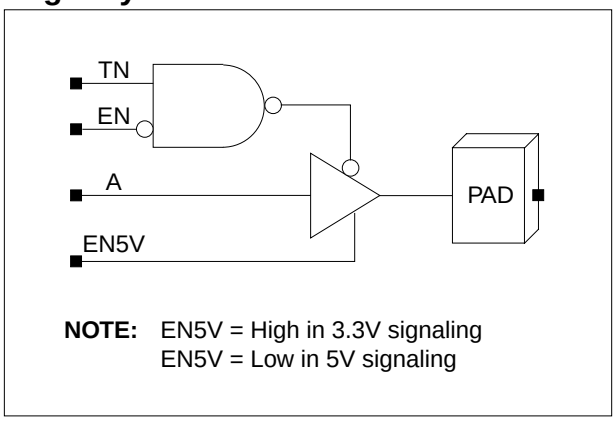
Switching Characteristics

(Typical process, 25 °C, 3.3 V, t_R/t_F = 0.80 ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	**Group2***	**Group3***
PAD to Y	t_R	0.182	0.160 + 0.011*SL	0.140 + 0.026*SL	0.121 + 0.027*SL
	t_F	0.199	0.165 + 0.017*SL	0.164 + 0.018*SL	0.142 + 0.020*SL
	t_{PLH}	0.314	0.286 + 0.014*SL	0.288 + 0.013*SL	0.302 + 0.012*SL
	t_{PHL}	0.449	0.413 + 0.018*SL	0.419 + 0.014*SL	0.460 + 0.011*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



NOTE: EN5V = High in 3.3V signaling
EN5V = Low in 5V signaling

Truth Table

Output Truth Table			
A	**EN**	**TN**	**PAD**
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	HI-Z

Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.80 ns, CL Capacitive Load(pF))

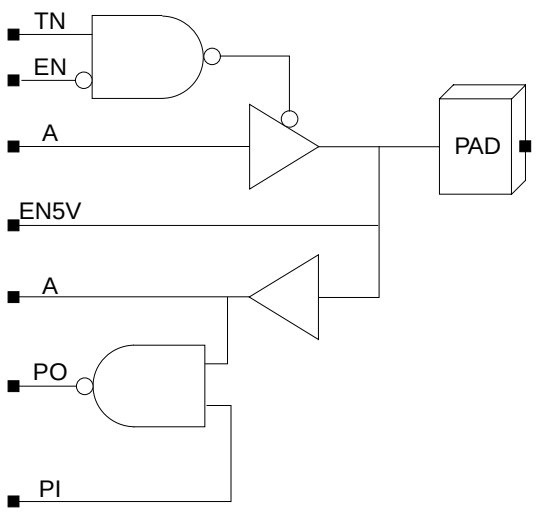
Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.872	0.532 + 0.067*CL	0.472 + 0.068*CL	0.461 + 0.068*CL
	t_F	3.005	0.671 + 0.047*CL	0.669 + 0.047*CL	0.672 + 0.047*CL
	t_{PLH}	2.538	1.312 + 0.025*CL	1.328 + 0.024*CL	1.343 + 0.024*CL
	t_{PHL}	3.309	1.977 + 0.027*CL	2.032 + 0.026*CL	2.075 + 0.025*CL
TN to PAD	t_R	3.872	0.530 + 0.067*CL	0.488 + 0.067*CL	0.454 + 0.068*CL
	t_F	3.011	0.679 + 0.047*CL	0.682 + 0.047*CL	0.682 + 0.047*CL
	t_{PLH}	2.620	1.392 + 0.025*CL	1.419 + 0.024*CL	1.425 + 0.024*CL
	t_{PHL}	3.214	1.882 + 0.027*CL	1.937 + 0.026*CL	1.980 + 0.025*CL
	t_{PLZ}	1.111	1.111 + 0.000*CL	1.111 + 0.000*CL	1.111 + 0.000*CL
	t_{PHZ}	0.898	0.898 + 0.000*CL	0.898 + 0.000*CL	0.898 + 0.000*CL
EN to PAD	t_R	3.872	0.530 + 0.067*CL	0.488 + 0.067*CL	0.454 + 0.068*CL
	t_F	3.011	0.681 + 0.047*CL	0.674 + 0.047*CL	0.682 + 0.047*CL
	t_{PLH}	2.816	1.588 + 0.025*CL	1.615 + 0.024*CL	1.621 + 0.024*CL
	t_{PHL}	3.405	2.071 + 0.027*CL	2.174 + 0.025*CL	2.166 + 0.025*CL
	t_{PLZ}	0.928	0.928 + 0.000*CL	0.928 + 0.000*CL	0.928 + 0.000*CL
	t_{PHZ}	0.693	0.693 + 0.000*CL	0.693 + 0.000*CL	0.693 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

(Under Development) PTBPCI

5V-Tolerant PCI Bidirectional Buffer

Logic Symbol



NOTE: EN5V = High in 3.3V signaling
EN5V = Low in 5V signaling

Truth Table

Input Truth Table

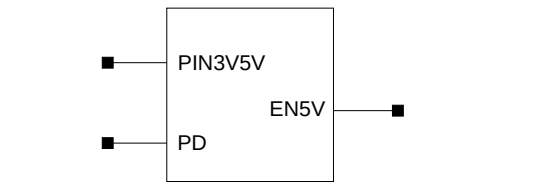
PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

Option:

Logic Symbol



Truth Table

PD	PIN3V5V	EN5V
0	3.3V	1
0	5V	0
1	x	0

Cell Data

Cell Name	Detecting Voltage
VDET_90PCI	3.3V, 5V

NOTES:

1. PIN3V5V is a special power supply PIN for switching the universal PCI I/O buffer between 3.3V and 5V signaling environment. THis VDET_90PCI is used to detect the voltage state of the PIN3V5V. From the rising edge of PD, the output EN5V will be set to “0” until the falling edge comes. Since the falling edge of PD, the voltage state of PIN3V5V will be detected as shown in the above truth table.
2. The power(VDD) and ground(VSS) of this VDET_90PCI, must be connected to the “VDD & VSS of the I/O PART”.

Overview

USB I/O buffer consists of a differential input receiver, a differential output driver, two single-ended receivers and two pads. The differential input receiver has 0.8V ~ 2.5V common mode input voltage range and both of the two single-ended receivers have 0.8V and 2.0V as their low and high input threshold voltages, V_{IL}, V_{IH}.

For low power consumption in a stand-by mode, the stand-by (STBYS, STBYD) pins of two kinds of receivers should be in high state. The differential output drivers has a Low/Full speed control pin (LSOEB) to select the operation speed and has ENL to achieve bi-directional half duplex operation.

Electrical Specifications

DC Electrical Characteristics

Parameter	Symbol	Condition (Notes 1, 2)	Min	Max	Unit
Supply Current					
High Power Function	I_{CCHPF}			500	mA
Low Power Function	I_{CCLPF}			100	
Unconfig. Function / Hub	I_{CCINIT}			100	
Suspended Device	I_{CCS}			500	µA
Leakage Current					
Hi-Z State Data Line Leakage	I_{LO}	0V < VIN < 3.3V	–10	10	µA
Input Levels					
Differential Input Sensitivity	V_{DI}		0.2		V
Differential Common Mode Range	V_{CM}	Includes V_{DI} range	0.8	2.5	
Single Ended Receiver Threshold	V_{SE}		0.8	2.0	
Output Levels					
Static Output Low	V_{OL}	RL of 1.5KΩ to 3.6V		0.3	V
Static Output High	V_{OH}	RL of 15KΩ to GND	2.8	3.6	

Full Speed Output Buffer Electrical Characteristics

Parameter	Symbol	Condition (Notes 1, 2, 3)	Min	Max	Unit
Driver Characteristics					
Transition Time		Notes 5 and Figure 1			ns
Rise Time	T_R	CL = 50pF	4.0	20.0	
Fall Time	T_F	CL = 50pF	4.0	20.0	
Rise/Fall Time Matching	T_{RFM}	(T_R/T_F)	90	110	%
Output Signal Crossover Voltage	V_{CRS}		1.3	2.0	V

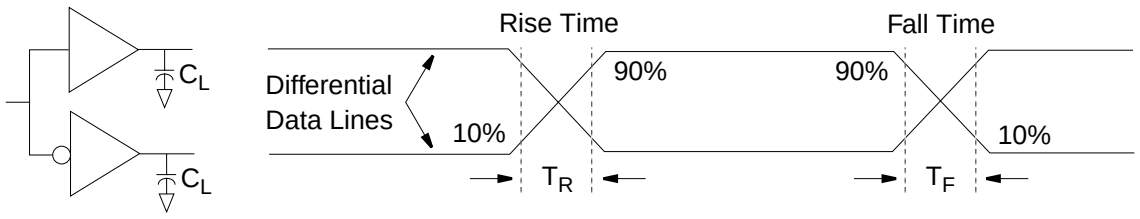
Low Speed Output Buffer Electrical Characteristics

Parameter	Symbol	Condition (Notes 1, 2, 4)	Min	Max	Unit
Driver Characteristics					
Transition Time		Notes 5 and Figure 1			ns
Rise Time	T_R	CL = 50pF	75		
		CL = 350pF		300	
Fall Time	T_F	CL = 50pF	75		
		CL = 350pF		300	
Rise/Fall Time Matching	T_{RFM}	(T_R/T_F)	80	120	%
Output Signal Crossover Voltage	V_{CRS}		1.3	2.0	V

NOTES:

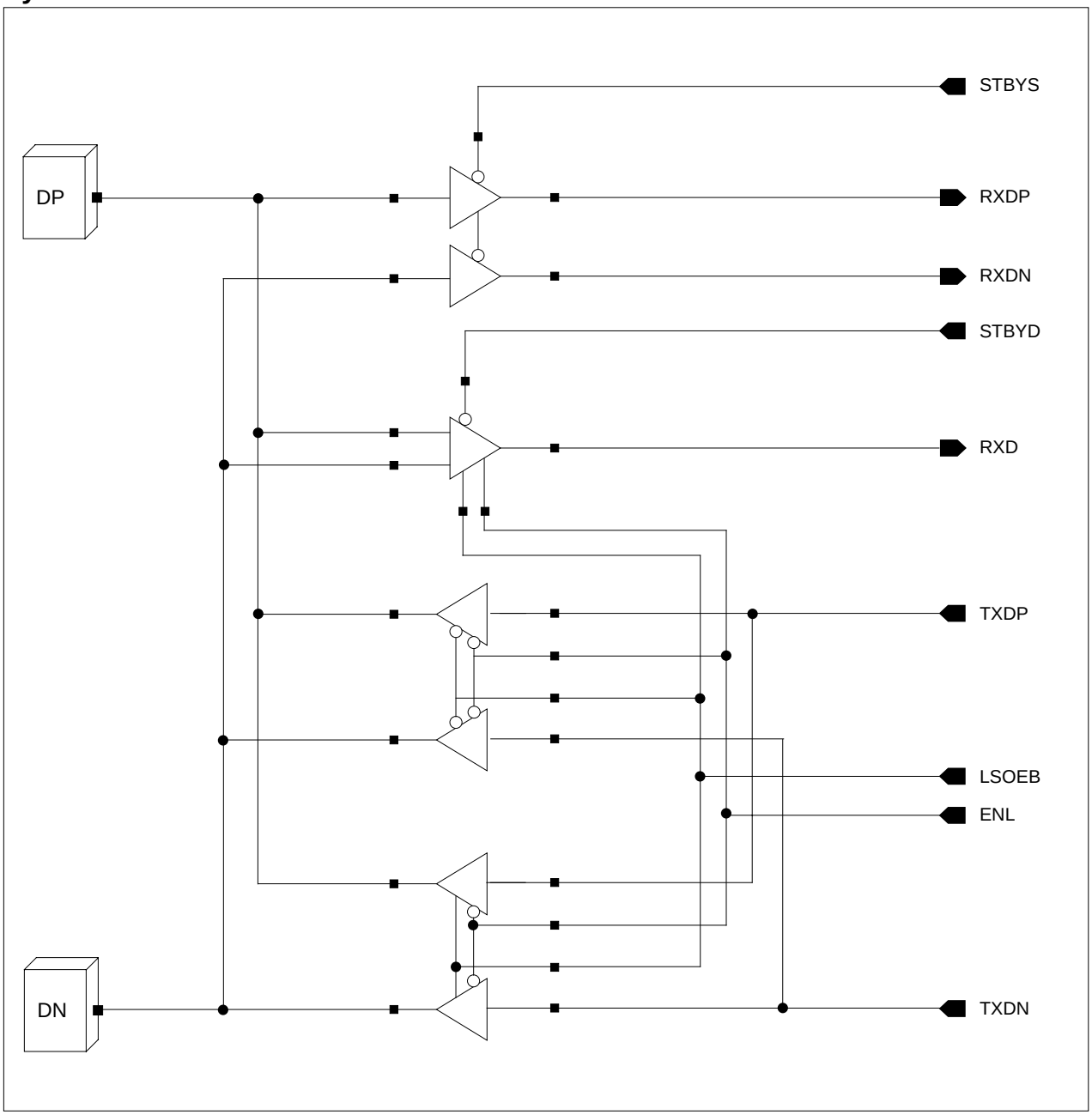
1. All voltages are measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load (CL) to ground of 50pF, unless otherwise specified.
3. Full speed timings have a 1.5KΩ pull-up to 2.8V.
4. Low speed timings have a 1.5KΩ pull-up to 2.8V.
5. Measured from 10% to 90% of the data signal.

Figure 1: Data Signal Rise and Fall Time



Full Speed: 4 to 20ns at C_L = 50pF Low Speed: 75ns at C_L = 50pF, 300ns at C_L = 350pF

Symbol



Pin Connection

Input	Output	Bi-Direction
STBYS	RXDP	DP
STBYD	RXDN	DN
TXDP	RXD	
TXDN		
ENL		
LSOEB		

Cell Structure

PBUSB = PISER + PICDR + POTLS + POTFS

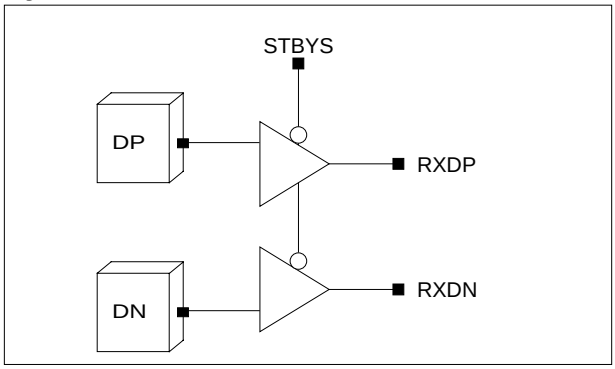
PBUSB1 = PISER + PICDR + POTLS + POTFS

There only exists PBUSB not PBUSB1 in the physical DB. The division of cell name (PBUSB/PBUSB1) is caused to notify their different working-mode. PBUSB selects POTLS (LSOEB=0) to work on Low Speed Mode. PBUSB1 selects POTFS (LSOEB=1) to work on Full Speed Mode.

PISER

Single-Ended Receiver

Symbol



Pin Connection

Input	Output
DP	RXDP
DN	RXDN
STBYS	

Truth Table

DP	DN	STBYS	RXDP	RXDN
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	0	1	1
x	x	1	0	0

PISER Switching Characteristics (Typical process, 25°C, 3.3 V, t_R/t_F = 0.80ns, SL: Standard Load)

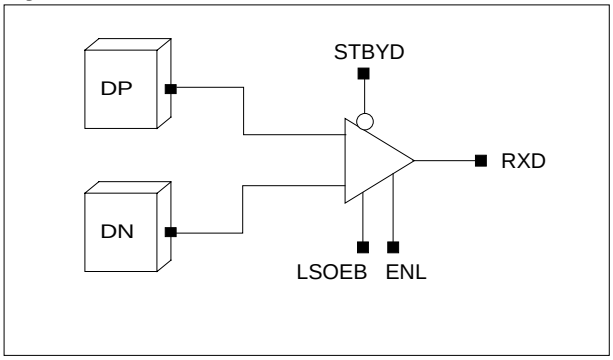
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
DP to RXDP	t_R	0.170	0.164 + 0.003*SL	0.134 + 0.026*SL	0.133 + 0.026*SL
	t_F	0.225	0.167 + 0.029*SL	0.177 + 0.022*SL	0.218 + 0.019*SL
	t_{PLH}	0.633	0.623 + 0.005*SL	0.611 + 0.014*SL	0.647 + 0.012*SL
	t_{PHL}	0.978	0.922 + 0.028*SL	0.937 + 0.017*SL	0.995 + 0.013*SL
STBYS to RXDP	t_R	0.154	0.080 + 0.037*SL	0.094 + 0.026*SL	0.084 + 0.027*SL
	t_F	0.112	0.052 + 0.030*SL	0.065 + 0.020*SL	0.074 + 0.020*SL
	t_{PLH}	0.453	0.413 + 0.020*SL	0.423 + 0.013*SL	0.440 + 0.012*SL
	t_{PHL}	0.199	0.175 + 0.012*SL	0.175 + 0.012*SL	0.184 + 0.011*SL
DN to RXDN	t_R	0.170	0.164 + 0.003*SL	0.134 + 0.026*SL	0.133 + 0.026*SL
	t_F	0.225	0.167 + 0.029*SL	0.177 + 0.022*SL	0.218 + 0.019*SL
	t_{PLH}	0.633	0.623 + 0.005*SL	0.611 + 0.014*SL	0.647 + 0.012*SL
	t_{PHL}	0.978	0.922 + 0.028*SL	0.937 + 0.017*SL	0.995 + 0.013*SL
STBYS to RXDN	t_R	0.154	0.080 + 0.037*SL	0.094 + 0.026*SL	0.084 + 0.027*SL
	t_F	0.112	0.052 + 0.030*SL	0.065 + 0.020*SL	0.074 + 0.020*SL
	t_{PLH}	0.453	0.413 + 0.020*SL	0.423 + 0.013*SL	0.440 + 0.012*SL
	t_{PHL}	0.199	0.175 + 0.012*SL	0.175 + 0.012*SL	0.184 + 0.011*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 17, *Group3 : 17 < SL

PICDR

Differential Receiver

Symbol



Pin Connection

Input	Output
DP DN STBYD LSOEB ENL	RXD

Truth Table

DP	DN	STBYD	LSOEB	ENL	RXD
0	0	0	x	1	0
0	1	0	x	1	0
1	0	0	x	1	1
1	1	0	x	1	x
x	x	1	x	1	0
0	0	x	0	0	0
0	1	x	0	0	0
1	0	x	0	0	1
1	1	x	0	0	x
x	x	1	1	0	0
0	0	0	1	0	0
0	1	0	1	0	0
1	0	0	1	0	1
1	1	0	1	0	x

PICDR Switching Characteristics (Typical process, 25°C, 3.3 V, t_R/t_F = 0.80ns, SL: Standard Load)

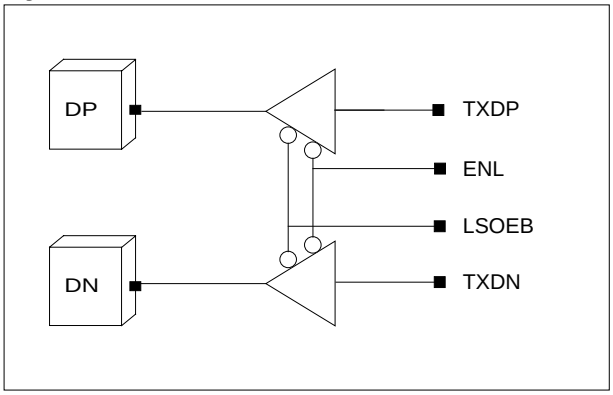
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
DP to RXD	t_R	0.125	0.075 + 0.025*SL	0.073 + 0.026*SL	0.061 + 0.027*SL
	t_F	0.100	0.064 + 0.018*SL	0.062 + 0.020*SL	0.055 + 0.020*SL
	t_{PLH}	0.398	0.362 + 0.018*SL	0.370 + 0.012*SL	0.370 + 0.012*SL
	t_{PHL}	0.341	0.317 + 0.012*SL	0.318 + 0.012*SL	0.325 + 0.011*SL
DN to RXD	t_R	0.125	0.075 + 0.025*SL	0.073 + 0.026*SL	0.061 + 0.027*SL
	t_F	0.100	0.064 + 0.018*SL	0.062 + 0.020*SL	0.055 + 0.020*SL
	t_{PLH}	0.398	0.362 + 0.018*SL	0.370 + 0.012*SL	0.370 + 0.012*SL
	t_{PHL}	0.341	0.317 + 0.012*SL	0.318 + 0.012*SL	0.325 + 0.011*SL
STBYD to RXD	t_R	0.137	0.091 + 0.023*SL	0.088 + 0.026*SL	0.072 + 0.027*SL
	t_F	0.128	0.070 + 0.029*SL	0.085 + 0.018*SL	0.047 + 0.021*SL
	t_{PLH}	0.839	0.811 + 0.014*SL	0.814 + 0.012*SL	0.815 + 0.012*SL
	t_{PHL}	0.649	0.621 + 0.014*SL	0.626 + 0.010*SL	0.614 + 0.011*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 17, *Group3 : 17 < SL

POTLS

Tri-State Output Buffer with Low Speed

Symbol



Pin Connection

Input	Output
TXDP TXDN LSOEB ENL	DP DN

Truth Table

TXDP	TXDN	LSOEB	ENL	DP	DN
0	0	0	0	0	0
0	1	0	0	0	1
1	0	0	0	1	0
1	1	0	0	1	1
x	x	x	1	Hi-z	Hi-z

POTLS Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.80ns, CL: Capacitive Load[pF])

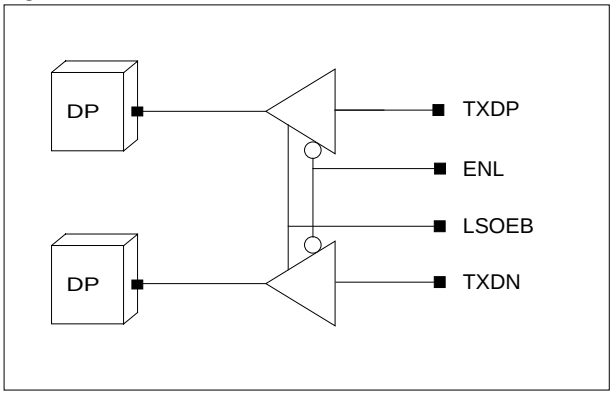
Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TXDP to DP	t_R	149.210	149.210 + 0.000*CL	137.045 + 0.077*CL	136.903 + 0.079*CL
	t_F	138.970	138.630 + 0.007*CL	132.465 + 0.089*CL	133.910 + 0.072*CL
	t_{PLH}	120.950	117.710 + 0.065*CL	114.020 + 0.114*CL	123.823 + 0.000*CL
	t_{PHL}	112.760	106.740 + 0.120*CL	106.545 + 0.123*CL	109.123 + 0.093*CL
ENL to DP	t_R	150.820	150.820 + 0.000*CL	134.785 + 0.095*CL	136.513 + 0.075*CL
	t_F	116.730	83.570 + 0.663*CL	93.485 + 0.531*CL	108.360 + 0.356*CL
	t_{PLH}	116.670	112.930 + 0.075*CL	112.015 + 0.087*CL	122.073 + 0.000*CL
	t_{PHL}	56.341	27.635 + 0.574*CL	37.979 + 0.436*CL	46.479 + 0.336*CL
	t_{PLZ}	0.984	0.984 + 0.000*CL	0.984 + 0.000*CL	0.984 + 0.000*CL
	t_{PHZ}	0.544	0.544 + 0.000*CL	0.544 + 0.000*CL	0.550 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POTFS

Tri-State Output Buffer with Full Speed

Symbol



Pin Connection

Input	Output
TXDP TXDN LSOEB ENL	DP DN

Truth Table

TXDP	TXDN	LSOEB	ENL	DP	DN
0	0	1	0	0	0
0	1	1	0	0	1
1	0	1	0	1	0
1	1	1	0	1	1
x	x	x	1	Hi-Z	Hi-Z

POTFS Switching Characteristics

(Typical process, 25°C, 3.3 V, t_R/t_F = 0.80ns, CL: Capacitive Load[pF])

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TXDP to DP	t_R	5.909	0.457 + 0.109*CL	0.408 + 0.110*CL	0.382 + 0.110*CL
	t_F	6.201	0.111 + 0.122*CL	0.111 + 0.122*CL	0.111 + 0.122*CL
	t_{PLH}	4.049	1.639 + 0.048*CL	1.654 + 0.048*CL	1.660 + 0.048*CL
	t_{PHL}	3.373	0.559 + 0.056*CL	0.557 + 0.056*CL	0.560 + 0.056*CL
ENL to DP	t_R	5.908	0.454 + 0.109*CL	0.415 + 0.110*CL	0.381 + 0.110*CL
	t_F	6.201	0.111 + 0.122*CL	0.118 + 0.122*CL	0.110 + 0.122*CL
	t_{PLH}	4.156	1.746 + 0.048*CL	1.761 + 0.048*CL	1.772 + 0.048*CL
	t_{PHL}	3.443	0.629 + 0.056*CL	0.635 + 0.056*CL	0.629 + 0.056*CL
	t_{PLZ}	0.456	0.456 + 0.000*CL	0.456 + 0.000*CL	0.456 + 0.000*CL
	t_{PHZ}	0.555	0.555 + 0.000*CL	0.555 + 0.000*CL	0.555 + 0.000*CL

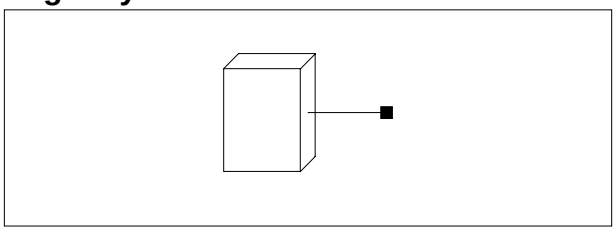
*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POWER PADS

Cell List

Cell Name		Function Description
VDD Power Pads	**VSS Power Pads**	
VDD3I	VSSI	3.3V Internal
VDD3P	VSSP	3.3V Pre-Driver
VDD3O	VSSO	3.3V Output-Driver
VDD3IP	VSSIP	3.3V Internal and Pre-Driver
VDD3OP	VSSOP	3.3V Output-Driver and Pre-Driver
VDD3T	VSST	3.3V Total

Logic Symbol

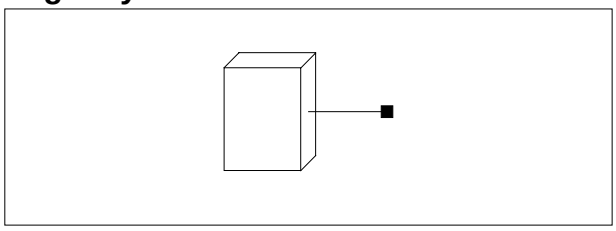


Cell List

Cell Name	Function Description
PIA_BB	Analog Normal Input Pad with Separate Bulk Bias
PIAR10_BB	Analog Normal Input Pad with Resistor 10ohm and Separate Bulk Bias
PIAR50_BB	Analog Normal Input Pad with Resistor 50ohm and Separate Bulk Bias
PIC_BB	Analog LVCMOS Level Input Buffer with Separate Bulk Bias
PICC_BB	Analog LVCMOS Level Input Buffer with Separate Bulk Bias and without Nand-Tree.
POA_BB	Analog Normal Output Pad with Separate Bulk Bias
POAR50_BB	Analog Normal Output Pad with Resistor 50ohm and Separate Bulk Bias
POT2_BB	Analog Tri State Output Pad with Separate Bulk Bias, 2mA Drive
POT4_BB	Analog Tri State Output Pad with Separate Bulk Bias, 4mA Drive
POT12_BB	Analog Tri State Output Pad with Separate Bulk Bias, 12mA Drive

Cell Name		Function Description
VDD Power Pads	**VSS Power Pads**	
VDDA		Analog 3.3V Power with Separate Bulk Bias
	VSSA	Analog Ground with Separate Bulk Bias
	VBBA	Analog Ground for Bulk Bias
VDDD		Digital 3.3V Power with Separate Bulk Bias
	VSSD	Digital Ground with Separate Bulk Bias

Logic Symbol



Compiled Macrocells

5

Contents

OVERVIEW TO COMPILED MEMORY

This section contains the selection of compiled memory available in STD90 cell library. These are complete memories that are customized to satisfy the requirements of the circuit at hand. Depending on the function to be generated, the final memory will be implemented as a stand-alone, densely packed, pitch-matched and customized leafcells. In STD90 cell library, the compiled memory is fully generated by a user-configurable compiler, called Memory Compiler. It allows you to configure a memory through memory-related specification such as word depth, bit per word, column mux type and so on. The compiler allows you to select and customize any of memory to satisfy the specific circuit requirements. When the required specifications have been fully given, you may get any or all of the following items:

— Area-optimized and speed-optimized layout blocks
— Schematic netlist for simulation and verification
— Phantom cell to use in chip-level layout
— Tabular model for timing and power characteristics
— Automatic datasheet for a specific instance

For more detailed information regarding to memory compiler, contact your local representative or headquarters.

COMPILED MEMORY NAMING CONVENTION

The naming convention of compiled memory in this section will be shown as Figure 5-1. The memory name consists of the following convention.

[memory_code]_[appl_code]_[config_code]

Figure 5-1. Compiled Memory Naming Convention

The first string ‘memory_code’ means the name of memory type and the name of the memory type available in STD90 compiled memory is as follows:

- SPSRAM : Single-Port Synchronous SRAM
- SPSRAMBW : Single-Port Synchronous SRAM with Bit-Write
- DPSRAM : Dual-Port Synchronous SRAM
- SPARAM : Single-Port Asynchronous SRAM
- DROM : Synchronous Diffusion-Programmable ROM
- MROM : Synchronous Metal-Programmable ROM

The second string ‘appl_code’ means the specific application code to support the compiled memory and the application code is one of HD (High-Density), LP (Low-Power) and HS (High-Speed). In STD90 compiled memory, the high-density memory is only supported. The last string ‘config_code’ represents the configuration of the memory to be specified. This configuration code is composed of the following convention:

<WORD> x <BPW> m <YMUX>

Here, WORD is the word depth, BPW is bit per word, YMUX is the available column mux type.

For example, SPSRAM_HD_1024x32m16 refers to a High-Density single-port synchronous SRAM with 1024 words, 32 bits and 16 column mux.

CHARACTERISTICS FOR TIMING AND POWER

Compiled memory in this section has been characterized using typical-case at 25 degree and 3.3V supply. The values of worst-case or best-case can be derived by using derating factors provided in Chapter 1.

For the timing characteristics, 2-dimensional table look-up model has been adopted to yield more accuracy. Based on the combination of input slopes and output loads, the propagation delay is measured from the input crossing 50% VDD to the output crossing 50% VDD. The timing values reported in the tables are also taken from the same voltage level as the switching characteristics with 0.2ns for input slope and 10SL(Standard Load) for output load.

For the power characteristics, the average power consumption is measured on the condition that input slope is 0.2ns and output load is 10SL. Also, the power consumption depends on input switching activity. The power values reported in the tables are also taken from 50% input switching activity. For compiled memory, average read power consumption, average write power consumption and average standby power consumption are available. Average standby power consumption is measured on the condition that CSN (Chip Select Negative) is in disable mode and other signals are in normal operation mode. In dual-port memory, the average power consumption is measured on the condition that only one port is in active mode and the other port is isolated.

BUILT-IN SELF TEST FOR COMPILED MEMORY

SEC provides engineering design services to support BIST (Built-In Self Test) circuitry for the compiled memory macrocell. BIST circuits are designed to detect and to locate a set of fault types, such as stuck-at faults, transition faults, coupling faults and address decoder faults, that impact the functionality of the memory block. As shown in Figure 5-2, SEC adopts BIST architecture which is called SOA (Single Ordered Addressing) algorithm.

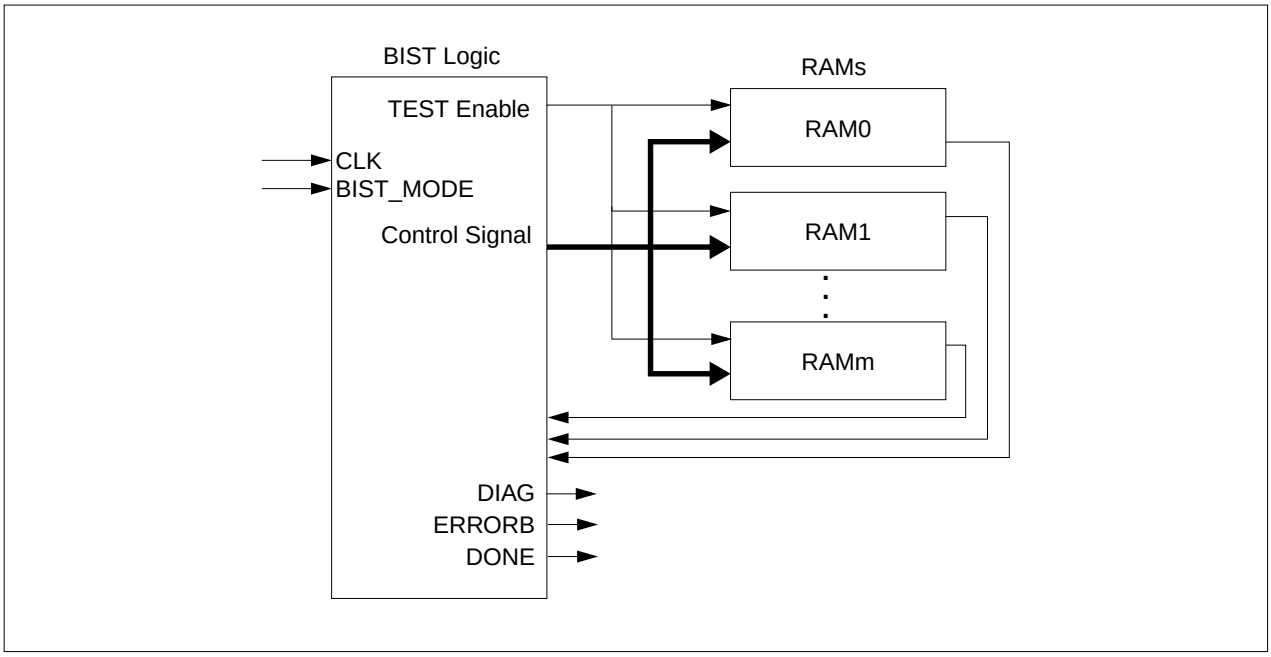


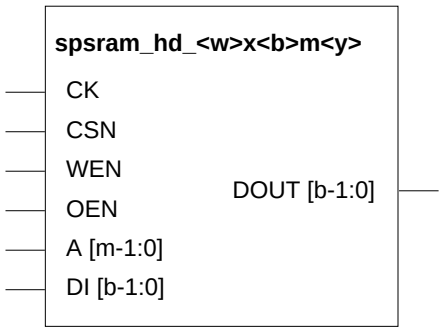
Figure 5-2. Memory BIST Architecture

From Figure 5-2, although several memory macrocells of the same types or the different types exist together in a circuit, SEC supports it as single BIST architecture. For more detailed information regarding to the BIST for compiled memory macrocells, please contact your local representative or head quarter.

SELECTION GUIDE FOR COMPILED MEMORY

Memory Type	Description
SPSRAM_HD	- High-Density single-port synchronous static RAM - Allowable for high-speed and low-power application - Positive-edge triggered clock operation - Flexible aspect ratio (Ymux=4, 8, 16, 32)
SPSRAMBW_HD	- High-Density single-port synchronous static RAM with bit-write - Allowable for high-speed and low-power application - Positive-edge triggered clock operation - Bit-Write feature available - Flexible aspect ratio (Ymux=4, 8, 16, 32)
DPSRAM_HD	- High-Density dual-port synchronous static RAM - Allowable for high-speed and low-power application - Positive-edge triggered clock operation - Flexible aspect ratio (Ymux=4, 8, 16, 32)
SPARAM_HD	- High-Density single-port asynchronous static RAM - Allowable for high-speed and low-power application - Synchronous write operation and Asynchronous read operation - Flexible aspect ratio (Ymux=4, 8, 16, 32)
DROM_HD	- High-Density synchronous diffusion programmable ROM - Allowable for high-speed and low-power application - Diffusion programmable - Positive-edge triggered clock operation - Flexible aspect ratio (Ymux=8, 16, 32)
MROM_HD	- High-Density synchronous metal programmable ROM - Allowable for high-speed and low-power application - Metal-2 programmable - Positive-edge triggered clock operation - Flexible aspect ratio (Ymux=8, 16, 32)

Logic Symbol



NOTES:

1. Words (w) is the number of words in SPSRAM_HD.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. $m = \lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Allowable for high-speed and low-power application
- Synchronous operation
- Duty-free cycle
- Positive-edge clock operation
- Automatic power-down mode available
- Self-controlled circuit available
- Asynchronous tri-state output
- Low noise output optimization
- Separated data I/O
- Flexible aspect ratio
- Zero standby current
- Latched inputs and outputs
- Up to 128Kbits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

SPSRAM_HD is a single-port synchronous static RAM which is provided as a compiler. SPSRAM_HD is intended for use in high-density applications. It is also allowable for high-speed and low-power application. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data on DI[] is written into the memory location specified on A[]. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

CK	CSN	WEN	OEN	A	DI	DOUT	COMMENT
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read cycle

Parameter Description

SPSRAM_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and Column mux(y).

Parameters		Ymux(y)=4	Ymux(y)=8	Ymux(y)=16	Ymux(y)=32
words(w)	Min	32	64	128	256
	Max	1024	2048	4096	8192
	Step	16	32	64	128
bpws(b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

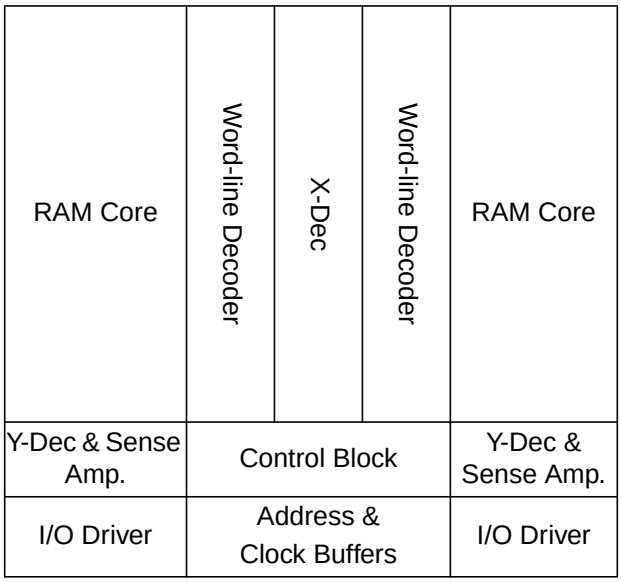
Name	I/O	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

Unit: [SL]

CK	CSN	WEN	OEN	A	DI/DOUT			
					Ymux = 4	Ymux = 8	Ymux = 16	Ymux = 32
1.81	3.01	2.35	0.88	2.98	1.31	1.31	1.31	1.31
					11.68	11.68	11.68	11.68

Block Diagrams



Application Notes

1. Prohibiting over-the-cell routing
In chip-level layout, over-the-cell routing in SPSRAM_HD is not permitted because the memory characteristic may be changed when any signals cross over SPSRAM_HD. It may be caused the severe failure of memory operation.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPSRAM_HD.

4. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckh}	Clock pulse width high
t_{ckl}	Clock pulse width low	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**256**	**512**	**768**	**1024**
bpw	**32**	**64**	**96**	**128**
Timing (ns)				
t_{cyc}	2.97	3.43	3.99	4.66
t_{ckl}	0.93	0.95	0.96	0.95
t_{ckh}	0.97	0.97	0.97	0.97
t_{as}	0.34	0.34	0.34	0.34
t_{ah}	0.56	0.59	0.60	0.60
t_{cs}	0.93	0.95	0.96	0.95
t_{ch}	0.70	0.70	0.70	0.70
t_{ds}	0.35	0.35	0.35	0.35
t_{dh}	0.72	0.78	0.83	0.89
t_{ws}	0.28	0.28	0.28	0.28
t_{wh}	0.56	0.59	0.60	0.60
t_{acc}	2.33	2.62	2.91	3.21
t_{da}	1.81	2.09	2.38	2.68
t_{dz}	0.60	0.64	0.69	0.73
t_{zd}	0.70	0.76	0.81	0.86
t_{od}	0.80	0.85	0.91	0.95
Power (μW/MHz)				
Power_read	671.57	1236.97	1831.97	2456.55
Power_write	717.80	1426.95	2265.93	3234.74
Power_standby	5.50	6.38	7.39	8.52
Area (μm)				
Width	741.69	1287.97	1834.26	2380.55
Height	604.00	908.00	1212.00	1516.00

NOTE: Standby power is measured on condition that CSN is high and the others are in normal operation mode.

Reference Table

*** For Ymux=8** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**512**	**1024**	**1536**	**2048**
bpw	**16**	**32**	**48**	**64**
Timing (ns)				
t_{cyc}	2.97	3.43	3.99	4.66
t_{ckl}	0.93	0.95	0.96	0.95
t_{ckh}	0.97	0.97	0.97	0.97
t_{as}	0.34	0.34	0.34	0.34
t_{ah}	0.56	0.59	0.61	0.60
t_{cs}	0.93	0.95	0.95	0.95
t_{ch}	0.70	0.70	0.70	0.69
t_{ds}	0.36	0.36	0.36	0.36
t_{dh}	0.71	0.75	0.79	0.84
t_{ws}	0.28	0.28	0.28	0.28
t_{wh}	0.56	0.59	0.61	0.60
t_{acc}	2.35	2.63	2.93	3.23
t_{da}	1.83	2.11	2.40	2.70
t_{dz}	0.59	0.63	0.66	0.70
t_{zd}	0.69	0.74	0.78	0.83
t_{od}	0.79	0.84	0.88	0.92
Power (μW/MHz)				
Power_read	497.43	885.09	1302.91	1750.87
Power_write	528.20	994.72	1541.15	2167.48
Power_standby	4.51	4.94	5.58	6.42
Area (μm)				
Width	741.69	1287.97	1834.26	2380.55
Height	604.00	908.00	1212.00	1516.00

NOTE: Standby power is measured on condition that CSN is high and the others are in normal operation mode.

Reference Table

*** For Ymux=16** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**1024**	**2048**	**3072**	**4096**
bpw	**8**	**16**	**24**	**32**
Timing (ns)				
t_{cyc}	2.97	3.43	4.00	4.67
t_{ckl}	0.93	0.95	0.96	0.95
t_{ckh}	0.97	0.97	0.97	0.97
t_{as}	0.34	0.34	0.34	0.34
t_{ah}	0.56	0.59	0.61	0.60
t_{cs}	0.93	0.95	0.95	0.95
t_{ch}	0.70	0.70	0.70	0.70
t_{ds}	0.36	0.36	0.36	0.36
t_{dh}	0.70	0.74	0.78	0.82
t_{ws}	0.28	0.28	0.28	0.28
t_{wh}	0.56	0.59	0.61	0.60
t_{acc}	2.39	2.67	2.96	3.26
t_{da}	1.86	2.14	2.43	2.73
t_{dz}	0.58	0.62	0.65	0.68
t_{zd}	0.69	0.73	0.77	0.81
t_{od}	0.78	0.83	0.86	0.90
Power (μW/MHz)				
Power_read	409.27	735.12	1090.84	1476.43
Power_write	433.88	807.19	1235.74	1719.54
Power_standby	5.23	5.78	6.11	6.21
Area (μm)				
Width	741.69	1287.97	1834.26	2380.55
Height	604.00	908.00	1212.00	1516.00

NOTE: Standby power is measured on condition that CSN is High and the others are in normal operation mode.

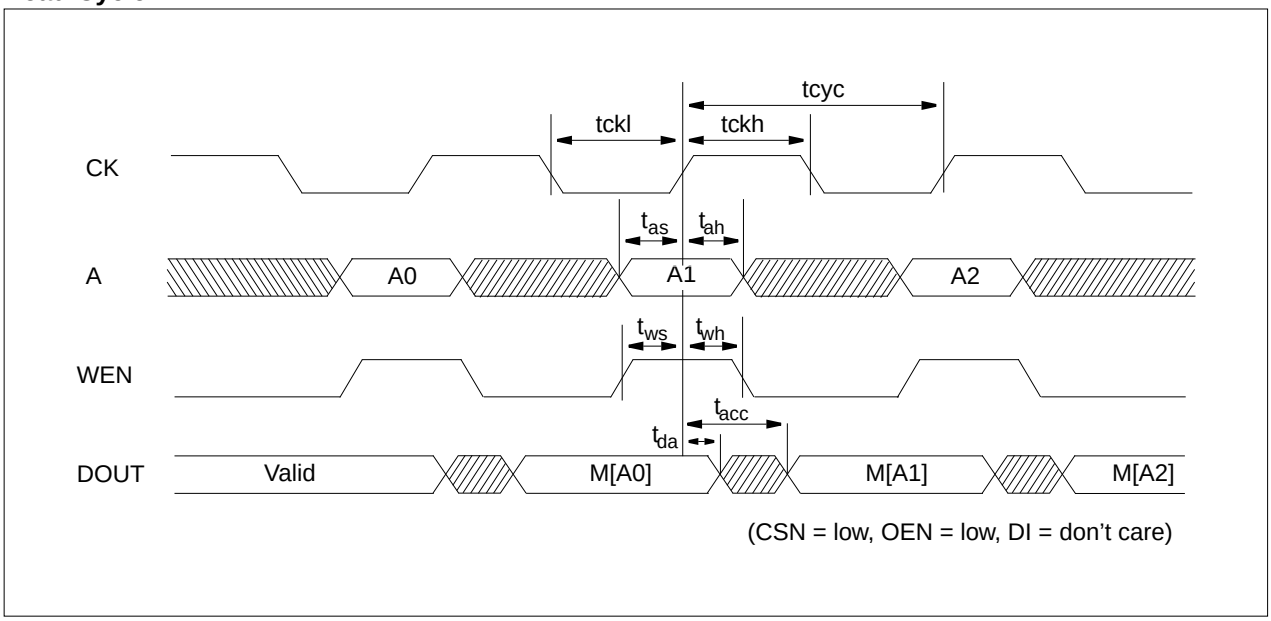
Reference Table

*** For Ymux=32** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

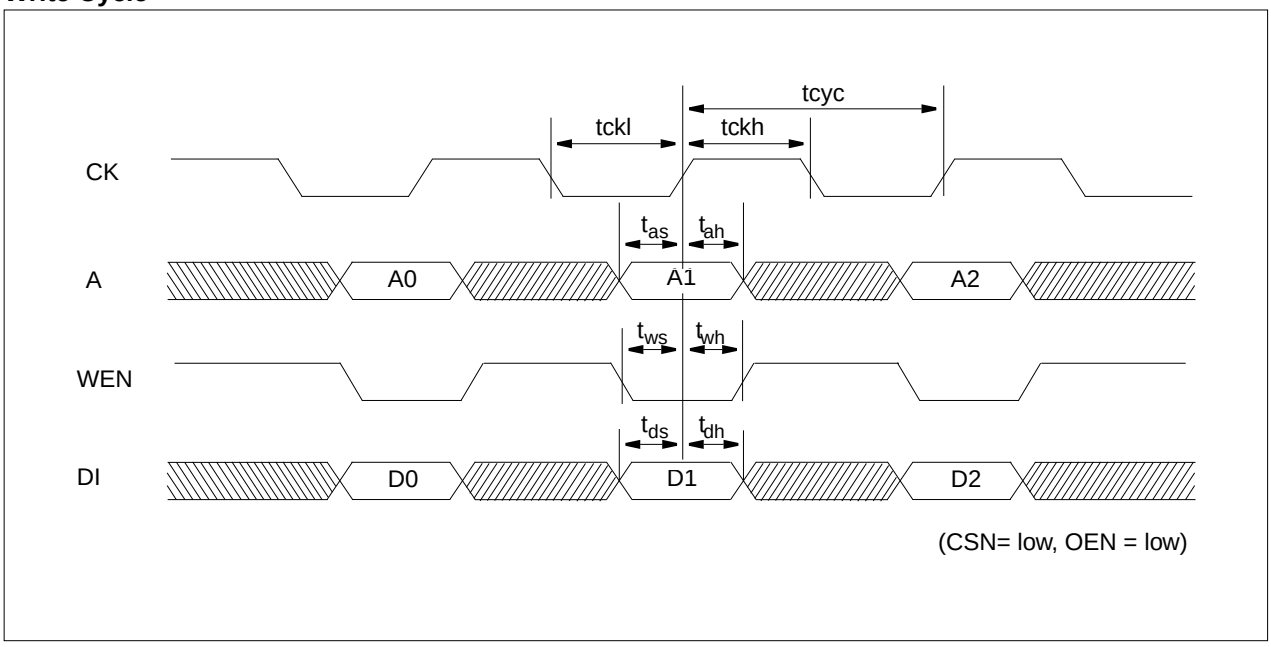
Parameters				
words	**2048**	**4096**	**6144**	**8192**
bpw	**4**	**8**	**12**	**16**
Timing (ns)				
t_{cyc}	2.97	3.43	4.00	4.68
t_{ckl}	0.93	0.95	0.96	0.95
t_{ckh}	0.97	0.97	0.97	0.97
t_{as}	0.34	0.34	0.34	0.34
t_{ah}	0.55	0.57	0.59	0.61
t_{cs}	0.93	0.95	0.96	0.95
t_{ch}	0.70	0.70	0.70	0.69
t_{ds}	0.36	0.36	0.36	0.36
t_{dh}	0.70	0.73	0.76	0.80
t_{ws}	0.28	0.28	0.28	0.28
t_{wh}	0.55	0.57	0.59	0.61
t_{acc}	2.45	2.74	3.03	3.33
t_{da}	1.91	2.19	2.48	2.78
t_{dz}	0.58	0.61	0.64	0.67
t_{zd}	0.69	0.73	0.76	0.80
t_{od}	0.78	0.82	0.86	0.89
Power (μW/MHz)				
Power_read	379.92	683.91	1018.38	1383.32
Power_write	400.94	736.57	1115.48	1537.68
Power_standby	3.80	4.10	4.51	5.04
Area (μm)				
Width	741.69	1287.97	1834.26	2380.55
Height	604.00	908.00	1212.00	1516.00

NOTE: Standby power is measured on condition that CSN is High and the others are in normal operation mode.

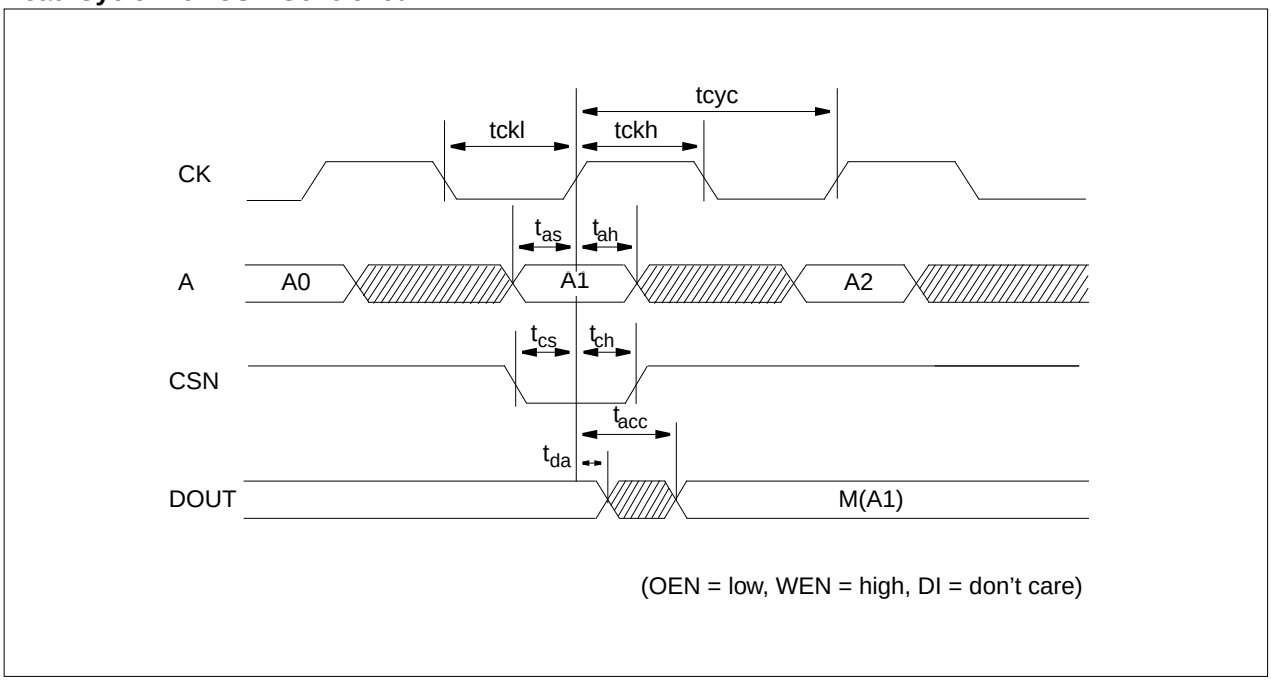
Read Cycle



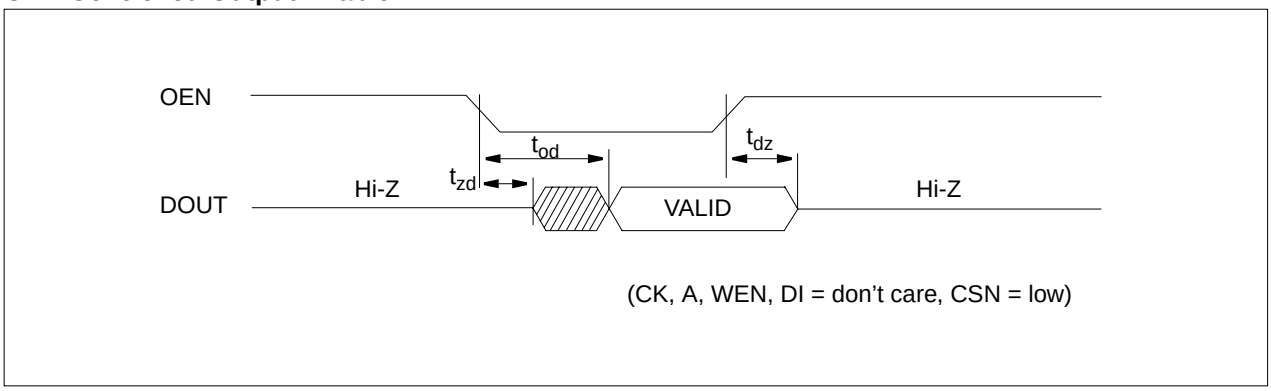
Write Cycle



Read Cycle with CSN Controlled

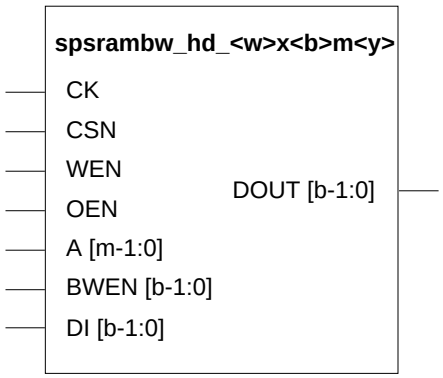


OEN Controlled Output Enable



NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:

1. Words(w) is the number of words in SPSRAMBW_HD
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Allowable for high-speed and low-power application
- Synchronous operation
- Bit-write capability
- Duty-free cycle
- Positive-edge clock operation
- Automatic power-down mode available
- Self-controlled circuit available
- Asynchronous tri-state output
- Low noise output optimization
- Separated data I/O
- Flexible aspect ratio
- Zero standby current
- Latched inputs and outputs
- Up to 128Kbits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

SPSRAMBW_HD is a single-port synchronous static RAM with bit-write capability which is provided as a compiler. SPSRAMBW_HD is intended for use in high-density applications. Basically, its functionality is exactly same as SPSRAM_HD except a bit-write operation which is controlled by BWEN[], named bit-write enable signal bus. Each bit of BWEN[] enables or disables the write operation of its corresponding bit in DI[]. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data bits in DI[], which their corresponding bit(s) in BWEN[] are low, are written into the memory location specified on A[]. When all bits of BWEN[] are high, any data in DI[] are not written into the memory location specified on A[]. When all bits of BWEN[] are low, the data in DI[] are written into the memory location specified on A[], which is exactly same as the write operation in SPSRAM_HD. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPSRAMBW_HD Function Table

CK	CSN	WEN	OEN	A	BWEN	DI	DOUT	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	all L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	all H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read cycle

SPSRAMBW_HD

High-Density Single-Port Synchronous SRAM with Bit-write

Parameter Description

SPSRAMBW_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y):

Parameters		Ymux(y)=4	Ymux(y)=8	Ymux(y)=16	Ymux(y)=32
words(w)	Min	32	64	128	256
	Max	1024	2048	4096	8192
	Step	16	32	64	128
bpws(b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

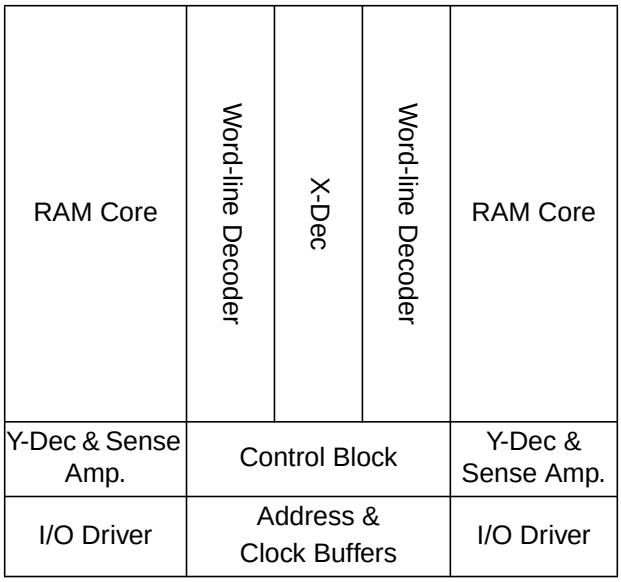
Name	I/O	Description
CK	Clock	Clock input. CSN, WEN, A[], BWEN[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
BWEN[]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A[]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI[]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT[]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

Unit: [SL]

CK	CSN	WEN	BWEN	OEN	A	DI/DOUT		
						Ymux = 4	Ymux = 8	Ymux = 16
1.81	3.01	2.35	1.31	0.88	2.98	1.31	1.31	1.31
						11.68	11.68	11.68

Block Diagrams



Application Notes

1. Prohibiting over-the-cell routing
In chip-level layout, over-the-cell routing in SPSRAMBW_HD is not permitted because the memory characteristic may be changed when any signals cross over SPSRAMBW_HD. It may be caused the severe failure of memory operation.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPSRAMBW_HD.

4. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckh}	Clock pulse width high
t_{ckl}	Clock pulse width low	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{bws}	BWEN setup time
t_{bwh}	BWEN hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**256**	**512**	**768**	**1024**
bpw	**32**	**64**	**96**	**128**
Timing (ns)				
t_{cyc}	2.97	3.43	3.99	4.66
t_{ckl}	0.93	0.95	0.96	0.95
t_{ckh}	0.97	0.97	0.97	0.97
t_{as}	0.34	0.34	0.34	0.34
t_{ah}	0.56	0.59	0.60	0.60
t_{cs}	0.93	0.95	0.96	0.95
t_{ch}	0.70	0.70	0.70	0.70
t_{ds}	0.35	0.35	0.35	0.35
t_{dh}	0.72	0.78	0.83	0.89
t_{bws}	0.35	0.35	0.35	0.35
t_{bwh}	0.72	0.78	0.83	0.89
t_{ws}	0.28	0.28	0.28	0.28
t_{wh}	0.59	0.59	0.60	0.60
t_{acc}	2.33	2.62	2.91	3.21
t_{da}	1.81	2.09	2.38	2.68
t_{dz}	0.60	0.64	0.69	0.73
t_{zd}	0.70	0.76	0.81	0.86
t_{od}	0.80	0.85	0.91	0.95
Power (μW/MHz)				
Power_read	671.57	1236.97	1831.97	2456.55
Power_write	717.80	1426.95	2265.93	3234.74
Power_standby	5.50	6.38	7.39	8.52
Area (μm)				
Width	741.69	1287.97	1834.26	2380.55
Height	604.00	908.00	1212.00	1516.00

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

*** For Ymux=8** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**512**	**1024**	**1536**	**2048**
bpw	**16**	**32**	**48**	**64**
Timing (ns)				
t_{cyc}	2.97	3.43	3.99	4.66
t_{ckl}	0.93	0.95	0.96	0.95
t_{ckh}	0.97	0.97	0.97	0.97
t_{as}	0.34	0.34	0.34	0.34
t_{ah}	0.56	0.59	0.61	0.60
t_{cs}	0.93	0.95	0.95	0.95
t_{ch}	0.70	0.70	0.70	0.69
t_{ds}	0.36	0.36	0.36	0.36
t_{dh}	0.71	0.75	0.79	0.84
t_{bws}	0.36	0.36	0.36	0.36
t_{bwh}	0.71	0.75	0.79	0.84
t_{ws}	0.28	0.28	0.28	0.28
t_{wh}	0.56	0.59	0.61	0.60
t_{acc}	2.35	2.63	2.93	3.23
t_{da}	1.83	2.11	2.40	2.70
t_{dz}	0.59	0.63	0.66	0.73
t_{zd}	0.69	0.74	0.78	0.83
t_{od}	0.79	0.84	0.88	0.92
Power (μW/MHz)				
Power_read	497.43	885.09	1302.91	1750.87
Power_write	528.20	994.72	1541.15	2167.48
Power_standby	4.51	4.94	5.58	6.42
Area (μm)				
Width	741.69	1287.97	1834.26	2380.55
Height	604.00	908.00	1212.00	1516.00

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

*** For Ymux=16** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**1024**	**2048**	**3072**	**4096**
bpw	**8**	**16**	**24**	**32**
Timing (ns)				
t_{cyc}	2.97	3.43	4.00	4.67
t_{ckl}	0.93	0.95	0.96	0.95
t_{ckh}	0.97	0.97	0.97	0.97
t_{as}	0.34	0.34	0.34	0.34
t_{ah}	0.56	0.59	0.61	0.60
t_{cs}	0.93	0.95	0.95	0.95
t_{ch}	0.70	0.70	0.70	0.70
t_{ds}	0.36	0.36	0.36	0.36
t_{dh}	0.70	0.74	0.78	0.82
t_{bws}	0.36	0.36	0.36	0.36
t_{bwh}	0.70	0.74	0.78	0.82
t_{ws}	0.28	0.28	0.28	0.28
t_{wh}	0.56	0.59	0.61	0.60
t_{acc}	2.39	2.67	2.96	3.26
t_{da}	1.86	2.14	2.43	2.73
t_{dz}	0.58	0.62	0.65	0.68
t_{zd}	0.69	0.73	0.77	0.81
t_{od}	0.78	0.83	0.86	0.90
Power (μW/MHz)				
Power_read	409.27	735.12	1090.84	1476.43
Power_write	433.88	807.19	1235.74	1719.54
Power_standby	5.23	5.78	6.11	6.21
Area (μm)				
Width	741.69	1287.97	1834.26	2380.55
Height	604.00	908.00	1212.00	1516.00

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

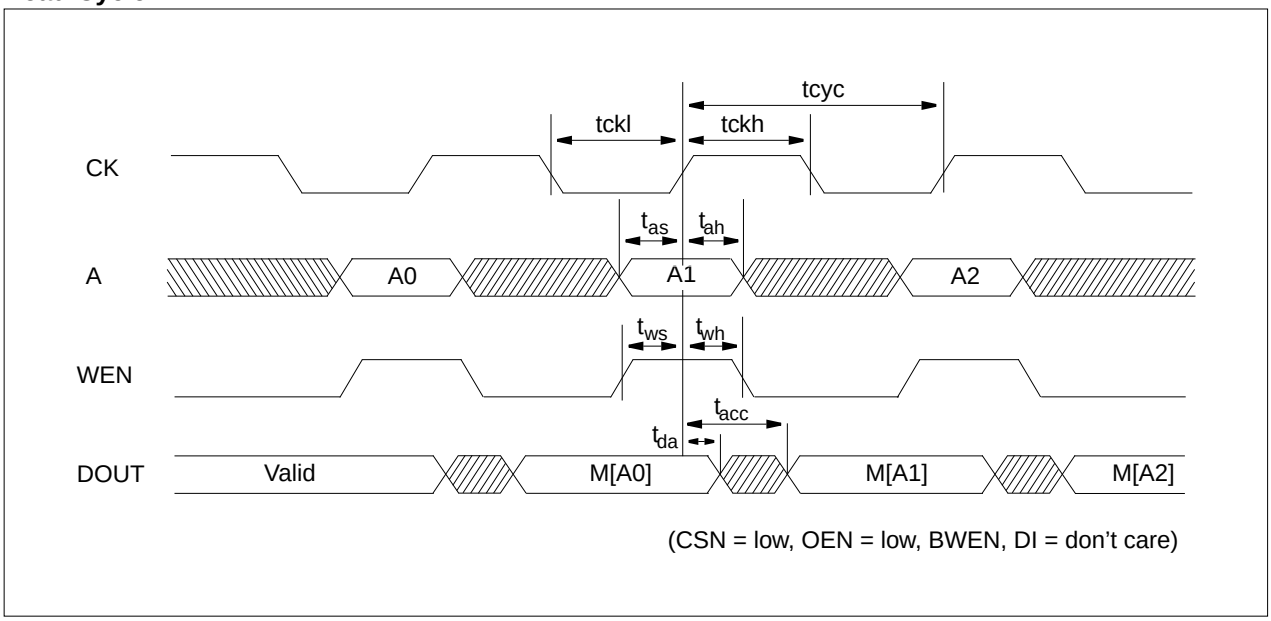
Reference Table

*** For Ymux=32** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

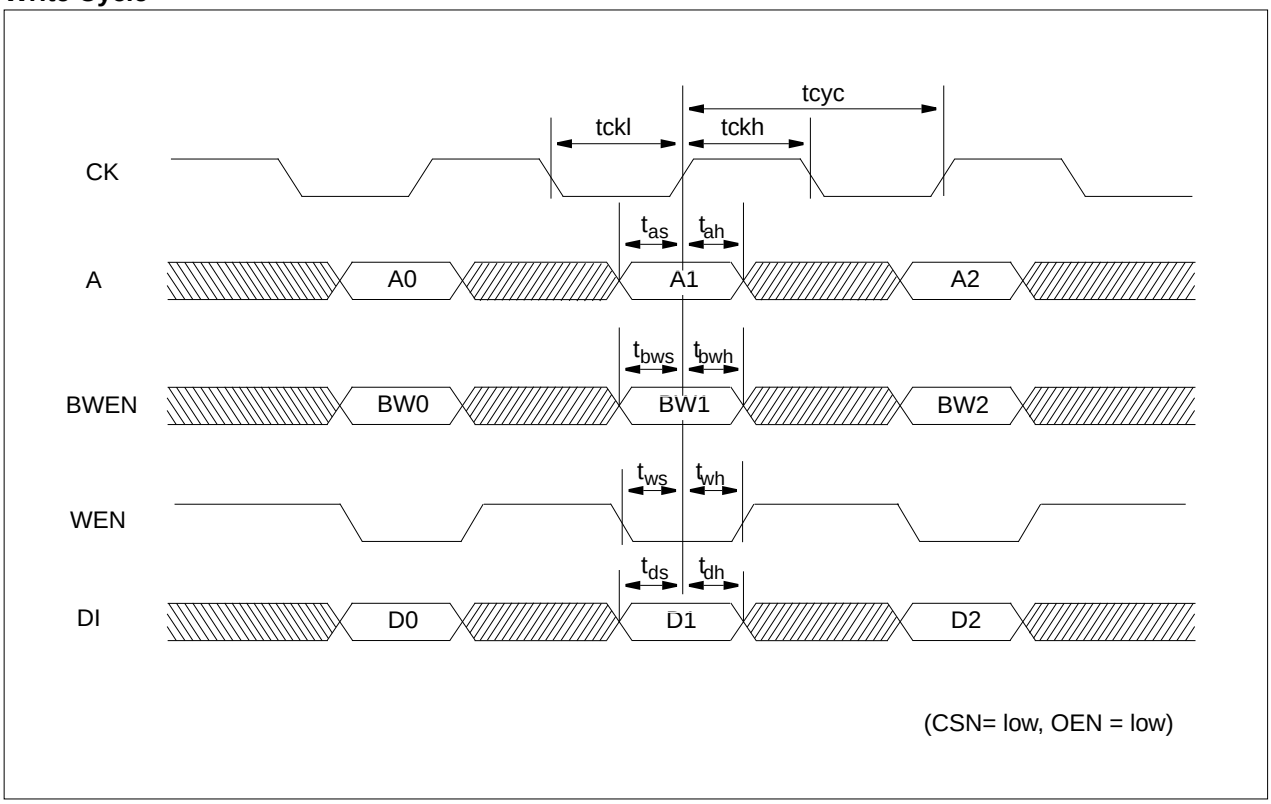
Parameters				
words	**2048**	**4096**	**6144**	**8192**
bpw	**4**	**8**	**12**	**16**
Timing (ns)				
t_{cyc}	2.97	3.43	4.00	4.68
t_{ckl}	0.93	0.95	0.96	0.95
t_{ckh}	0.97	0.97	0.97	0.97
t_{as}	0.34	0.34	0.34	0.34
t_{ah}	0.55	0.57	0.59	0.61
t_{cs}	0.93	0.95	0.96	0.95
t_{ch}	0.70	0.70	0.70	0.69
t_{ds}	0.36	0.36	0.36	0.36
t_{dh}	0.70	0.73	0.76	0.80
t_{bws}	0.36	0.36	0.36	0.36
t_{bwh}	0.70	0.73	0.76	0.80
t_{ws}	0.28	0.28	0.28	0.28
t_{wh}	0.55	0.57	0.59	0.61
t_{acc}	2.45	2.74	3.03	3.33
t_{da}	1.91	2.19	2.48	2.78
t_{dz}	0.58	0.61	0.64	0.67
t_{zd}	0.69	0.73	0.76	0.80
t_{od}	0.78	0.82	0.86	0.89
Power (μW/MHz)				
Power_read	379.92	683.91	1018.38	1383.32
Power_write	3.80	4.10	4.51	5.04
Power_standby	741.69	1287.97	1834.26	2380.55
Area (μm)				
Width	2.97	3.43	4.00	4.68
Height	0.93	0.95	0.96	0.95

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

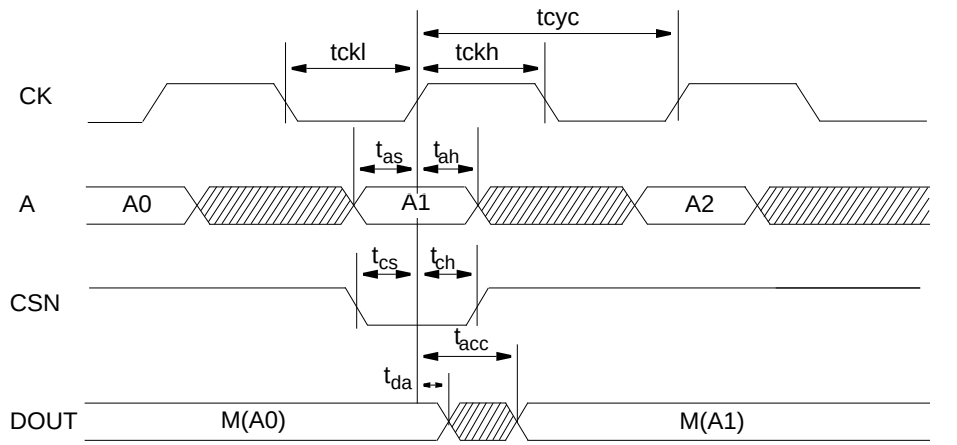
Read Cycle



Write Cycle

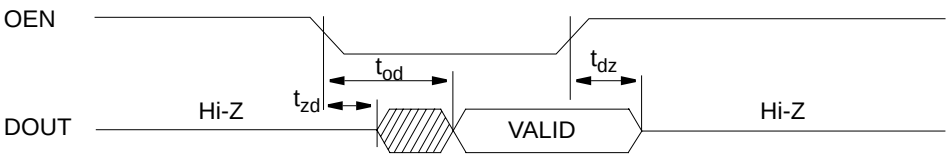


Read Cycle with CSN Controlled



(OEN = low, WEN = high, BWEN, DI = don't care)

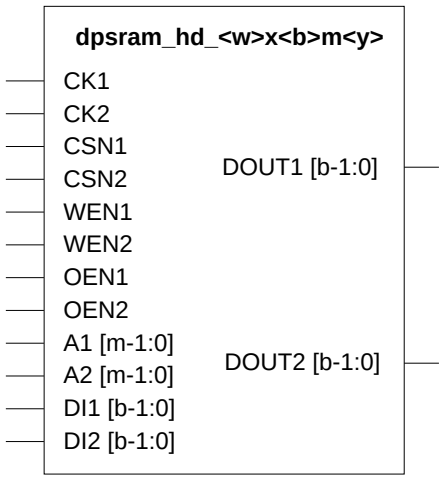
OEN Controlled Output Enable



(CSN, CK, A, WEN, BWEN, DI = don't care)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:

1. Words (w) is the number of words in DPSRAM_HD.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Allowable for high-speed and low-power application
- Synchronous operation
- Duty-free cycle
- Positive-edge clock operation
- Automatic power-down mode available
- Self-controlled circuit available
- Asynchronous tri-state output
- Low noise output optimization
- Separated data I/O
- Flexible aspect ratio
- Zero standby current
- Latched inputs and outputs
- Up to 64Kbits capacity
- Up to 4K number of words
- Up to 128 number of bits per word

Function Description

DPSRAM_HD is a dual-port synchronous static RAM which is provided as a compiler. DPSRAM_HD is intended for use in high-density applications. It is also allowable for high-speed and low-power applications. On the rising edge of CK, the write cycle is initiated when WEN1 (WEN2) is low and CSN1 (CSN2) is low. The data on DI1[] (DI2[]) is written into the memory location specified on A1[] (A2[]). During the write cycle, DOUT1[] (DOUT2[]) remains stable. On the rising edge of CK, the read cycle is initiated when WEN1(WEN2) is high and CSN1 (CSN2) is low. The data at DOUT1[] (DOUT2[]) become valid after a delay. While in standby mode that CSN1 (CSN2) is high, A1[] (A2[]) and DI1[] (DI2[]) are disabled, data stored in the memory is retained and DOUT1[] (DOUT2[]) remains stable. When OEN1 (OEN2) is high, DOUT1[] (DOUT2[]) is placed in a high-impedance state. Each port is fully independent.

DPSRAM_HD Function Table

CK1 CK2	CSN1 CSN2	WEN1 WEN2	OEN1 OEN2	A1 A2	DI1 DI2	DOUT1 DOUT2	Comment
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read cycle

DPSRAM_HD

High-Density Dual-Port Synchronous Static RAM

Parameter Description

DPSRAM_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y).

Parameters		Ymux = 4	Ymux = 8	Ymux = 16	Ymux = 32
Words (w)	Min	32	64	128	256
	Max	512	1024	2048	4096
	Step	16	32	64	128
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

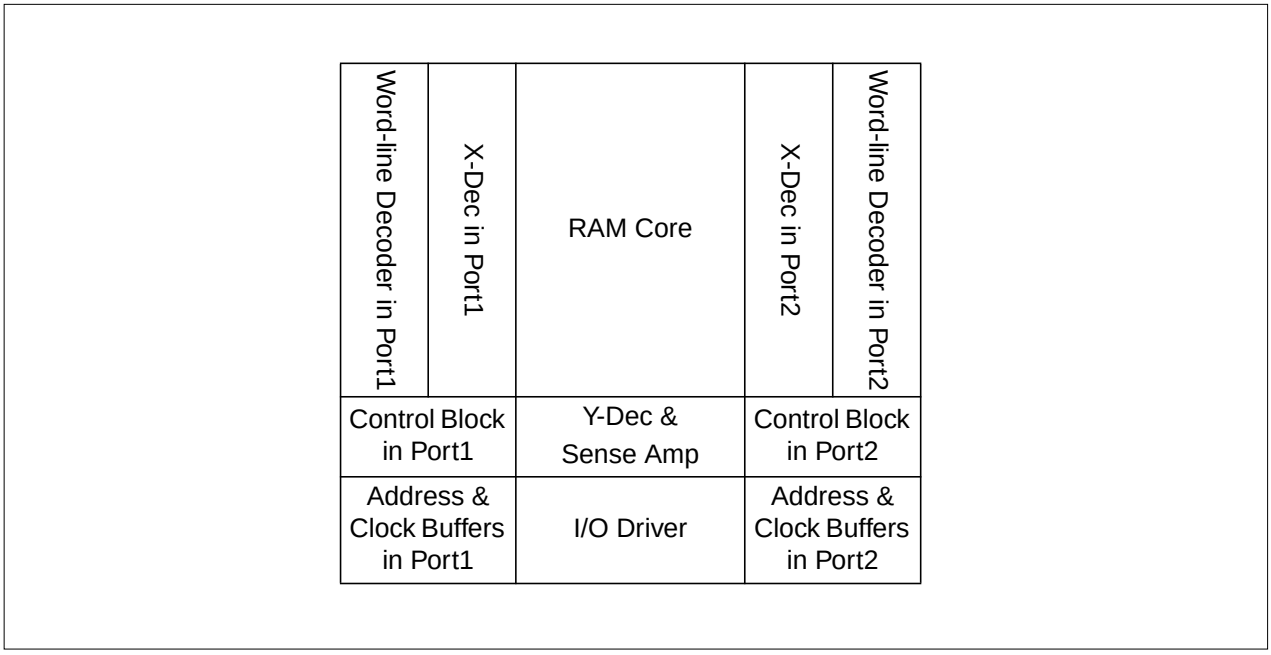
Name	Type	Description
CK1 CK2	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN1 CSN2	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN1 WEN2	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
OEN1 OEN2	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A1 [ ] A2 [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI1 [ ] DI2 [ ]	Data Input	Data input bus. data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT1 [ ] DOUT2 [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	DI/DOUT			
					Ymux = 4	Ymux = 8	Ymux = 16	Ymux = 32
1.40	2.56	2.04	0.75	2.56	0.72	0.72	0.72	0.72
					14.83	14.83	14.83	14.83

Block Diagram



Application Notes

1. Prohibiting over-the-cell routing
In chip-level layout, over-the-cell routing in DPSRAM_HD is not permitted because the memory characteristic may be changed when any signals are cross over DPSRAM_HD. It may be caused the severe failure of memory operation.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DPSRAM_HD.

4. Contention mode in same address access
In DPSRAM_HD, simultaneous operation by both ports on the same memory address, as write/write, write/read or read/write operation, causes a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal at the rising edge of CK. DPSRAM_HD has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot end and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports. In write/write operation, the data stored at the current address will be unpredictable. In write/read or read/write operation, the read port is invalid while the write port is still valid. If you want to avoid the contention mode, you have to give the value greater than tcc (clock-to-clock setup time). However, simultaneous read/read is allowable without any restrictions. Power reduction during standby mode.

5. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{cc}	Clock to clock setup time
t_{as}	Address setup time	t_{ah}	Address hold time
t_{cs}	CSN setup time	t_{ch}	CSN hold time
t_{ds}	Data-In setup time	t_{dh}	Data-In hold time
t_{ws}	WEN setup time	t_{wh}	WEN hold time
t_{acc}	Data access time	t_{da}	De-access time
t_{dz}	DOUT drive to high-Z time	t_{zd}	DOUT high-Z to drive time
t_{od}	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**128**	**256**	**384**	**512**
bpw	**32**	**64**	**96**	**128**
Timing (ns)				
t_{cyc}	3.07	3.71	4.43	5.23
t_{ckl}	0.93	0.95	0.96	0.96
t_{ckh}	0.97	0.99	1.05	1.16
t_{cc}	1.41	1.95	2.60	3.35
t_{as}	0.72	0.67	0.62	0.57
t_{ah}	0.56	0.59	0.60	0.60
t_{cs}	0.93	0.95	0.96	0.96
t_{ch}	0.69	0.69	0.69	0.69
t_{ds}	0.43	0.43	0.43	0.43
t_{dh}	0.72	0.86	1.01	1.17
t_{ws}	0.28	0.28	0.28	0.28
t_{wh}	0.56	0.59	0.60	0.60
t_{acc}	2.41	2.86	3.36	3.90
t_{da}	1.98	2.43	2.93	3.48
t_{dz}	0.68	0.85	1.05	1.25
t_{zd}	0.78	0.98	1.19	1.41
t_{od}	0.87	1.07	1.28	1.51
Power (μW/MHz)				
Power_read	514.19	983.36	1481.00	2007.12
Power_write	699.81	1508.19	2502.21	3681.86
Power_standby	4.55	4.84	4.66	4.00
Area (μm)				
Width	1099.10	1938.75	2778.40	3618.06
Height	593.65	794.45	995.25	1196.05

NOTES:

1. In power consumption of DPSRAM_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

*** For Ymux=8** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**256**	**512**	**768**	**1024**
bpw	**16**	**32**	**48**	**64**
Timing (ns)				
t_{cyc}	3.07	3.71	4.43	5.23
t_{ckl}	0.93	0.95	0.96	0.96
t_{ckh}	0.98	0.98	0.98	0.98
t_{cc}	1.41	1.95	2.60	3.36
t_{as}	0.72	0.67	0.62	0.58
t_{ah}	0.56	0.57	0.59	0.61
t_{cs}	0.93	0.95	0.96	0.96
t_{ch}	0.69	0.69	0.69	0.69
t_{ds}	0.43	0.43	0.43	0.43
t_{dh}	0.68	0.78	0.88	0.99
t_{ws}	0.28	0.28	0.28	0.28
t_{wh}	0.56	0.57	0.59	0.61
t_{acc}	2.43	2.88	3.38	3.93
t_{da}	1.99	2.44	2.94	3.49
t_{dz}	0.61	0.72	0.84	0.97
t_{zd}	0.70	0.83	0.96	1.10
t_{od}	0.80	0.92	1.05	1.19
Power (μW/MHz)				
Power_read	452.19	862.38	1299.88	1764.67
Power_write	635.06	1364.14	2258.49	3318.12
Power_standby	4.81	5.34	5.40	5.00
Area (μm)				
Width	1099.10	1938.75	2778.40	3618.06
Height	593.65	794.45	995.25	1196.05

NOTES:

1. In power consumption of DPSRAM_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

*** For Ymux=16** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**512**	**1024**	**1536**	**2048**
bpw	**8**	**16**	**24**	**32**
Timing (ns)				
t_{cyc}	3.06	3.70	4.43	5.24
t_{ckl}	0.93	0.95	0.96	0.96
t_{ckh}	0.98	0.98	0.98	0.98
t_{cc}	1.41	1.95	2.60	3.36
t_{as}	0.72	0.67	0.62	0.58
t_{ah}	0.56	0.59	0.60	0.60
t_{cs}	0.93	0.94	0.95	0.97
t_{ch}	0.69	0.69	0.69	0.69
t_{ds}	0.42	0.42	0.42	0.42
t_{dh}	0.66	0.73	0.81	0.89
t_{ws}	0.28	0.28	0.28	0.28
t_{wh}	0.56	0.59	0.60	0.60
t_{acc}	2.46	2.91	3.41	3.96
t_{da}	2.02	2.47	2.97	3.52
t_{dz}	0.58	0.65	0.73	0.82
t_{zd}	0.67	0.76	0.85	0.93
t_{od}	0.76	0.85	0.94	1.03
Power (μW/MHz)				
Power_read	413.37	799.77	1213.15	1653.50
Power_write	597.81	1292.52	2143.01	3149.29
Power_standby	5.06	5.95	6.86	7.80
Area (μm)				
Width	1099.10	1938.75	2778.40	3618.16
Height	593.65	794.45	995.25	1196.05

NOTES:

1. In power consumption of DPSRAM_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

*** For Ymux=32** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

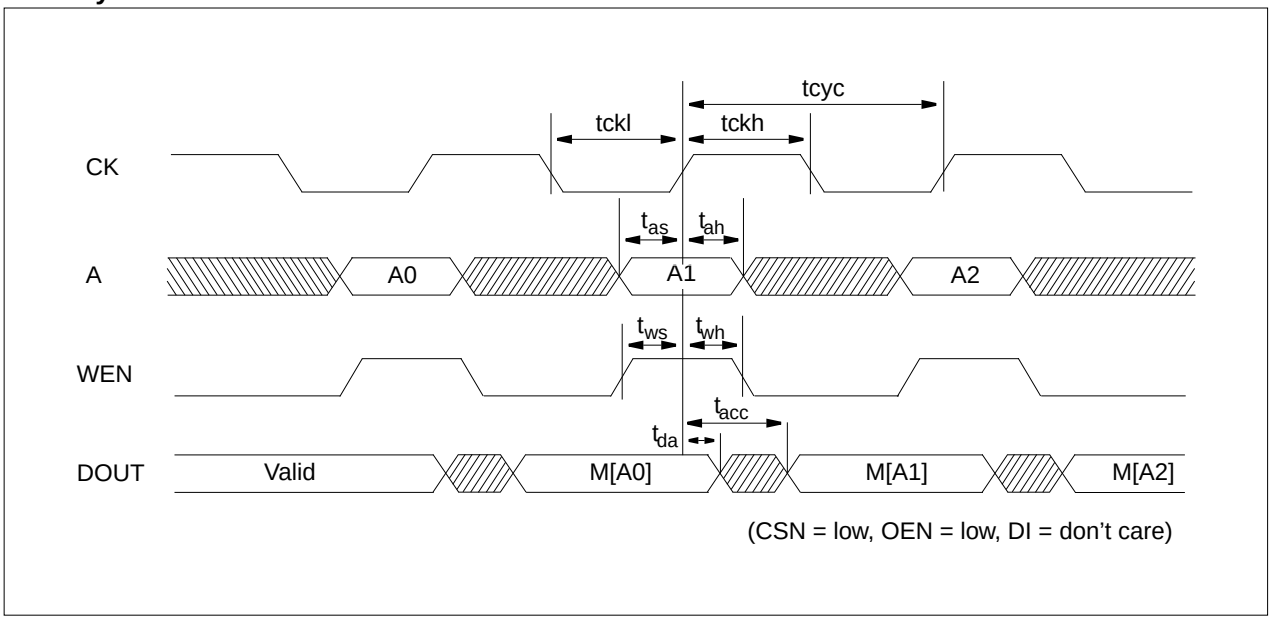
Parameters				
words	**1024**	**2048**	**3072**	**4096**
bpw	**4**	**8**	**12**	**16**
Timing (ns)				
t_{cyc}	3.04	3.69	4.43	5.25
t_{ckl}	0.93	0.95	0.96	0.96
t_{ckh}	0.98	0.98	0.98	0.98
t_{cc}	1.41	1.95	2.60	3.36
t_{as}	0.72	0.67	0.62	0.57
t_{ah}	0.56	0.59	0.60	0.60
t_{cs}	0.93	0.95	0.96	0.96
t_{ch}	0.69	0.69	0.69	0.69
t_{ds}	0.42	0.42	0.42	0.42
t_{dh}	0.65	0.71	0.78	0.85
t_{ws}	0.28	0.28	0.28	0.28
t_{wh}	0.56	0.59	0.60	0.60
t_{acc}	2.53	2.98	3.48	4.03
t_{da}	2.07	2.52	3.02	3.58
t_{dz}	0.56	0.62	0.68	0.74
t_{zd}	0.65	0.72	0.78	0.85
t_{od}	0.74	0.81	0.88	0.95
Power (μW/MHz)				
Power_read	375.30	757.77	168.55	1607.65
Power_write	535.02	1218.49	2051.39	3033.74
Power_standby	4.55	4.84	5.13	5.41
Area (μm)				
Width	1099.10	1938.75	2778.40	3618.16
Height	593.65	794.45	995.25	1196.05

NOTES:

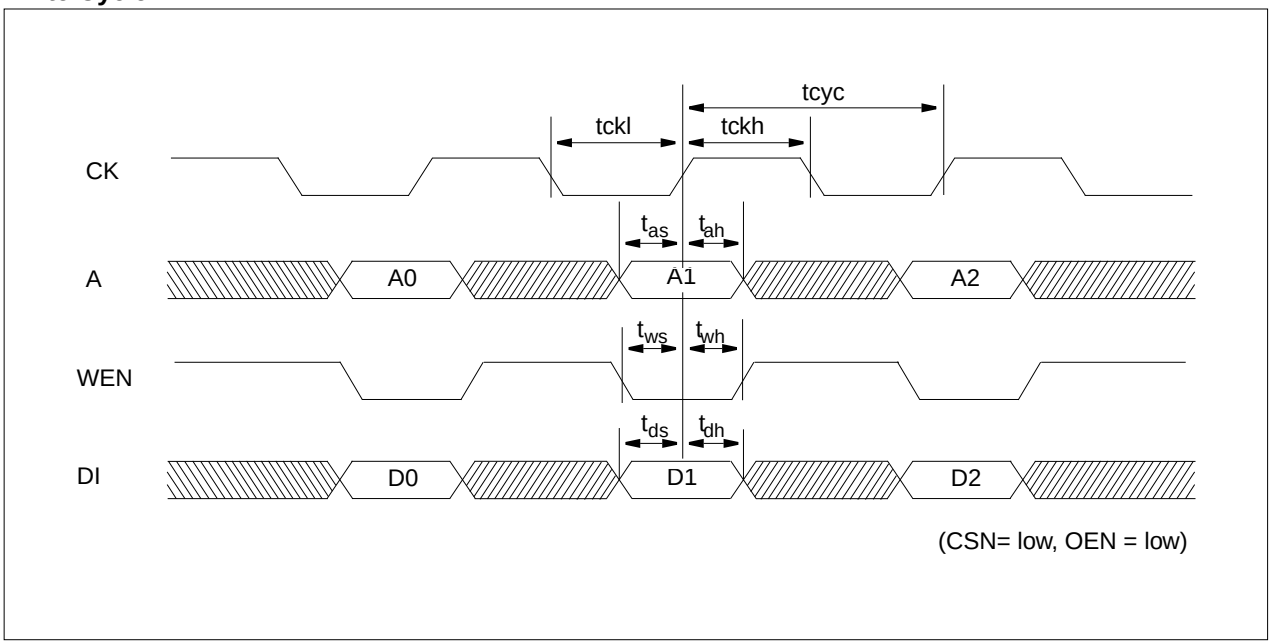
1. In power consumption of DPSRAM_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Timing Diagrams

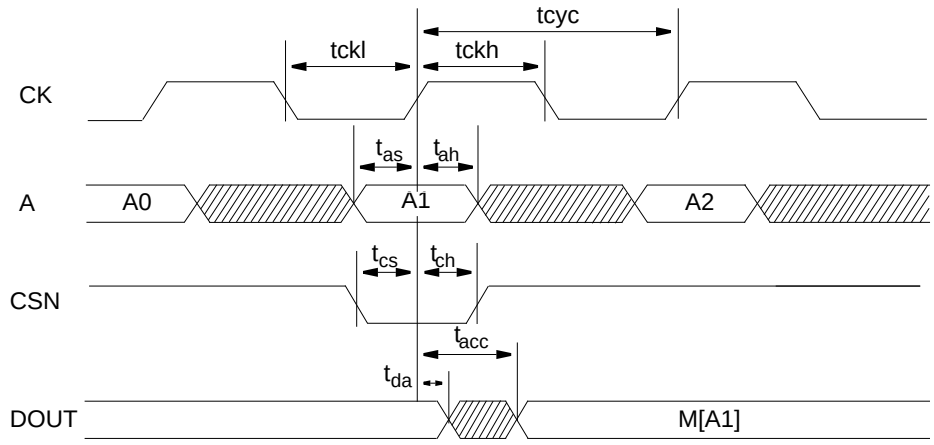
Read Cycle



Write Cycle

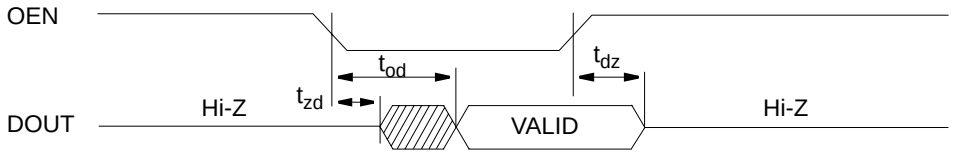


Read Cycle with CSN Controlled



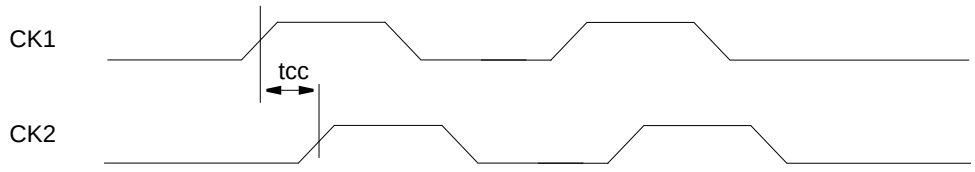
(OEN = low, WEN = high, DI = don't care)

OEN Controlled Output Enable



(CK, A, WEN, DI = don't care, CSN = low)

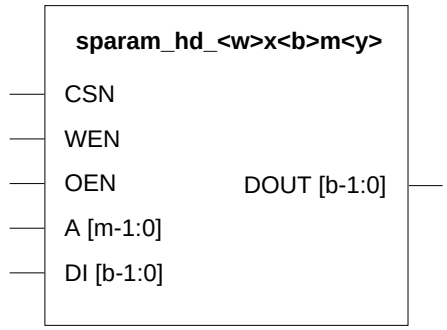
Contention Mode



(A1 = A2)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:
1. Words (w) is the number of words in SPARAM_HD.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Allowable for high-speed and low-power application
- Asynchronous operation
- Address transition detector
- Write enable transition detector
- Chip select transition detector
- Automatic power-down mode
- Stand-by (power down) mode available
- Asynchronous tri-state output
- Low noise output optimization
- Separated data I/O
- Flexible aspect ratio
- Zero standby current
- Up to 128Kbits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

SPARAM_HD is a single-port asynchronous static RAM which is provided as a compiler. SPARAM_HD is intended for use in high-density applications. It is also allowable for high-speed and low-power applications. At the falling edge of WEN, the write cycle is initiated. At the rising edge of WEN, the write cycle is ended. During the write cycle, the data on DI[] is written into the memory location specified on A[]. The read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay whenever A[] transition is detected. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPARAM_HD Function Table

CSN	WEN	OEN	A	DI	DOUT	Comment
X	X	H	X	X	Z	Unconditional tri-state output
H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
L	↓	L	Valid	Valid	DOUT(t-1)	Write cycle starts
L	↑	L	Valid	Valid	MEM(A)	Write cycle ends and read cycle starts
L	L	L	Stable	Valid	DOUT(t-1)	Write cycle
L	H	L	Toggle	X	MEM(A)	Read cycle

SPARAM_HD

High-Density Single-Port Asynchronous Static RAM

Parameter Description

SPARAM_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y).

Parameter		Ymux(y)=4	Ymux(y)=8	Ymux(y)=16	Ymux(y)=32
words(w)	Min	32	64	128	256
	Max	1024	2048	4096	8192
	Step	16	32	64	128
bpws(b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

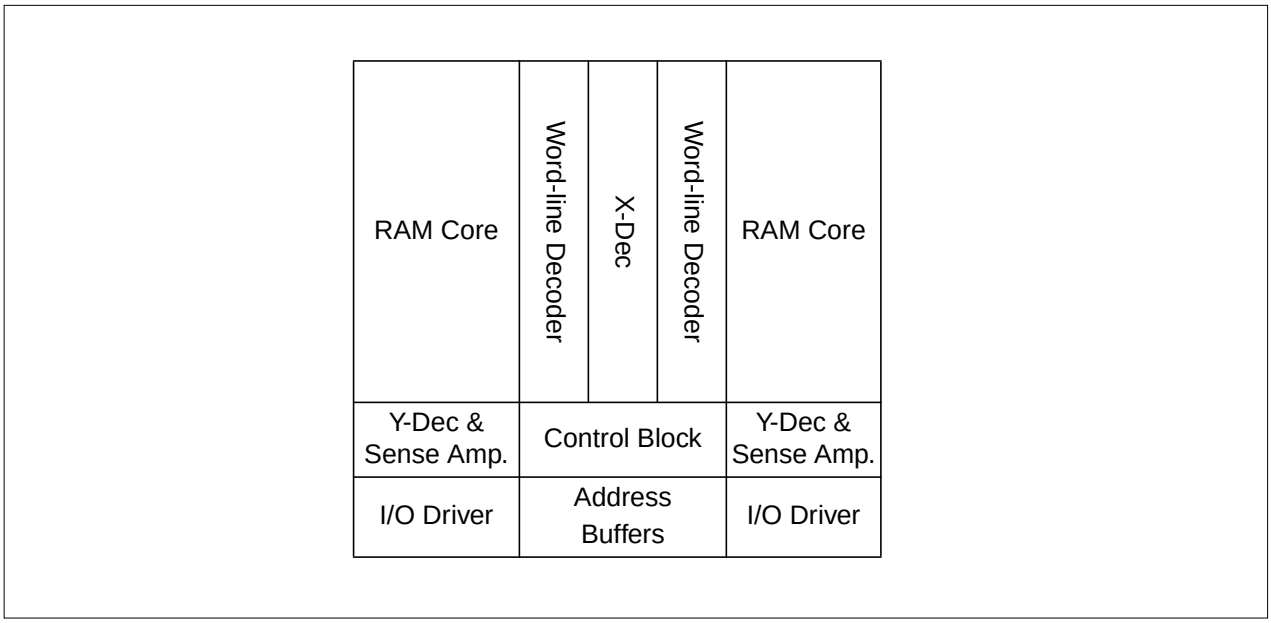
Name	I/O	Description
CSN	Chip Enable	Chip select input. The chip select signal acts as the memory enable signal for selections of multiple blocks. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur. Conversely, if low, a read or write access can occur. When CSN falls, an access is initiated.
WEN	Read/Write Enable	Write enable input. The write enable signal selects the type of memory access. The high state for a read access and the low state for a write access. Upon the rising edge of WEN, a write access completed and a read access initiated.
OEN	Data Output Enable	Output enable input. The output enable signal controls the output drivers from driven to tri-state condition unconditionally.
A [ ]	Address	Address Input bus. A[ ] should be stable when WEN is low. The address selects the location to be accessed. When the address changes, the transition is detected and the internal clock pulse is generated.
DI [ ]	Data Input	Data input bus. The data input is written to the accessed location when WEN is low.
DOUT [ ]	Data Output	Data output bus. The data output is data stored in the accessed location during a read access. Data output driver has tri-state logic. When OEN is low, the driver drives a certain value. Otherwise, data output keeps Hi-Z state. During a write access, data on DOUT is predictable.

Pin Capacitance

Unit: [SL]

CSN	WEN	OEN	A	DI/DOUT			
				Ymux = 4	Ymux = 8	Ymux = 16	Ymux = 32
13.97	7.17	2.17	2.77	2.95	2.95	2.95	2.95
				3.55	3.55	3.55	3.55

Block Diagrams



Application Notes

1. Prohibiting over-the-cell routing
In chip-level layout, over-the-cell routing in SPARAM_HD is not permitted because the memory characteristic may be changed when any signals are cross over SPARAM_HD. It may be caused the severe failure of memory operation.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPARAM_HD.

4. Avoiding short transition on the address bus
In SPARAM_HD, rather than the write operation which is synchronously performed by WEN signal, the read operation is asynchronously performed whenever the address transition is occurred. In this case, if the short transition on the address, called a skew, is happened, since SPARAM_HD recognizes the short address transition as the stable address transition and do perform a read operation. At that time, while in the read operation the stable address cycle time (tcyc) is required. The essential requirement to recognize valid address transition is that at least minimum address period should be equal or greater than tacc (access time).

5. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Address cycle time	t_{as}	Address setup time
t_{cas}	Address setup time for CSN rise	t_{ah}	Address hold time
t_{wh}	WEN hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{wen}	WEN pulse width low
t_{acc}	Data access time for read cycle	t_{wacc}	Data access time for WEN rise
t_{da}	De-access time	t_{wda}	De-access time for WEN rise
t_{zd}	DOUT high-Z to drive time	t_{dz}	DOUT drive to high-Z time
t_{od}	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**256**	**512**	**768**	**1024**
bpw	**32**	**64**	**96**	**128**
Timing (ns)				
t_{cyc}	3.72	4.21	4.72	5.23
t_{as}	0.10	0.10	0.10	0.10
t_{cas}	3.73	4.23	4.73	5.22
t_{ah}	0.82	1.13	1.44	1.76
t_{wh}	3.73	4.23	4.73	5.22
t_{ds}	0.36	0.48	0.59	0.68
t_{dh}	0.37	0.45	0.53	0.61
t_{cs}	0.10	0.10	0.10	0.10
t_{ch}	1.00	1.12	1.23	1.35
t_{wen}	2.44	2.74	3.04	3.34
t_{acc}	3.72	4.21	4.72	5.23
t_{da}	0.43	0.55	0.68	0.80
t_{wda}	0.10	0.10	0.10	0.10
t_{wacc}	1.00	1.12	1.24	1.35
t_{dz}	0.59	0.69	0.80	0.90
t_{zd}	0.37	0.49	0.61	0.72
t_{od}	0.62	0.74	0.86	0.98
Power (μW/MHz)				
Power_read	377.36	703.54	1049.72	1415.93
Power_write	676.68	1385.53	2149.09	2967.37
Power_standby	54.54	93.59	132.74	172.01
Area (μm)				
Width	831.95	1382.72	1933.49	2484.27
Height	585.22	889.22	1193.22	1497.22

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

*** For Ymux=8** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**512**	**1024**	**1536**	**2048**
bpw	**16**	**32**	**48**	**64**
Timing (ns)				
t_{cyc}	3.72	4.21	4.72	5.24
t_{as}	0.10	0.10	0.10	0.10
t_{cas}	3.73	4.23	4.73	5.23
t_{ah}	0.83	1.14	1.45	1.77
t_{wh}	3.73	4.23	4.73	5.23
t_{ds}	0.35	0.47	0.58	0.67
t_{dh}	0.37	0.45	0.53	0.61
t_{cs}	0.10	0.10	0.10	0.10
t_{ch}	1.00	1.12	1.23	1.35
t_{wen}	2.44	2.74	3.04	3.34
t_{acc}	3.72	4.21	4.72	5.24
t_{da}	0.43	0.55	0.68	0.80
t_{wda}	0.10	0.10	0.10	0.10
t_{wacc}	1.00	1.12	1.24	1.35
t_{dz}	0.59	0.70	0.80	0.90
t_{zd}	0.38	0.49	0.61	0.72
t_{od}	0.62	0.74	0.86	0.98
Power (μW/MHz)				
Power_read	329.69	612.37	915.23	1238.27
Power_write	640.92	1292.73	1945.95	2600.57
Power_standby	45.34	74.44	103.65	132.98
Area (μm)				
Width	831.95	1382.72	1933.49	2484.27
Height	585.22	889.22	1193.22	1497.22

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

*** For Ymux=16** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**1024**	**2048**	**3072**	**4096**
bpw	**8**	**16**	**24**	**32**
Timing (ns)				
t_{cyc}	3.72	4.21	4.72	5.24
t_{as}	0.10	0.10	0.10	0.10
t_{cas}	3.73	4.23	4.73	5.23
t_{ah}	0.82	1.14	1.45	1.77
t_{wh}	4.84	5.34	5.84	6.34
t_{ds}	0.35	0.47	0.57	0.66
t_{dh}	0.43	0.51	0.59	0.66
t_{cs}	0.10	0.10	0.10	0.10
t_{ch}	1.00	1.12	1.23	1.35
t_{wen}	2.44	2.74	3.04	3.34
t_{acc}	3.72	4.21	4.72	5.24
t_{da}	0.43	0.56	0.68	0.80
t_{wda}	0.10	0.10	0.10	0.10
t_{wacc}	1.00	1.12	1.24	1.35
t_{dz}	0.59	0.70	0.80	0.90
t_{zd}	0.38	0.49	0.61	0.72
t_{od}	0.63	0.74	0.86	0.98
Power (μW/MHz)				
Power_read	302.32	566.11	850.30	1154.92
Power_write	604.76	1237.02	1845.18	2429.24
Power_standby	40.94	65.48	90.13	114.89
Area (μm)				
Width	831.95	1382.72	1933.49	2484.27
Height	585.22	889.22	1193.22	1497.22

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

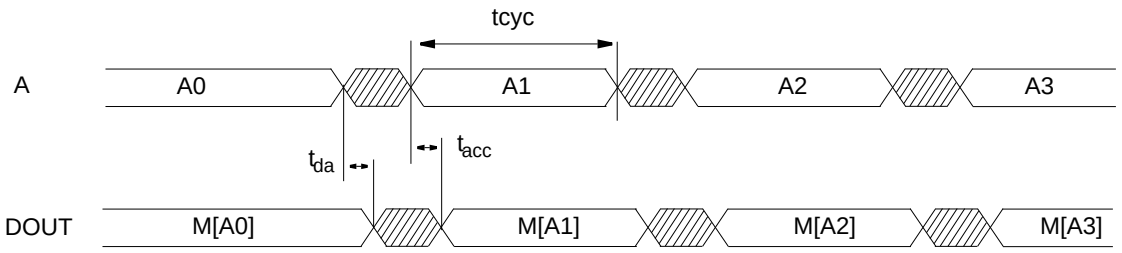
*** For Ymux=32** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**2048**	**4096**	**6144**	**8192**
bpw	**4**	**8**	**12**	**16**
Timing (ns)				
t_{cyc}	4.67	5.11	5.59	6.14
t_{as}	0.17	0.18	0.19	0.20
t_{cas}	4.79	5.45	6.15	6.92
t_{ah}	1.14	1.50	1.89	2.30
t_{wh}	4.79	5.45	6.15	6.92
t_{ds}	0.61	0.78	0.96	1.15
t_{dh}	0.54	0.65	0.77	0.89
t_{cs}	0.10	0.10	0.10	0.10
t_{ch}	1.24	1.41	1.58	1.76
t_{wen}	3.59	3.83	4.11	4.43
t_{acc}	4.67	5.11	5.59	6.14
t_{da}	0.63	0.75	0.87	0.98
t_{wda}	0.10	0.10	0.10	0.10
t_{wacc}	1.22	1.31	1.39	1.48
t_{dz}	0.91	0.99	1.07	1.15
t_{zd}	0.57	0.69	0.80	0.91
t_{od}	0.82	0.95	1.07	1.18
Power (μW/MHz)				
Power_read	281.72	539.90	818.90	1118.73
Power_write	556.29	1191.99	1793.82	2361.78
Power_standby	38.74	61.29	83.99	106.84
Area (μm)				
Width	831.95	1382.72	1933.49	2484.27
Height	585.22	889.22	1193.22	1497.22

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

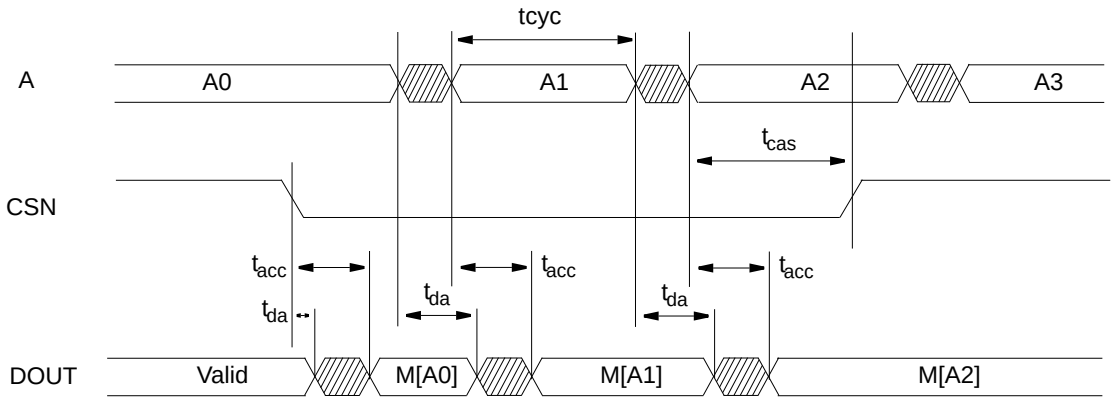
Timing Diagrams

Read Cycle



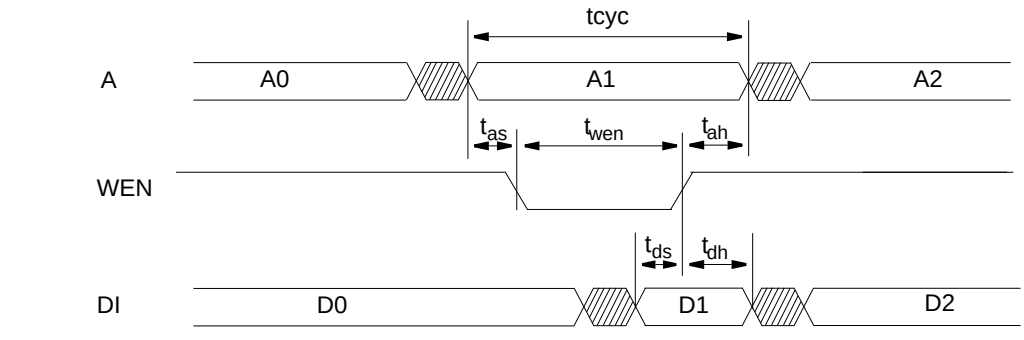
(WEN = high, CSN = low, OEN = low, DI = don't care)

Read Cycle with CSN-Controlled



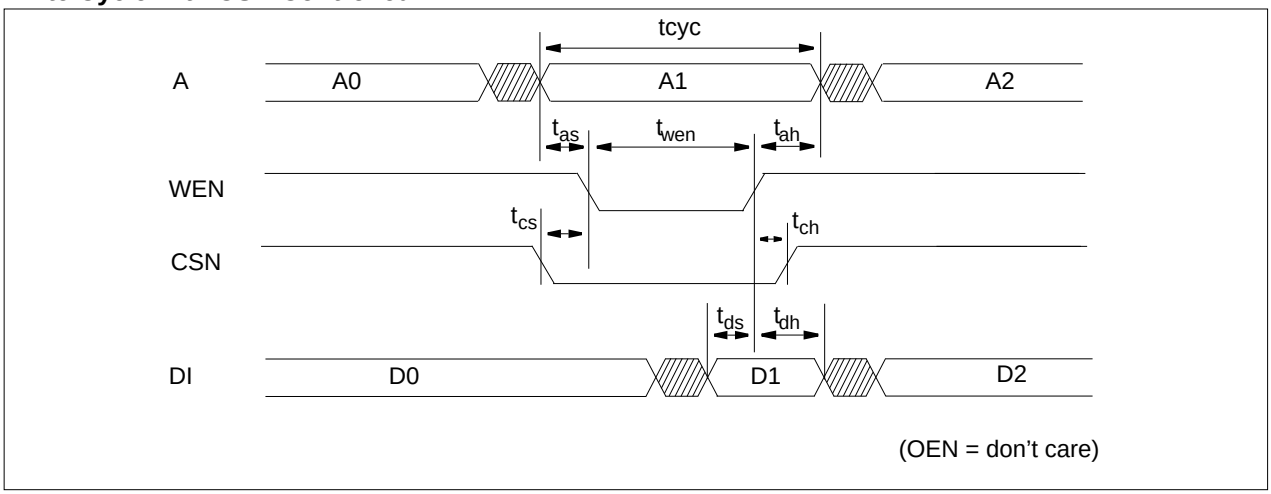
(OEN = low, WEN = high, DI = don't care)

Basic Write Cycle

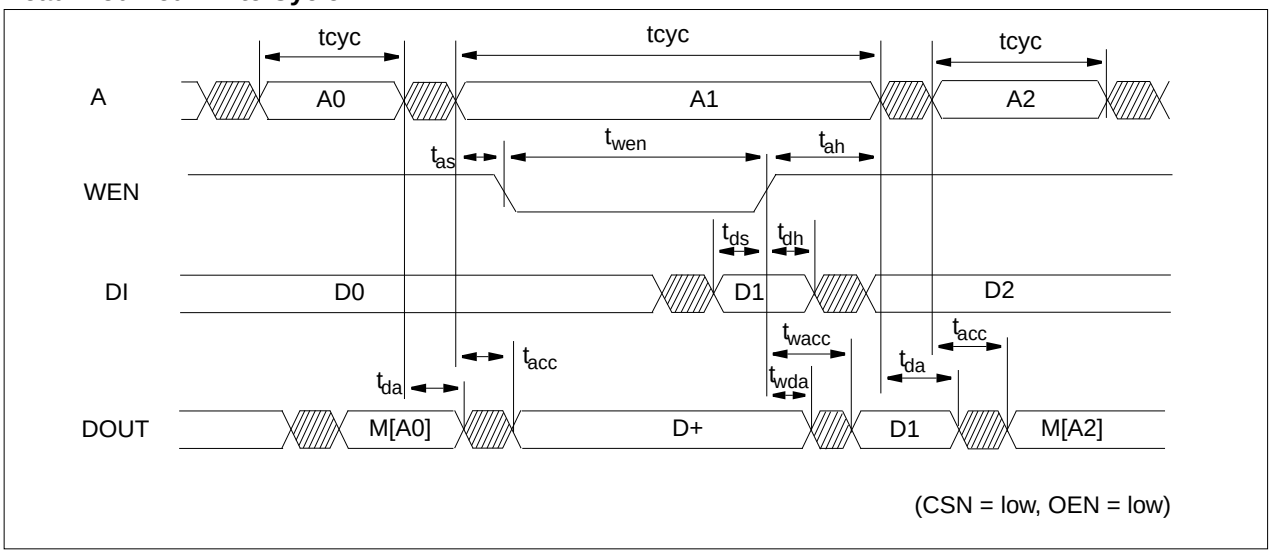


(CSN = low, OEN = don't care)

Write Cycle with CSN Controlled



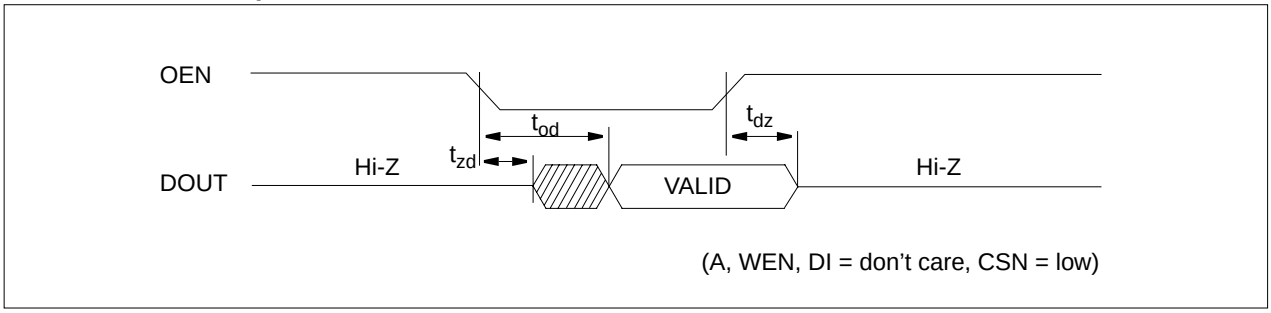
Read-Modified-Write Cycle



NOTES:

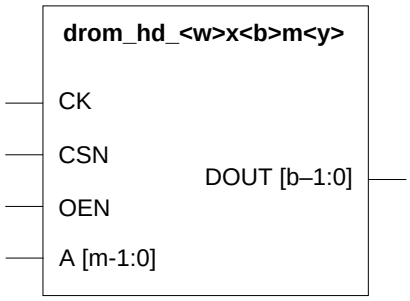
1. When the wen hold time after the last address bit transition is satisfied, D+ will toggle in response to a successful read of the initial contents of address A1. When the wen hold time after the last address bit transition is not satisfied, D+ will go to unknown state.
2. Address bits are not allowed to change while WEN is low. If they do change, then the data for one or more addresses in the memory array may be corrupted.

OEN Controlled Output Enable



NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:
1. Words (w) is the number of words in DROM_HD.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. $m = \lceil \log_2 w \rceil$

Features

- Suitable for high-density applications
- Allowable for high-speed and low-power applications
- Fully synchronous operation
- Duty-free cycle
- Positive-edge clock operation
- Diffusion-programmable
- Automatic power-down mode available
- Self-controlled circuit available
- Asynchronous tri-state output
- Low noise output optimization
- Flexible aspect ratio
- Zero standby current
- Latched inputs and outputs
- Up to 512Kbits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

DROM_HD is a synchronous diffusion programmable ROM which is provided as a compiler. DROM_HD is intended for use in high-density applications. It is also allowable for high-speed and low-power applications. The read cycle is initiated at the rising edge of CK. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] is disabled and DOUT[] remains stable. When OEN is high, DOUT is placed in a high-impedance state.

DROM Function Table

CK	CSN	OEN	A	DOUT	Comment
X	X	H	X	Z	Unconditional tri-state output
X	H	L	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	Valid	MEM(A)	Read cycle

Parameter Description

DROM_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and Column mux(y).

Parameter		Ymux(y)=8	Ymux(y)=16	Ymux(y)=32
words(w)	Min	64	128	256
	Max	4096	8192	16384
	Step	32	64	128
bpws(b)	Min	2	2	2
	Max	128	64	32
	Step	1	1	1

DROM_HD

High-Density Synchronous Diffusion Programmable ROM

Pin Descriptions

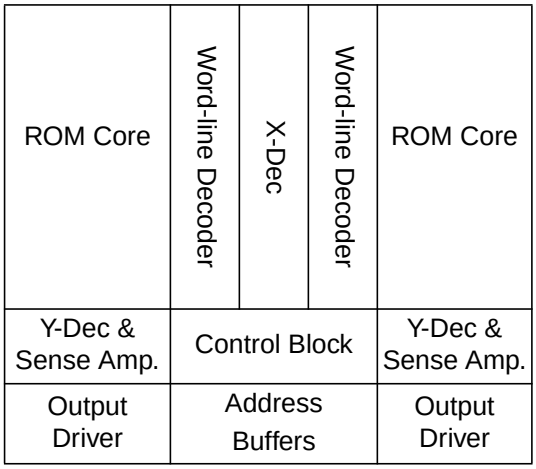
Name	I/O	Description
CK	Clock	Clock input. CSN and A[] are latched into the ROM on the rising edge of CK. If CSN is low on the rising edge of CK, the ROM is in read mode. Upon the falling edge of CK, the ROM is in a precharge state.
CSN	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the ROM on the rising edge of CK. When CSN is low, the ROM is enabled for reading. When CSN is high, the ROM goes to the standby mode and is disabled for reading. DOUT remains previous data output.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the ROM on the rising edge of CK.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the ROM is in read mode.

Pin Capacitance

(Unit = SL)

CK	CSN	OEN	A	DOUT		
				Ymux = 8	Ymux = 16	Ymux = 32
2.67	2.76	1.63	2.80	4.43	4.43	4.43

Block Diagrams



Application Notes

1. Prohibiting over-the-cell routing
In chip-level layout, over-the-cell routing in DROM_HD is not permitted because the memory characteristic may be changed when any signals are cross over DROM_HD. It may be caused the severe failure of memory operation.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DROM_HD.

4. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.

DROM_HD

High-Density Synchronous Diffusion Programmable ROM

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ch}	CSN hold time from CK rise
t_{ckl}	Clock pulse width low	t_{acc}	Data access time
t_{ckh}	Clock pulse width high	t_{da}	De-access time
t_{as}	Address setup time	t_{dz}	DOUT drive to high-Z time
t_{ah}	Address hold time	t_{zd}	DOUT high-Z to drive time
t_{cs}	CSN setup time	t_{od}	OEN to valid output
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=8** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**1024**	**2048**	**3072**	**4096**
bpw	**32**	**64**	**96**	**128**
Timing (ns)				
t_{cyc}	4.01	4.84	5.86	7.09
t_{ckl}	0.62	0.62	0.62	0.62
t_{ckh}	0.70	0.70	0.70	0.70
t_{as}	0.11	0.11	0.11	0.11
t_{ah}	0.53	0.53	0.53	0.53
t_{cs}	0.71	0.71	0.71	0.71
t_{ch}	0.48	0.48	0.48	0.47
t_{acc}	2.93	3.49	4.06	4.67
t_{da}	2.53	3.12	3.73	4.39
t_{dz}	0.54	0.64	0.74	0.84
t_{zd}	0.67	0.77	0.87	0.97
t_{od}	0.75	0.85	0.95	1.04
Power (μW/MHz)				
Power_read	445.20	711.20	911.65	1046.54
Power_standby	2.13	2.35	2.58	2.80
Area (μm)				
Width	676.07	1142.89	1609.71	2076.53
Height	381.40	573.40	765.40	957.40

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

*** For Ymux=16** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**2048**	**4096**	**6144**	**8192**
bpw	**16**	**32**	**48**	**64**
Timing (ns)				
t_{cyc}	4.02	4.84	5.86	7.09
t_{ckl}	0.62	0.62	0.62	0.62
t_{ckh}	0.70	0.70	0.70	0.70
t_{as}	0.11	0.11	0.11	0.11
t_{ah}	0.53	0.53	0.53	0.53
t_{cs}	0.71	0.71	0.71	0.71
t_{ch}	0.48	0.48	0.48	0.48
t_{acc}	2.97	3.52	4.10	4.71
t_{da}	2.54	3.13	3.74	4.40
t_{dz}	0.51	0.57	0.64	0.70
t_{zd}	0.63	0.70	0.77	0.84
t_{od}	0.71	0.78	0.85	0.91
Power (μW/MHz)				
Power_read	304.76	512.10	685.26	824.22
Power_standby	2.11	2.31	2.52	2.72
Area (μm)				
Width	675.86	1142.80	1609.75	2076.70
Height	381.40	573.40	765.40	957.40

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

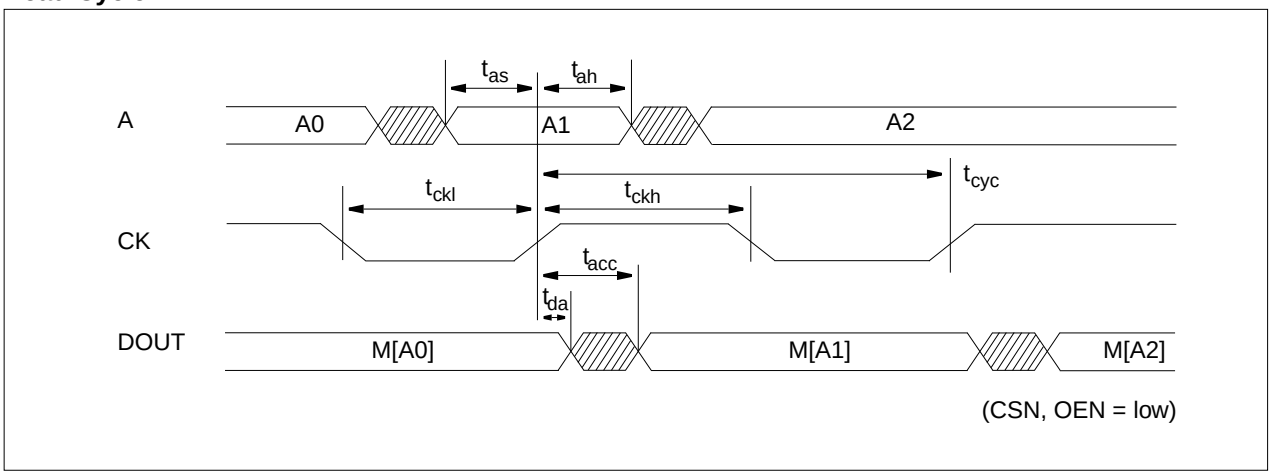
*** For Ymux=32** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**4096**	**8192**	**12288**	**16384**
bpw	**8**	**16**	**24**	**32**
Timing (ns)				
t_{cyc}	4.02	4.82	5.84	7.07
t_{ckl}	0.62	0.62	0.62	0.62
t_{ckh}	0.70	0.70	0.70	0.70
t_{as}	0.10	0.10	0.10	0.10
t_{ah}	0.53	0.53	0.53	0.53
t_{cs}	0.71	0.71	0.71	0.71
t_{ch}	0.48	0.48	0.48	0.48
t_{acc}	3.06	3.60	4.18	4.79
t_{da}	2.56	3.14	3.76	4.41
t_{dz}	0.49	0.54	0.59	0.64
t_{zd}	0.62	0.67	0.72	0.77
t_{od}	0.69	0.74	0.80	0.84
Power (μW/MHz)				
Power_read	260.49	441.28	603.48	747.07
Power_standby	2.10	2.29	2.49	2.69
Area (μm)				
Width	673.61	1141.72	1609.83	2077.94
Height	381.40	573.40	765.40	957.40

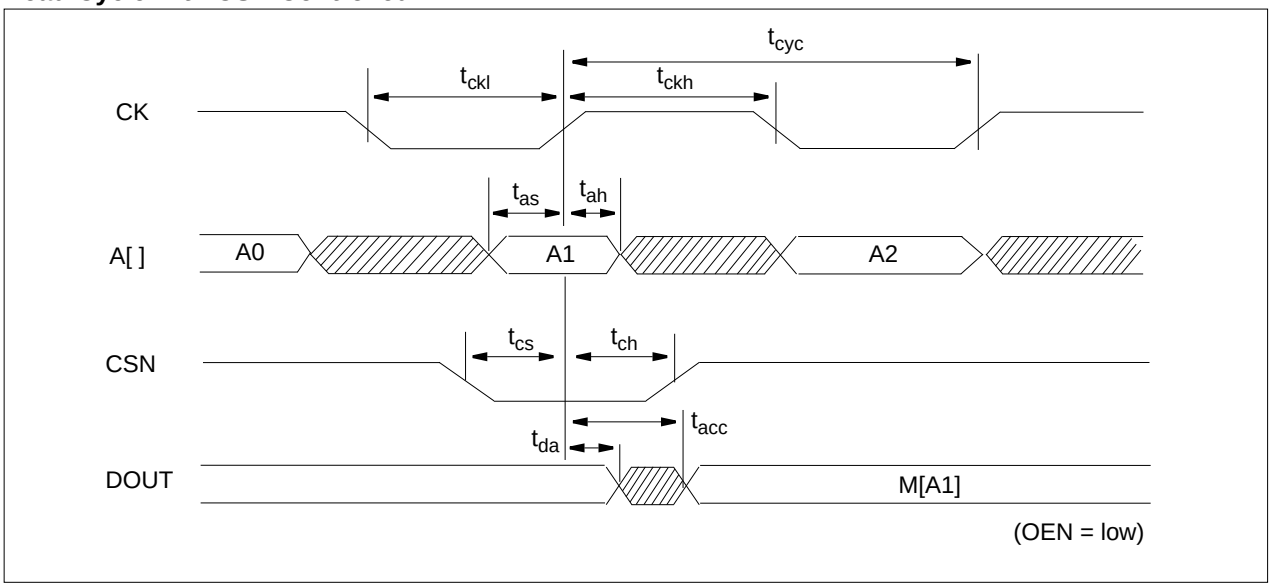
NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Timing Diagrams

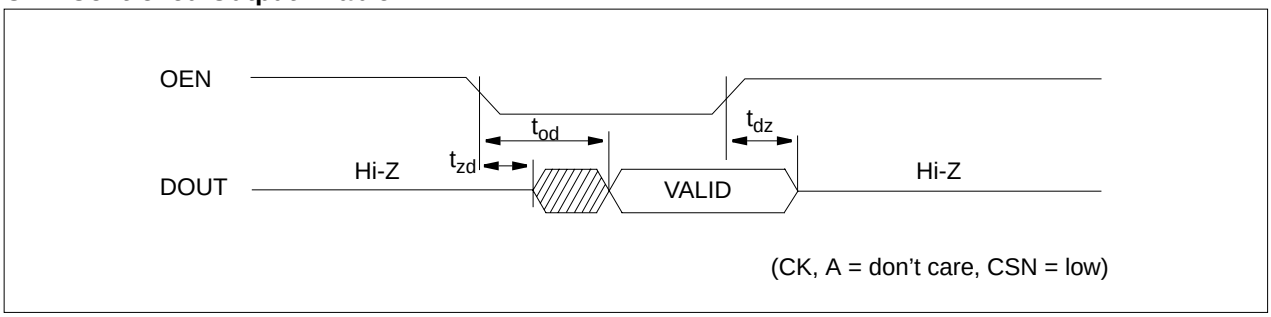
Read Cycle



Read Cycle with CSN Controlled

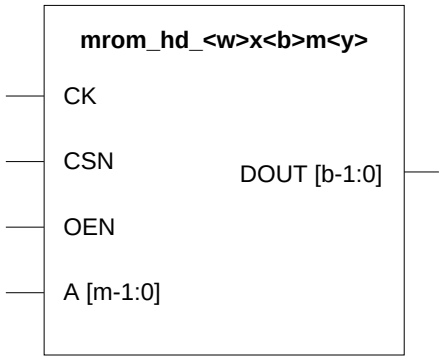


OEN Controlled Output Enable



NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:
1. Words (w) is the number of words in MROM_HD.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density applications
- Allowable for high-speed and low-power applications
- Fully synchronous operation
- Duty-free cycle
- Positive-edge clock operation
- Metal-2 programmable
- Automatic power-down mode available
- Self-controlled circuit available
- Asynchronous tri-state output
- Low noise output optimization
- Flexible aspect ratio
- Zero standby current
- Latched inputs and outputs
- Up to 512Kbits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

MROM_HD is a synchronous metal-2 programmable ROM which is provided as a compiler. MROM_HD is intended for use in high-density applications. It is also allowable for high-speed and low-power applications. The read cycle is initiated at the rising edge of CK. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] is disabled and DOUT[] remains stable. When OEN is high, DOUT is placed in a high-impedance state.

MROM Function Table

CK	CSN	OEN	A	DOUT	Comment
X	X	H	X	Z	Unconditional tri-state output
X	H	L	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	Valid	MEM(A)	Read cycle

Parameter Description

MROM_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and Column mux(y).

Parameters		Ymux = 8	Ymux = 16	Ymux = 32
Words (w)	Min	64	128	256
	Max	4096	8192	16384
	Step	32	64	128
Bpw (b)	Min	2	2	2
	Max	128	64	32
	Step	1	1	1

Pin Descriptions

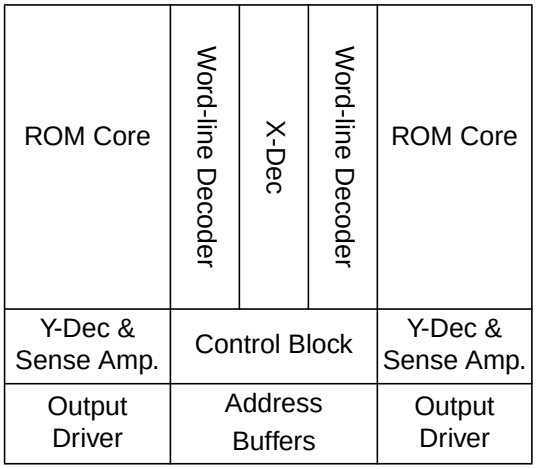
Name	I/O	Description
CK	Clock	Clock input. CSN and A[] are latched into the ROM on the rising edge of CK. If CSN is low on the rising edge of CK, the ROM is in read mode. Upon the falling edge of CK, the ROM is in a precharge state.
CSN	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the ROM on the rising edge of CK. When CSN is low, the ROM is enabled for reading. When CSN is high, the ROM goes to the standby mode and is disabled for reading. DOUT remains previous data output.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the ROM on the rising edge of CK.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the ROM is in read mode.

Pin Capacitance

(Unit = SL)

CK	CSN	OEN	A	DOUT		
				Ymux = 8	Ymux = 16	Ymux = 32
2.54	2.75	1.58	2.79	4.59	4.59	4.59

Block Diagrams



Application Notes

1. Prohibiting over-the-cell routing
In chip-level layout, over-the-cell routing in MROM_HD is not permitted because the memory characteristic may be changed when any signals are cross over MROM_HD. It may be caused the severe failure of memory operation.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of MROM_HD.

4. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ch}	CSN hold time from CK rise
t_{ckl}	Clock pulse width low	t_{acc}	Data access time
t_{ckh}	Clock pulse width high	t_{da}	De-access time
t_{as}	Address setup time	t_{dz}	DOUT drive to high-Z time
t_{ah}	Address hold time	t_{zd}	DOUT high-Z to drive time
t_{cs}	CSN setup time	t_{od}	OEN to valid output
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=8** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**1024**	**2048**	**3072**	**4096**
bpw	**32**	**64**	**96**	**128**
Timing (ns)				
t_{cyc}	4.85	6.33	8.13	10.25
t_{ckl}	0.62	0.62	0.62	0.62
t_{ckh}	0.70	0.70	0.70	0.70
t_{as}	0.12	0.12	0.12	0.13
t_{ah}	0.53	0.53	0.53	0.53
t_{cs}	0.71	0.71	0.71	0.71
t_{ch}	0.48	0.48	0.48	0.48
t_{acc}	3.20	4.16	5.22	6.41
t_{da}	2.89	3.91	4.96	6.06
t_{dz}	0.56	0.68	0.80	0.91
t_{zd}	0.69	0.82	0.94	1.05
t_{od}	0.77	0.89	1.01	1.13
Power (μW/MHz)				
Power_read	654.81	1003.38	1277.72	1477.84
Power_standby	2.13	2.35	2.57	2.80
Area (μm)				
Width	781.47	1419.98	2058.48	2696.99
Height	559.33	940.13	1320.93	1701.73

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

*** For Ymux=16** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**2048**	**4096**	**6144**	**8192**
bpw	**16**	**32**	**48**	**64**
Timing (ns)				
t_{cyc}	4.85	6.32	8.13	10.25
t_{ckl}	0.62	0.62	0.62	0.62
t_{ckh}	0.70	0.70	0.70	0.70
t_{as}	0.12	0.12	0.12	0.13
t_{ah}	0.53	0.53	0.53	0.53
t_{cs}	0.71	0.71	0.71	0.71
t_{ch}	0.48	0.48	0.48	0.47
t_{acc}	3.24	4.19	5.26	6.45
t_{da}	2.90	3.92	4.97	6.07
t_{dz}	0.52	0.60	0.67	0.74
t_{zd}	0.64	0.72	0.80	0.88
t_{od}	0.72	0.80	0.88	0.96
Power (μW/MHz)				
Power_read	447.32	708.77	937.27	1132.83
Power_standby	2.11	2.31	2.52	2.72
Area (μm)				
Width	781.18	1419.86	2058.54	2697.22
Height	559.33	940.13	1320.93	1701.73

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

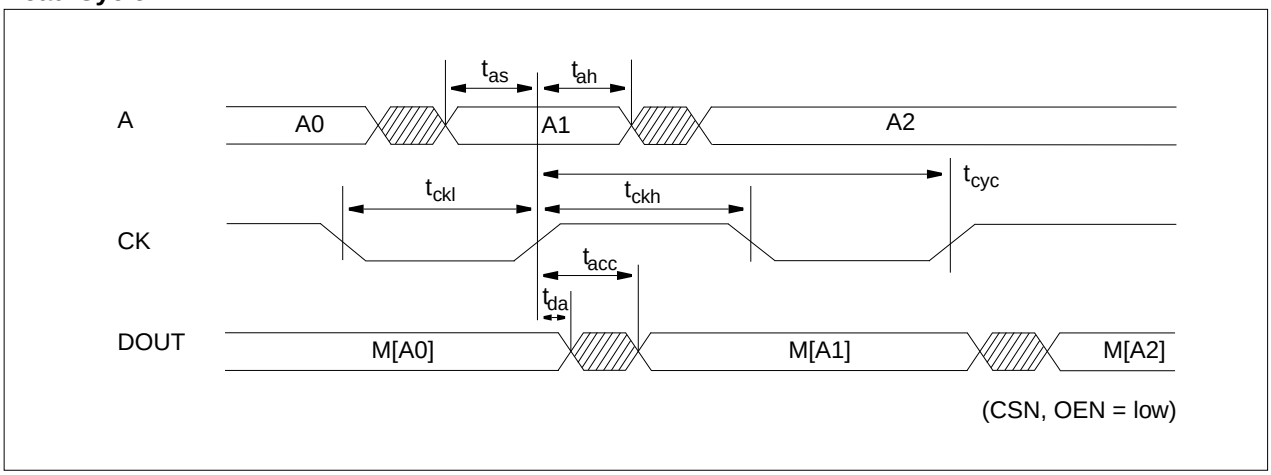
*** For Ymux=32** (Typical process, 3.3V, 25°C, Output load = 10SL, Input slope = 0.2ns, SA=0.5)

Parameters				
words	**4096**	**8192**	**12288**	**16384**
bpw	**8**	**16**	**24**	**32**
Timing (ns)				
t_{cyc}	4.85	6.30	8.09	10.24
t_{ckl}	0.62	0.62	0.62	0.62
t_{ckh}	0.70	0.70	0.70	0.70
t_{as}	0.12	0.12	0.12	0.13
t_{ah}	0.53	0.53	0.53	0.53
t_{cs}	0.71	0.71	0.71	0.71
t_{ch}	0.48	0.48	0.48	0.48
t_{acc}	3.32	4.27	5.34	6.53
t_{da}	2.92	3.93	4.99	6.10
t_{dz}	0.49	0.55	0.60	0.66
t_{zd}	0.62	0.68	0.74	0.79
t_{od}	0.70	0.76	0.82	0.87
Power (μW/MHz)				
Power_read	287.06	508.74	718.25	915.58
Power_standby	2.10	2.29	2.48	2.67
Area (μm)				
Width	778.19	1418.42	2058.65	2698.88
Height	559.33	940.13	1320.93	1701.73

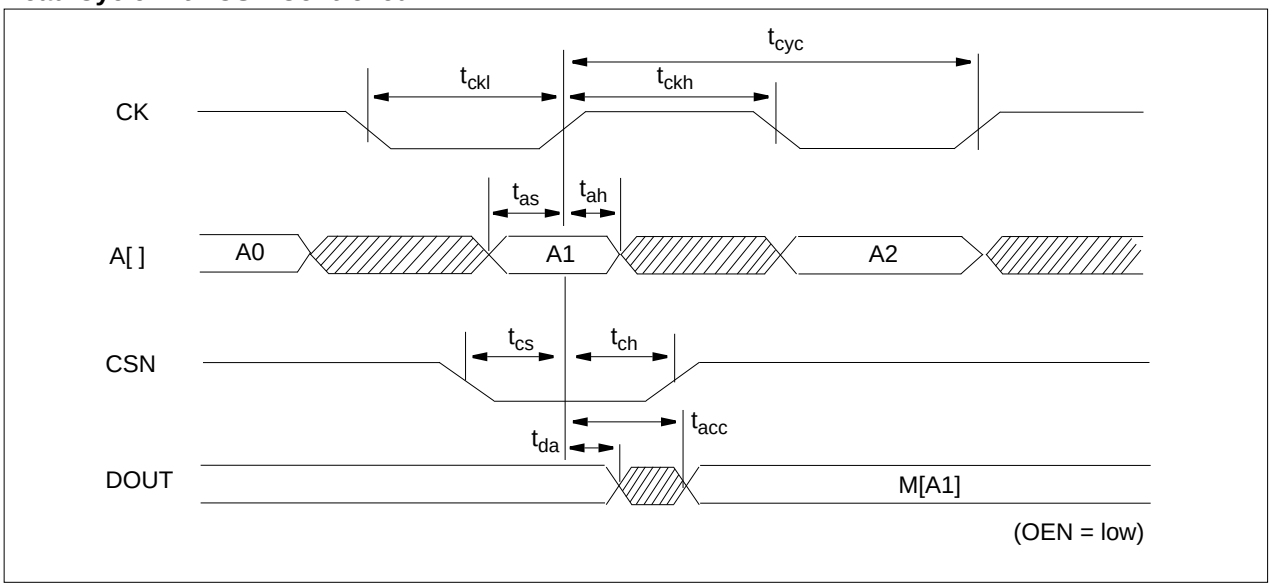
NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

Timing Diagrams

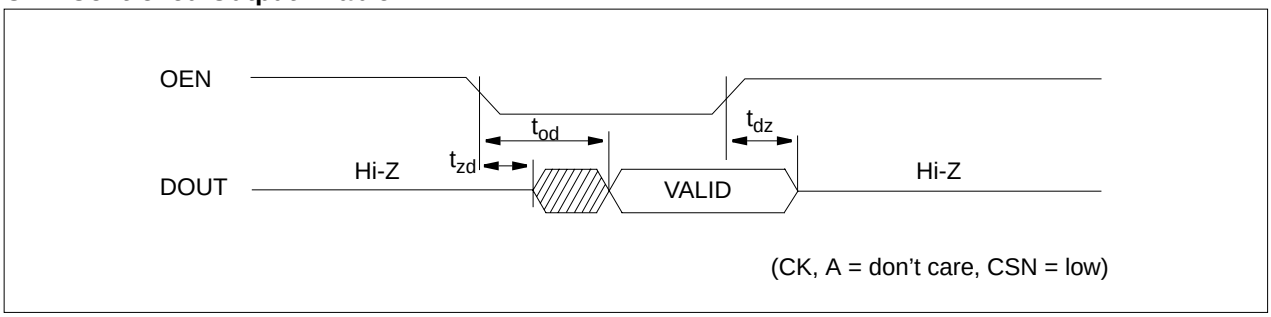
Read Cycle



Read Cycle with CSN Controlled



OEN Controlled Output Enable



NOTE: "don't care" means the condition that these pins are in normal operation mode.

COMPILED DATAPATH MACRO CELLS

Datapath macro cell is a set of n-bit data operators that enables more efficient datapath module design and implementation. Compiled datapath macro cell creates area-, speed- and power-optimized adders, subtracters, ALUs, barrel shifters, multipliers, and register files based on the user specified parameters. It creates a functional model, a timing information for simulation, and a verified hard macro layout.

The followings are the summaries of main features of compiled datapath macro cells:

Advanced Design Technique

All of STD90/MDL90 compiled datapath macro cells adopt very advanced design techniques to get optimized performances on the given parameters. Some of those design techniques are as follows

- Hierarchical double carry select scheme to reduce carry-chain delay
- Transmission gate multiplexing for data shifting
- Allowing pipeline insertion in multiplication
- Allowing over-the-cell routing
- Dense datapath module layout generation with topological regularity.

Flexible Datapath Macrocell Design Flow

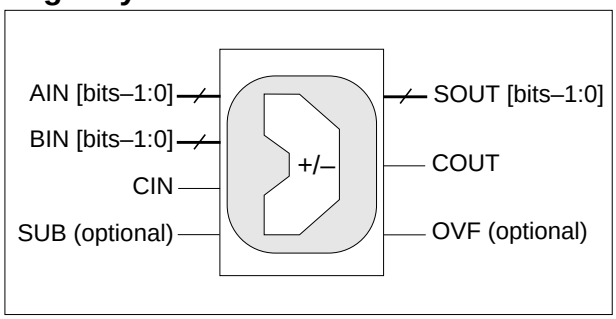
The implementation of datapath module is one of the most critical and important elements in the design of high performance systems; DSPs, multimedia, graphics, microprocessors and so on. In these systems, the datapath modules are used much more than other designs and at the same time, datapath module affects the overall design performances.

The macrocell generation flow is tightly integrated into Apollo, Avant! which is used as a main tool at a full chip layout step. By supporting an easy-to-use ASIC environment, achieving full custom-like density, performance, ASIC designers can expect improving productivity. In the design of datapath macro cell, the optimal module placement of leafcell is a key point to take advantage of inherent regularity in datapaths. An optimal datapath module placement can maximize density and minimize speed, bus line skew, power consumption and turn-around time in ASIC design.

SELECTION GUIDE FOR COMPILED DATAPATH MACROCELLS

Cell Name	Description
ADDER	4-to-64 bit addition/subtraction - Ripple-carry/group-bypass carry scheme - 2's Complement overflow
ALU	4-to-64 bit arithmetic logic unit - 9 arithmetic and 15 logical operations - 2's complement overflow
BS	4-to-64 bit barrel shifter - Transmission gate multiplexing scheme - Bi-directional shift or rotation - Fill for vacant bits with data
CSADDER	4-to-64 bit carry select adder - Double carry select scheme - 2's Complement overflow
BMPY	6-to-64 bit modified booth multiplier - 2's complement multiplication - Accumulation scheme - Pipelined architecture scheme
REGF	Multi-port asynchronous register file - 1-to-4 read and 1-to-2 write scheme - Fully asynchronous read, CLK synchronized write

Logic Symbol



Features

- *n*-bit (4 to 64) adder/subtracter
- Two's complement or unsigned magnitude operation
- Functional model, schematic and layout generators
- Timing model with auto-characterization
- Simple ripple and sophisticated group bypass scheme
- Two's complement overflow flag
- Three drive strength options for output

Function Description

The adder builds an *n*-bit wide adder/subtracter schematic.

The adder performs two's complement addition/subtraction or unsigned magnitude addition. The overflow flag gets set if an overflow occurs while adding two positive or negative numbers. The overflow is ignored while doing unsigned magnitude operations.

The adder/subtracter can be built with two different carry chains allowing speed/area trade-offs. The ripple carry chain is high in density, but low in performance. The group-bypass chain has a unique grouping of bits which creates a high performance design. This scheme is preferable for the addition of large data bits to attain high speed.

Function Table

Type	Function
Adder	SOUT = AIN + BIN + CIN (cinlogic=1), SOUT = AIN + BIN + ~CIN (cinlogic=0)
Subtracter	SOUT = AIN + ~BIN + CIN (cinlogic=1), SOUT = AIN + ~BIN + ~CIN (cinlogic=0)
Overflow	(~SOUT [bits–1]) • (AIN [bits–1] • BIN [bits–1]) + (SOUT [bits–1]) • (~AIN [bits–1]) •(~ BIN [bits–1])

Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits for the input data bus	4 to 64
nopass	0: group bypass; 1: ripple adder	0/1
subtract	0: adder only; 1: adder/subtracter	0/1
cinlogic	0: CIN ← ~CIN; 1: CIN ← CIN	0/1
overflow	Overflow flag for signed operation	0/1
drv	Drive strength	1/2/4

ADDER

Adder/Subtracter

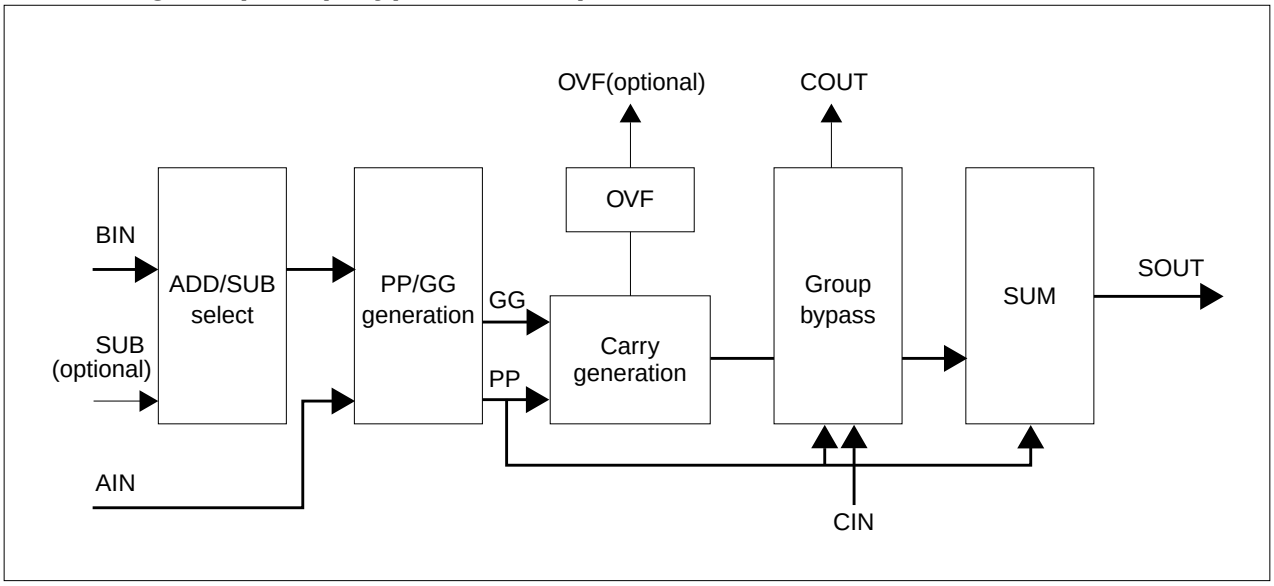
Pin Description

Name	I/O	Description
AIN [bits–1:0]	I	Data input
BIN [bits–1:0]		Data input
CIN		Carry-in
SUB		It specifies addition/subtraction (optional when the parameter subtract = 1).
SOUT[bits–1:0]	O	Result of addition/subtraction
COUT		Carry-out
OVF		Overflow/underflow of addition/subtraction (optional when the parameter overflow = 1)

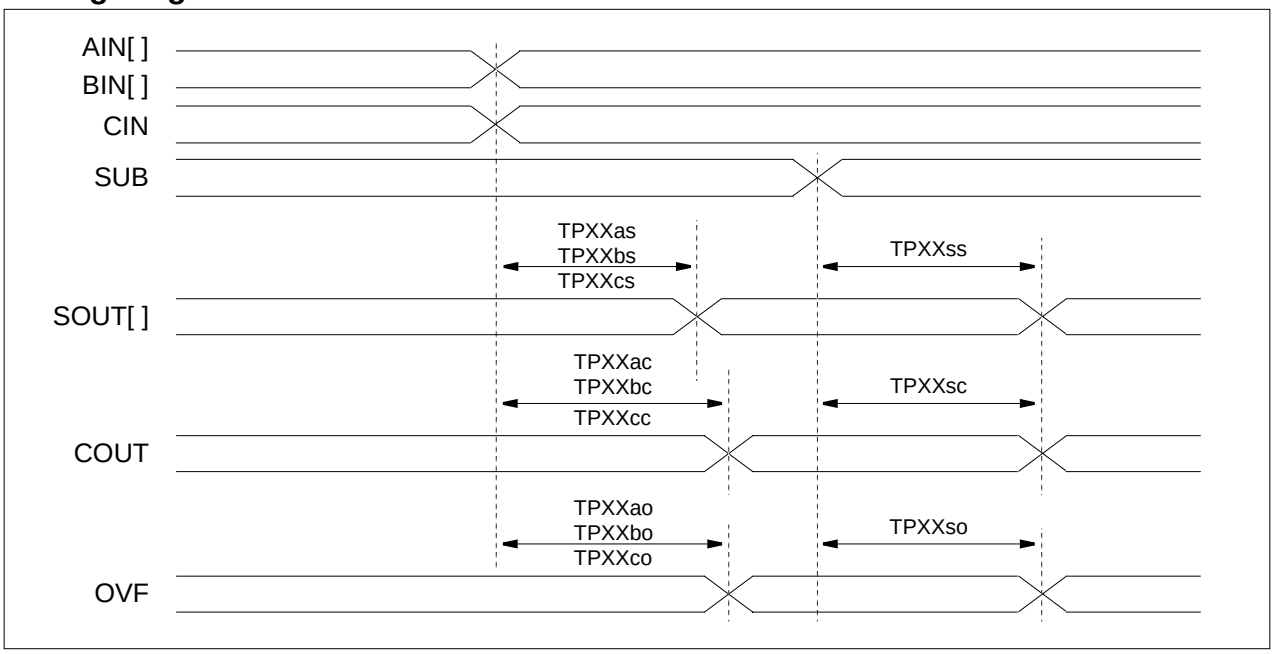
Pin Capacitance [Unit: pF]

Name	Case	Value
AIN	all	0.026
BIN	sub = 0 sub = 1	0.024 0.019
CIN	nopass = 0 nopass = 1, cinlogic = 0 nopass = 1, cinlogic = 1	0.051 0.058 0.061
SUB	sub = 1	0.018 * bits

Block Diagram (Group Bypass Schem)



Timing Diagram



Timing Type Definition

Timing Type	Definition
TPXXas	Propagation delay, TPLH/TPHL, from input AIN to output SOUT
TPXXbs	Propagation delay, TPLH/TPHL, from input BIN to output SOUT
TPXXcs	Propagation delay, TPLH/TPHL, from input CIN to output SOUT
TPXXss	Propagation delay, TPLH/TPHL, from input SUB to output SOUT
TPXXac	Propagation delay, TPLH/TPHL, from input AIN to output COUT
TPXXbc	Propagation delay, TPLH/TPHL, from input BIN to output COUT
TPXXcc	Propagation delay, TPLH/TPHL, from input CIN to output COUT
TPXXsc	Propagation delay, TPLH/TPHL, from input SUB to output COUT
TPXXao	Propagation delay, TPLH/TPHL, from input AIN to output OVF
TPXXbo	Propagation delay, TPLH/TPHL, from input BIN to output OVF
TPXXco	Propagation delay, TPLH/TPHL, from input CIN to output OVF
TPXXso	Propagation delay, TPLH/TPHL, from input SUB to output OVF

ADDER

Adder/Subtracter

Characteristic Reference Table

Symbol	Description	Unit	Symbol	Description	Unit
T	Junction temperature	°C	S	Input slope	ns
V_{DD}	Power supply voltage	V	SL	Standard load	-
C_L	Output load	SL	SA	Input switching activity	-

1) Timing Characteristics [Unit: ns]

(Typical process, T=25, V_{DD}=3.3, C_L=10, S=0.2, SA=0.5)

Type	8	24	36	48	64
Case: subtract=0, nopass=0, overflow=1, cinlogic=1					
TPHLac/TPLHac	0.81 / 1.06	1.22 / 1.46	1.48 / 1.72	1.69 / 1.92	1.91 / 2.13
TPHLbc/TPLHbc	0.90 / 1.11	1.31 / 1.52	1.57 / 1.77	1.78 / 1.98	2.00 / 2.18
TPHLcc/TPLHcc	0.47 / 0.48	0.88 / 0.88	1.13 / 1.14	1.35 / 1.36	1.57 / 1.58
TPHLao/TPLHao	1.35 / 1.21	1.76 / 1.63	2.03 / 1.90	2.25 / 2.12	2.49 / 2.36
TPHLbo/TPLHbo	1.40 / 1.30	1.82 / 1.72	2.08 / 1.99	2.31 / 2.21	2.54 / 2.45
TPHLco/TPLHco	0.76 / 0.87	1.18 / 1.29	1.45 / 1.56	1.69 / 1.78	1.93 / 2.02
TPHLas/TPLHas	1.44 / 1.32	1.85 / 1.73	2.11 / 1.99	2.33 / 2.21	2.55 / 2.42
TPHLbs/TPLHbs	1.49 / 1.41	1.90 / 1.82	2.16 / 2.08	2.38 / 2.30	2.60 / 2.51
TPHLcs/TPLHcs	0.85 / 0.98	1.27 / 1.39	1.54 / 1.65	1.76 / 1.86	2.00 / 2.08
Case: subtract=0, nopass=1, overflow=1, cinlogic=1					
TPHLac/TPLHac	1.24 / 1.35	3.03 / 3.20	4.36 / 4.58	5.67 / 5.95	7.41 / 7.75
TPHLbc/TPLHbc	1.27 / 1.39	3.06 / 3.25	4.39 / 4.63	5.70 / 6.00	7.44 / 7.80
TPHLcc/TPLHcc	1.09 / 1.14	2.88 / 3.00	4.21 / 4.38	5.53 / 5.74	7.26 / 7.54
TPHLao/TPLHao	1.37 / 1.37	3.24 / 3.17	4.63 / 4.49	5.99 / 5.80	7.78 / 7.52
TPHLbo/TPLHbo	1.42 / 1.40	3.29 / 3.19	4.67 / 4.52	6.04 / 5.84	7.83 / 7.56
TPHLco/TPLHco	1.16 / 1.22	3.03 / 3.02	4.41 / 4.35	5.78 / 5.66	7.57 / 7.39
TPHLas/TPLHas	1.39 / 1.38	3.26 / 3.17	4.64 / 4.50	6.00 / 5.81	7.79 / 7.54
TPHLbs/TPLHbs	1.44 / 1.40	3.31 / 3.20	4.69 / 4.53	6.05 / 5.84	7.84 / 7.57
TPHLcs/TPLHcs	1.18 / 1.23	3.05 / 3.02	4.43 / 4.35	5.80 / 5.67	7.59 / 7.39

Characteristic Reference Table (Continued)

2) Power Characteristics [Unit: μW/MHz]

(Typical process, T=25, V_{DD}=3.3, C_L=10, S=0.2, SA=0.5)

Case	8	24	36	48	64
subtract=0, nopass=0, cinlogic=1, overflow=1	19.32	56.95	82.59	106.00	133.76
subtract=0, nopass=1, cinlogic=1, overflow=1	15.74	45.35	65.98	85.24	108.80
subtract=1, nopass=0, cinlogic=1, overflow=1	21.10	62.22	92.14	121.27	158.87
subtract=1, nopass=1, cinlogic=1, overflow=1	17.66	55.70	83.71	111.29	147.36

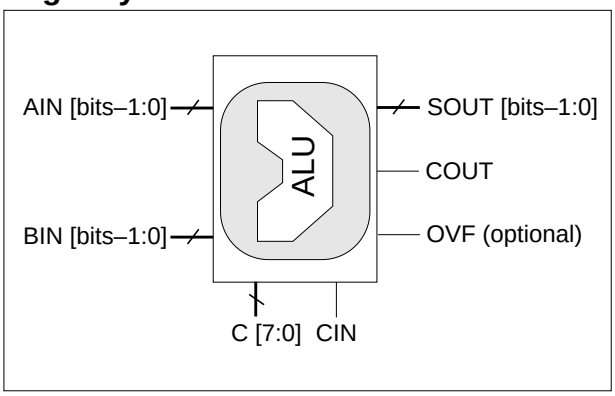
3) Size Variation [Unit: μm]

Type	Case	8	24	36	48	64
Width	subtract=0, nopass=0	72.56	72.47	72.36	72.22	71.96
	subtract=0, nopass=1	57.40	57.40	57.40	57.40	57.40
	subtract=1, nopass=0	81.66	81.57	81.46	81.32	81.06
	subtract=1, nopass=1	66.50	66.50	66.50	66.50	66.50
Height	subtract=0	117.20	347.60	520.40	693.20	923.60
	subtract=1	131.60	362.00	534.80	707.60	938.00

ALU

Arithmetic Logic Unit

Logic Symbol



Features

- *n*-bit (4 to 64) adder used
- Functional model, schematic and layout generators
- Timing model with auto-characterization
- High performance arithmetic logic unit
- Two's complement overflow flag
- Carry-out flag
- Three drive strength options for output

Function Description

The ALU builds an *n*-bit wide arithmetic logic unit schematic.
The logic circuit produced by the generator performs 15 logical and 9 arithmetic operations.

The arithmetic logic unit is built with a group-bypass carry chain. The group-bypass chain has a unique grouping of bits which creates a high performance design.

The overflow flag gets set if an overflow occurs while adding two positive or negative numbers.

Function Table

Logical	Opcode	Arithmetic	Opcode
0	0x00	AIN + BIN + CIN	0x76
~AIN & ~BIN	0x01	AIN + ~BIN + CIN	0xb9
~AIN & BIN	0x02	BIN + ~AIN + CIN	0xd9
~AIN	0x03	~AIN + CIN	0xf3
AIN & ~BIN	0x04	~BIN + CIN	0xf5
~BIN	0x05	AIN + CIN	0xfc
AIN ^ BIN	0x06	BIN + CIN	0xfa
~AIN | ~BIN	0x07	AIN – ~CIN	0x33
AIN & BIN	0x08	BIN – ~CIN	0x55
~(AIN ^ BIN)	0x09	• ~ : 1's complement • & : bit wise AND operation • | : bit wise OR operation • ^ : bit wise XOR operation	
BIN	0x0a		
~AIN | BIN	0x0b		
AIN	0x0c		
AIN | ~BIN	0x0d		
AIN | BIN	0x0e		

NOTE: While the ALU is not in active, it is preferable to keep opcode to "0x00".

Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits for the input data bus	4 to 64
overflow	Overflow flag for signed operation	0/1
drv	Drive strength	1/2/4

Pin Description

Name	I/O	Description
AIN [bits–1:0]	I	Data input for arithmetic/logical operations
BIN [bits–1:0]		Data input for arithmetic/logical operations
C [7:0]		Operational code control inputs Refer to “opcode” in the function table above.
CIN		Carry-in for arithmetic operations It must be maintained to ‘0’ in a logical operation.
SOUT [bits–1:0]	O	Result of an arithmetic/logical operation
COUT		Carry-out of an arithmetic operation
OVF		Overflow/underflow of a signed operation (optional when the parameter overflow = 1)

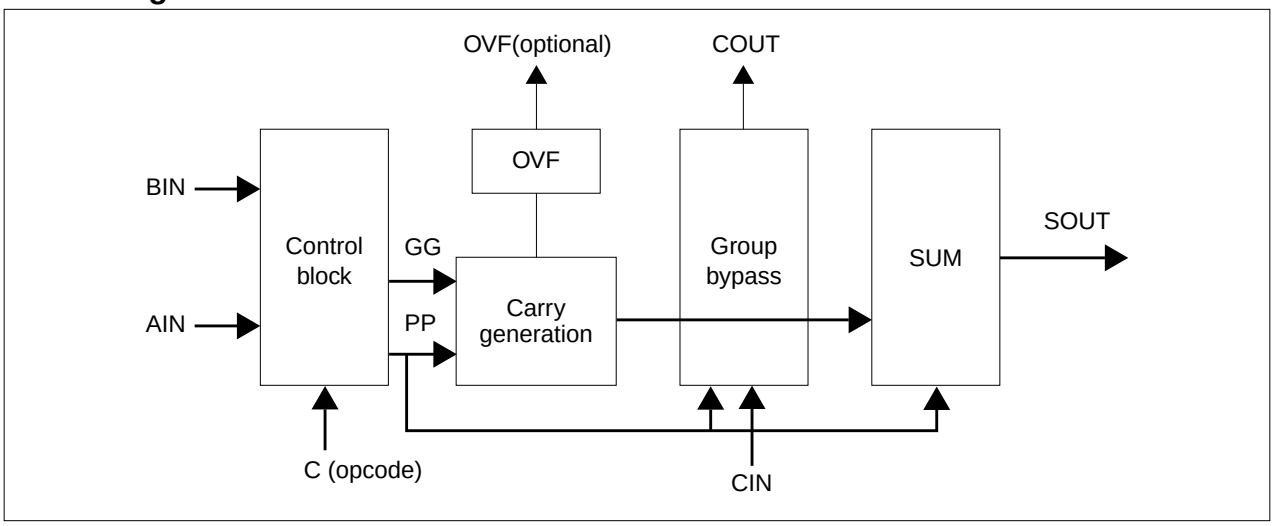
Pin Capacitance [Unit: pF]

Name	Value
AIN	0.026
BIN	0.046
CIN	0.048
C	0.025*bits + 0.026

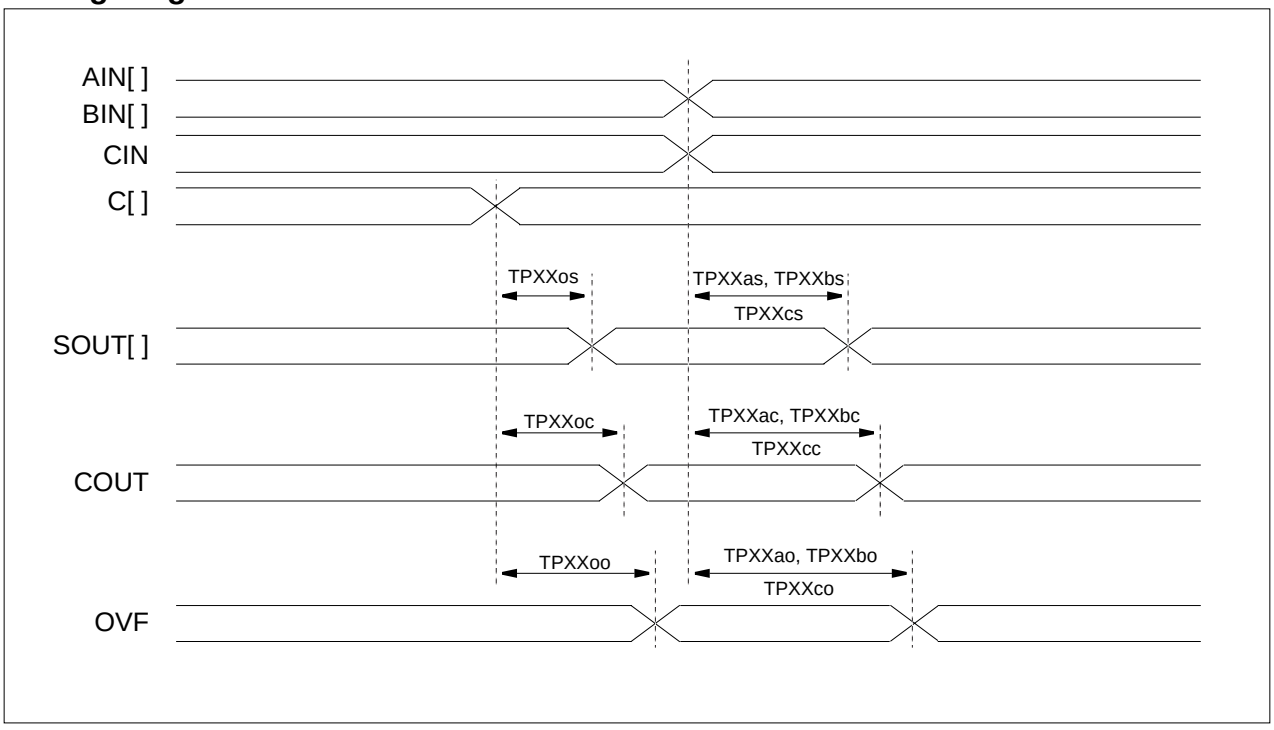
ALU

Arithmetic Logic Unit

Block Diagram



Timing Diagram



Timing Type Definition

Timing Type	Definition
TPXXas	Propagation delay, TPLH/TPHL, from input AIN to output SOUT
TPXXbs	Propagation delay, TPLH/TPHL, from input BIN to output SOUT
TPXXcs	Propagation delay, TPLH/TPHL, from input CIN to output SOUT
TPXXos	Propagation delay, TPLH/TPHL, from input C to output SOUT
TPXXac	Propagation delay, TPLH/TPHL, from input AIN to output COUT
TPXXbc	Propagation delay, TPLH/TPHL, from input BIN to output COUT

Characteristic Reference Tables

Symbol	Description	Unit	Symbol	Description	Unit
T	Junction temperature	°C	S	Input slope	ns
V_{DD}	Power supply voltage	V	SL	Standard load	-
C_L	Output load	SL	SA	Input switching activity	-

1) Timing Characteristics [Unit: ns]

(Typical process, T=25, V_{DD}=3.3, C_L=10, S=0.2, SA=0.5)

Type	8	24	36	48	64
Case: overflow=1, drv=1					
TPHLac/TPLHac	0.86 / 1.12	1.30 / 1.57	1.56 / 1.84	1.78 / 2.04	1.98 / 2.23
TPHLbc/TPLHbc	0.90 / 1.18	1.33 / 1.63	1.60 / 1.89	1.81 / 2.10	2.01 / 2.28
TPHLcc/TPLHcc	0.86 / 0.82	1.31 / 1.27	1.57 / 1.54	1.78 / 1.74	1.97 / 1.93
TPHLoc/TPLHoc	0.44 / 0.45	0.87 / 0.89	1.14 / 1.15	1.36 / 1.37	1.56 / 1.57
TPHLao/TPLHao	1.46 / 1.30	1.87 / 1.71	2.13 / 1.98	2.36 / 2.20	2.60 / 2.44
TPHLbo/TPLHbo	1.51 / 1.33	1.93 / 1.75	2.19 / 2.01	2.41 / 2.23	2.65 / 2.47
TPHLco/TPLHco	1.13 / 1.08	1.13 / 1.01	1.13 / 0.95	1.13 / 0.89	1.13 / 0.82
TPHLoo/TPLHoo	0.78 / 0.87	1.19 / 1.29	1.45 / 1.56	1.68 / 1.78	1.94 / 2.02
TPHLas/TPLHas	1.54 / 1.38	1.96 / 1.81	2.22 / 2.07	2.44 / 2.29	2.66 / 2.50
TPHLbs/TPLHbs	1.59 / 1.41	2.01 / 1.84	2.27 / 2.11	2.49 / 2.32	2.71 / 2.53
TPHLcs/TPLHcs	1.23 / 1.37	1.66 / 1.82	1.92 / 2.08	2.14 / 2.29	2.36 / 2.48
TPHLos/TPLHos	0.86 / 0.95	1.27 / 1.39	1.53 / 1.65	1.76 / 1.86	2.00 / 2.07

2) Power Characteristics [Unit: μW/MHz]

(Typical process, T=25, V_{DD}=3.3, C_L=10, S=0.2, SA=0.5)

Case	8	24	36	48	64
overflow=0	14.96	41.15	60.61	79.91	105.38
overflow=1	14.98	41.17	60.63	79.93	105.41

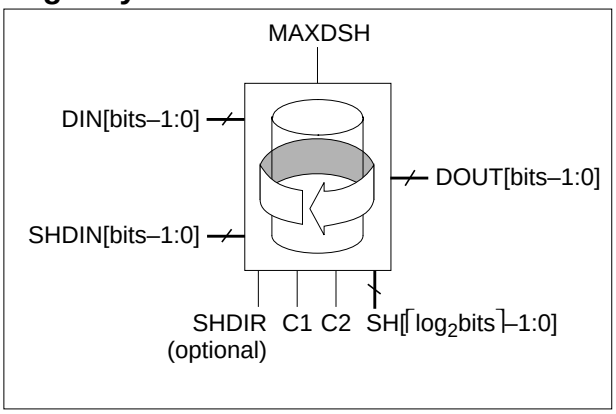
3) Size Variation [Unit: μm]

Type	8	24	36	48	64
Width	106.80	106.80	106.80	106.80	106.80
Height	117.20	347.60	520.40	693.20	923.60

BS

Barrel Shifter

Logic Symbol



Features

- *n*-bit (4 to 64) shifter
- Functional model, schematic and layout generators
- Timing model with auto-characterization
- High performance barrel shifter
- Transmission gate multiplexing scheme
- Bi-directional shift, fill vacant bits with data, or rotates
- Three drive strength options for output

Function Description

The barrel shifter builds an n-bit wide barrel shifter schematic. The barrel shifter can shift and rotate input signals in either direction. The direction of the shift can be chosen between MSB(LEFT) and LSB(RIGHT) of the bit string. The barrel shifter supports both arithmetic and logical shift operations.

The barrel shifter is constructed as a series of cascaded 2-to-1 and 4-to-1 multiplexers. In its largest configuration (64 bits), three rows of 4-to-1 MUXs are used. The architecture is based on a left-shifter block, a right-shifter block, a fill block and a direction block.

Data can be shifted left or right; the vacant bits are padded with zeros during a left shift and can be padded with MSB of the shift data bus during a right shift. A shift data bus (SHDIN) fills the vacant bits during a shift operation. During a right shift, the shift data bus fills the vacant bits with data from the LSB of the shift data bus; during a left shift, the shift data bus fills the vacant bits with data from the MSB of the shift data bus (essentially a circular shift).

Function Table

SHDIR	C1	C2	DOUT
0	0	0	Shift right and fill with zeros
0	0	1	Shift right and fill with MSB
0	1	0	Shift right and fill with data bus (SHDIN)
0	1	1	Right rotation
1	0	0	Shift left and fill with zeros
1	0	1	Shift left and fill with MSB
1	1	0	Shift left and fill with data bus (SHDIN)
1	1	1	Left rotation

Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits for the input data bus	4 to 64
type	Direction of shift	BOTH/LEFT/RIGHT
drv	Drive strength	1/2/4

Pin Description

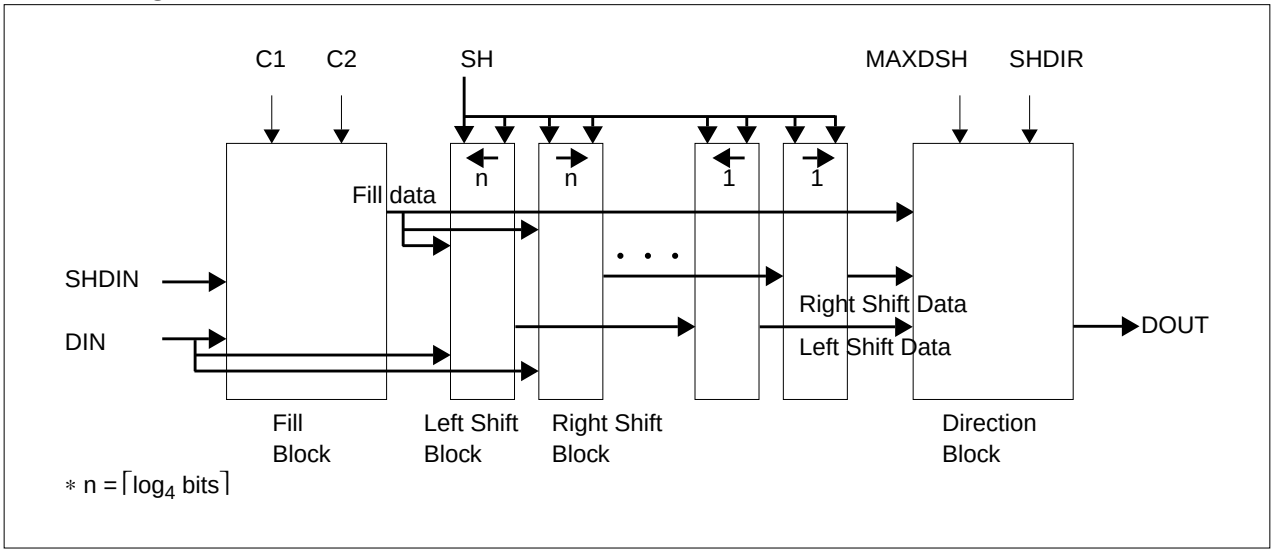
Name	I/O	Description
DIN [bits–1:0]	I	Data input
SHDIN [bits–1:0]		Shift data input
SHDIR		Shift direction (Left/Right) (optional when the parameter type = BOTH)
C1, C2		Control signals
SH [⌈$\log_2$bits⌉–1:0]		Shift amount (in binary)
MAXDSH		It fills data output with filling information according to C1 and C2. It refreshes output with fill data.
DOUT [bits–1:0]	O	Data output

⌈ ⌉ ceilling (the smallest integer greater than or equal to value)

Pin Capacitance [Unit: pF]

Name	Case	Value
C1	all	0.026
C2	all	0.046
SHDIN	all	0.029
MAXDSH	type = BOTH	0.043
	type = LEFT/RIGHT	0.053
DIN	type = BOTH	0.00005*bits*bits – 0.0027*bits + 0.207
	type = LEFT	0.00005*bits*bits – 0.0029*bits + 0.163
	type = RIGHT	0.00005*bits*bits – 0.0026*bits + 0.173
SH	type = BOTH	–0.00003*bits*bits + 0.00184*bits + 0.070
	type = LEFT	–0.000017*bits*bits + 0.001*bits + 0.032
	type = RIGHT	–0.000017*bits*bits + 0.0009*bits + 0.035
SHDIR	type = BOTH	0.022

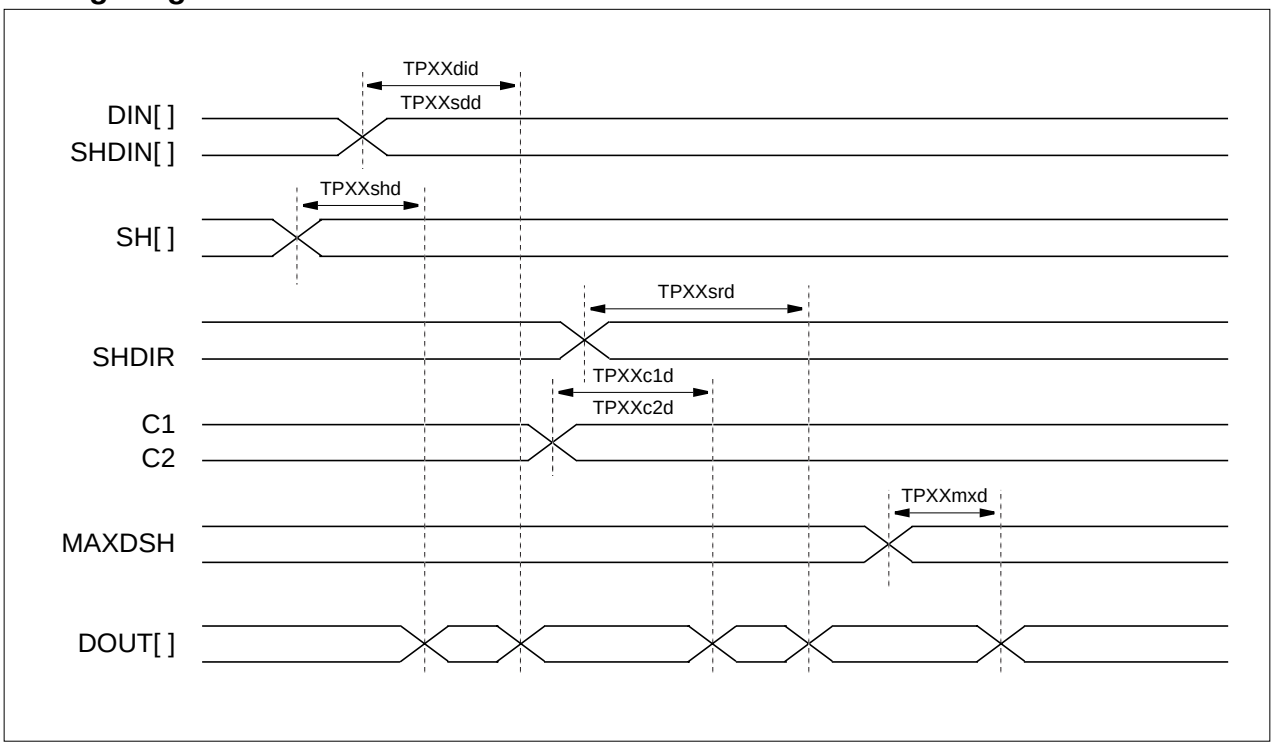
Block Diagram



BS

Barrel Shifter

Timing Diagram



Timing Type Definition

Timing Type	Definition
TPXXdid	Propagation delay, TPLH/TPHL, from input DIN to output DOUT
TPXXsdd	Propagation delay, TPLH/TPHL, from input SHDIN to output DOUT
TPXXshd	Propagation delay, TPLH/TPHL, from input SH to output DOUT
TPXXsrd	Propagation delay, TPLH/TPHL, from input SHDIR to output DOUT
TPXXc1d	Propagation delay, TPLH/TPHL, from input C1 to output DOUT
TPXXc2d	Propagation delay, TPLH/TPHL, from input C2 to output DOUT
TPXXmxd	Propagation delay, TPLH/TPHL, from input MAXDSH to output DOUT

Characteristic Reference Tables

Symbol	Description	Unit	Symbol	Description	Unit
T	Junction temperature	°C	S	Input slope	ns
V_{DD}	Power supply voltage	V	SL	Standard load	-
C_L	Output load	SL	SA	Input switching activity	-

1) Timing Characteristics [Unit: ns]

(Typical process, T=25, V_{DD}=3.3, C_L=10, S=0.2, SA=0.5)

Type	8	24	36	48	64
Case: type = BOTH, drv = 1					
TPHLc1d/TPLHc1d	0.99 / 1.10	1.20 / 1.30	1.31 / 1.41	1.38 / 1.48	1.41 / 1.54
TPHLc2d/TPLHc2d	0.95 / 1.17	1.14 / 1.29	1.23 / 1.35	1.29 / 1.41	1.30 / 1.45
TPHLdid/TPLHdid	1.20 / 1.36	1.38 / 1.52	1.47 / 1.59	1.52 / 1.63	1.53 / 1.62
TPHLmxd/TPLHmxd	0.54 / 0.70	0.61 / 0.82	0.65 / 0.90	0.69 / 0.98	0.74 / 1.08
TPHLshd/TPLHshd	0.72 / 0.84	0.86 / 0.96	0.92 / 1.02	0.95 / 1.05	0.92 / 1.05
TPHLsdd/TPLHsdd	0.72 / 0.84	0.86 / 0.97	0.93 / 1.06	0.95 / 1.14	0.92 / 1.22
TPHLsrd/TPLHsrd	0.52 / 0.64	0.56 / 0.73	0.59 / 0.79	0.62 / 0.83	0.66 / 0.86
Case: type = LEFT, drv = 1					
TPHLc1d/TPLHc1d	0.97 / 1.08	1.19 / 1.28	1.30 / 1.40	1.37 / 1.47	1.40 / 1.52
TPHLc2d/TPLHc2d	0.93 / 1.16	1.12 / 1.27	1.22 / 1.34	1.27 / 1.39	1.28 / 1.43
TPHLdid/TPLHdid	1.18 / 1.34	1.37 / 1.49	1.46 / 1.57	1.51 / 1.61	1.51 / 1.60
TPHLmxd/TPLHmxd	0.37 / 0.52	0.42 / 0.62	0.46 / 0.70	0.50 / 0.77	0.55 / 0.88
TPHLshd/TPLHshd	0.70 / 0.81	0.85 / 0.95	0.91 / 1.02	0.94 / 1.04	0.91 / 1.01
TPHLsdd/TPLHsdd	0.70 / 0.80	0.85 / 0.96	0.91 / 1.06	0.94 / 1.13	0.91 / 1.20
Case: type = RIGHT, drv = 1					
TPHLc1d/TPLHc1d	0.97 / 1.08	1.19 / 1.28	1.31 / 1.40	1.37 / 1.47	1.40 / 1.52
TPHLc2d/TPLHc2d	0.93 / 1.16	1.13 / 1.28	1.22 / 1.34	1.28 / 1.39	1.28 / 1.44
TPHLdid/TPLHdid	1.18 / 1.34	1.37 / 1.50	1.46 / 1.58	1.51 / 1.62	1.52 / 1.61
TPHLmxd/TPLHmxd	0.37 / 0.52	0.42 / 0.62	0.46 / 0.69	0.50 / 0.77	0.55 / 0.87
TPHLshd/TPLHshd	0.70 / 0.81	0.85 / 0.95	0.91 / 1.02	0.94 / 1.04	0.91 / 1.02
TPHLsdd/TPLHsdd	0.71 / 0.83	0.85 / 0.96	0.92 / 1.05	0.94 / 1.12	0.91 / 1.21

Characteristic Reference Table (Continued)

2) Power Characteristics [Unit: μW/MHz]

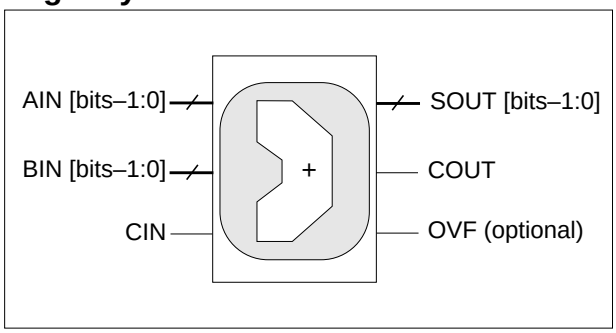
(Typical process, T=25, V_{DD}=3.3, C_L=10, S=0.2, SA=0.5)

Case	8	24	36	48	64
type=BOTH	18.22	104.12	168.54	232.96	318.86
type=LEFT	15.08	57.56	89.42	121.28	163.76
type=RIGHT	14.67	56.69	88.20	119.72	161.74

3) Size Variation [Unit: μm]

Type	Case	8	24	36	48	64
Width	type=BOTH	124.95	212.77	263.74	301.95	333.03
	type=LEFT/RIGHT	89.43	129.69	155.28	176.94	199.68
Height	all	146.00	376.40	549.20	722.00	952.40

Logic Symbol



Features

- *n*-bit (4 to 64) adder
- Two's complement or unsigned magnitude operation
- Functional model, schematic, and layout generators
- Timing model with auto-characterization
- Sophisticated double carry-select algorithm
- Two's complement overflow flag
- Three drive strength options for output

Function Description

The carry-select adder performs two's complement addition or unsigned magnitude operation. The overflow flag gets set if an overflow occurs while adding two positive or negative numbers.

The carry-select adder performs high speed binary addition by using a sophisticated double carry-select algorithm with group delay equalization for carry propagation. The outer carry-select scheme is used to provide a short path between the low order inputs and the high order outputs. The internal carry-select schemes are placed within these blocks to reduce their block propagation delays. The sizes of the carry-select blocks increase along the carry propagation tree to produce a fast addition.

Function Table

Type	Function
Adder	SOUT=AIN + BIN + CIN
Overflow	(~SOUT [bits–1]) • (AIN [bits–1] • BIN [bits–1]) + (SOUT [bits–1]) • (~AIN [bits–1]) •(~BIN [bits–1])

Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits for the input data bus	4 to 64
overflow	Overflow flag for signed operation	0/1
drv	Drive strength	1/2/4

CSADDER

Carry Select Adder

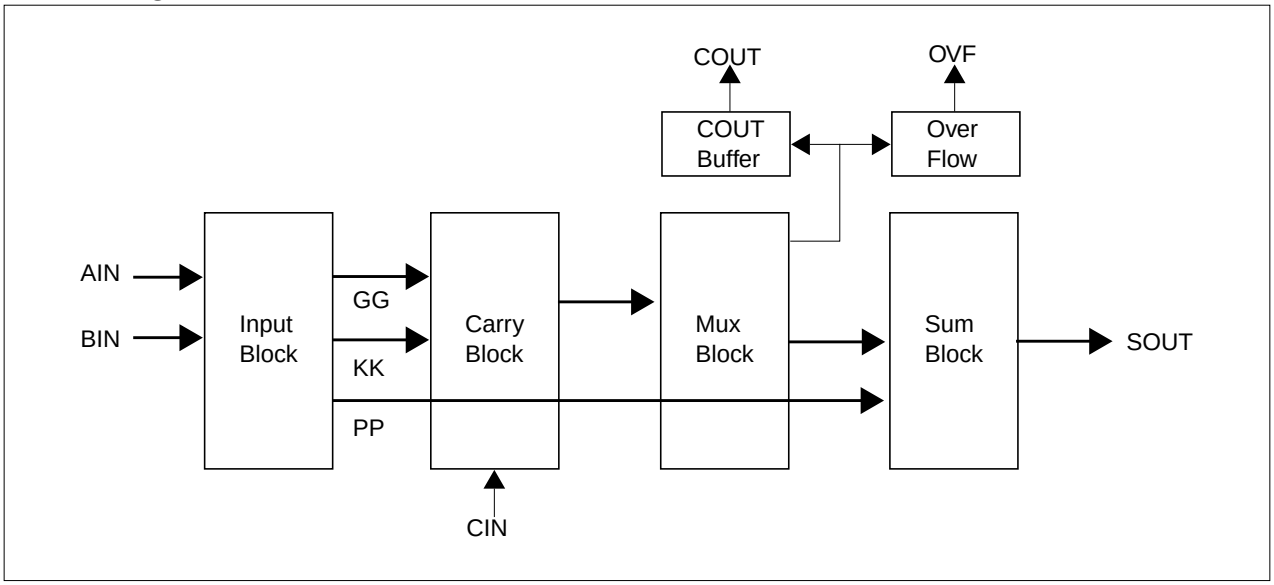
Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input
BIN [bits–1:0]		Data input
CIN		Carry-in
SOUT [bits–1:0]	O	Result of addition
COUT		Carry-out
OVF		Overflow output occurs during a signed addition (optional when the parameter overflow = 1)

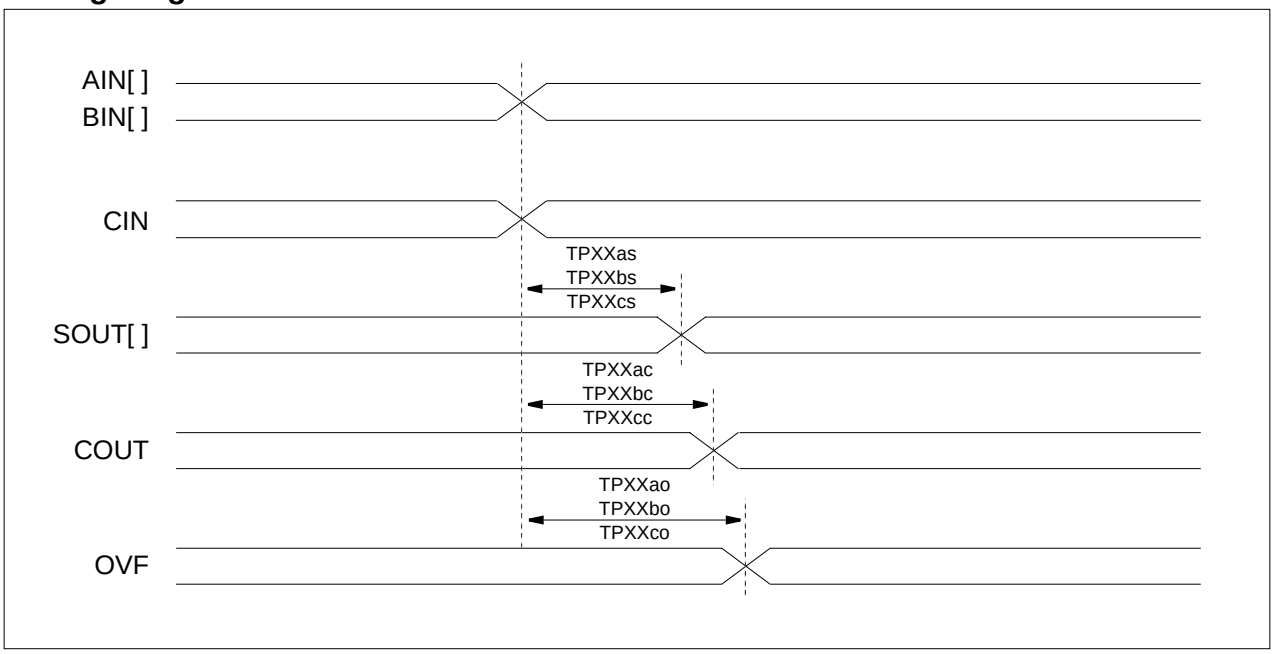
Pin Capacitance [Unit: pF]

Name	Value
AIN	0.036
BIN	0.036
CIN	0.031

Block Diagram



Timing Diagram



Timing Type Definition

Timing Type	Definition
TPXXas	Propagation delay, TPLH/TPHL, from input AIN to output SOUT
TPXXbs	Propagation delay, TPLH/TPHL, from input BIN to output SOUT
TPXXcs	Propagation delay, TPLH/TPHL, from input CIN to output SOUT
TPXXac	Propagation delay, TPLH/TPHL, from input AIN to output COUT
TPXXbc	Propagation delay, TPLH/TPHL, from input BIN to output COUT
TPXXcc	Propagation delay, TPLH/TPHL, from input CIN to output COUT
TPXXao	Propagation delay, TPLH/TPHL, from input AIN to output OVF
TPXXbo	Propagation delay, TPLH/TPHL, from input BIN to output OVF
TPXXco	Propagation delay, TPLH/TPHL, from input CIN to output OVF

CSADDER

Carry Select Adder

Characteristic Reference Table

Symbol	Description	Unit	Symbol	Description	Unit
T	Junction temperature	°C	S	Input slope	ns
V_{DD}	Power supply voltage	V	SL	Standard load	-
C_L	Output load	SL	SA	Input switching activity	-

1) Timing Characteristics [Unit: ns]

(Typical process, T=25, V_{DD}=3.3, C_L=10, S=0.2, SA=0.5)

Type	8	24	36	48	64
Case: ovf=0					
TPHLac/TPLHac	1.181/1.106	1.623/1.575	1.893/1.858	2.112/2.083	2.324/2.290
TPHLbc/TPLHbc	1.164/1.062	1.605/1.554	1.876/1.848	2.095/2.079	2.307/2.288
TPHLcc/TPLHcc	0.844/0.768	1.274/1.235	1.536/1.507	1.746/1.711	1.945/1.877
TPHLas/TPLHas	1.444/1.518	1.806/1.887	2.077/2.165	2.348/2.442	2.710/2.811
TPHLbs/TPLHbs	1.427/1.500	1.788/1.870	2.060/2.147	2.331/2.424	2.692/2.794
TPHLcs/TPLHcs	1.171/1.260	1.492/1.583	1.733/1.825	1.975/2.068	2.296/2.391
Case: ovf=1					
TPHLac/TPLHac	1.315/1.253	1.764/1.721	2.041/2.003	2.266/2.226	2.486/2.431
TPHLbc/TPLHbc	1.306/1.220	1.753/1.704	2.026/1.991	2.245/2.214	2.454/2.411
TPHLcc/TPLHcc	1.052/0.911	1.374/1.378	1.615/1.650	1.856/1.854	2.178/2.020
TPHLas/TPLHas	1.381/1.526	1.900/1.896	2.200/2.173	2.424/2.450	2.603/2.820
TPHLbs/TPLHbs	1.364/1.509	1.883/1.880	2.183/2.158	2.407/2.437	2.586/2.808
TPHLcs/TPLHcs	1.202/1.277	1.523/1.597	1.764/1.837	2.006/2.077	2.327/2.397
TPHLao/TPLHao	1.460/1.546	1.938/1.983	2.228/2.255	2.459/2.480	2.676/2.706
TPHLbo/TPLHbo	1.431/1.526	1.916/1.960	2.212/2.233	2.448/2.461	2.671/2.695
TPHLco/TPLHco	1.234/1.275	1.555/1.593	1.796/1.832	2.038/2.071	2.359/2.389

2) Power Characteristics [Unit: μW/MHz]

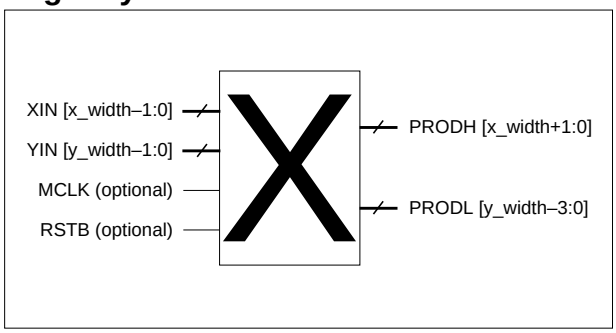
(Typical process, T=25, V_{DD}=3.3, C_L=10, S=0.2, SA=0.5)

Case	8	24	36	48	64
overflow=0	13.97	55.88	89.72	120.14	163.40
overflow=1	15.12	57.20	90.83	121.58	164.68

3) Size Variation [Unit: μm]

Type	8	24	36	48	64
Width	157.5	437.5	647.5	857.5	1137.5
Height	80.5	80.5	80.5	80.5	80.5

Logic Symbol



Features

- *n*-bit (6 to 64) multiplier
- Functional model, schematic and layout generators
- Timing model with auto-characterization
- High speed and density
- Two's complement multiplication
- pipeline stage
- accumulator

Function Description

The BMPY builds multipliers from 6-bits to 64-bits with an accumulator, a configurable size of output buffer and a pipe. The BMPY uses the modified Booth's algorithm to encode the multiplier bits by partitioning the bits into three bit groups, with one bit shared between groups.

You can insert one pipeline stage, which increases the efficiency of the multiplier. The MSB adder used in the design is a fast group bypass adder. The LSB adder is programmable to take a pipe and is, therefore, the adder array. The clock to the pipeline controls the internal data change, so that the data is always stable throughout the clock period and there is no hold problem.

Parameter Description

Parameter Name	Description	Range
x_width (note)	Multiplicand bits (the x-input width)	6 to 64 (even)
y_width	Multiplier bits (the y-input width)	6 to 64 (even)
pipes	Pipeline stage	0/1
accum	0: none; n: (x_width+n) bit accumulator	0/1/2/3/4
obuff	1: 6x output buffer; 2: 12x output buffer	1/2

NOTE: x_width should be greater than or equal to y_width ($x \geq y$).

BMPY

Modified Booth Multiplier

Pin Description

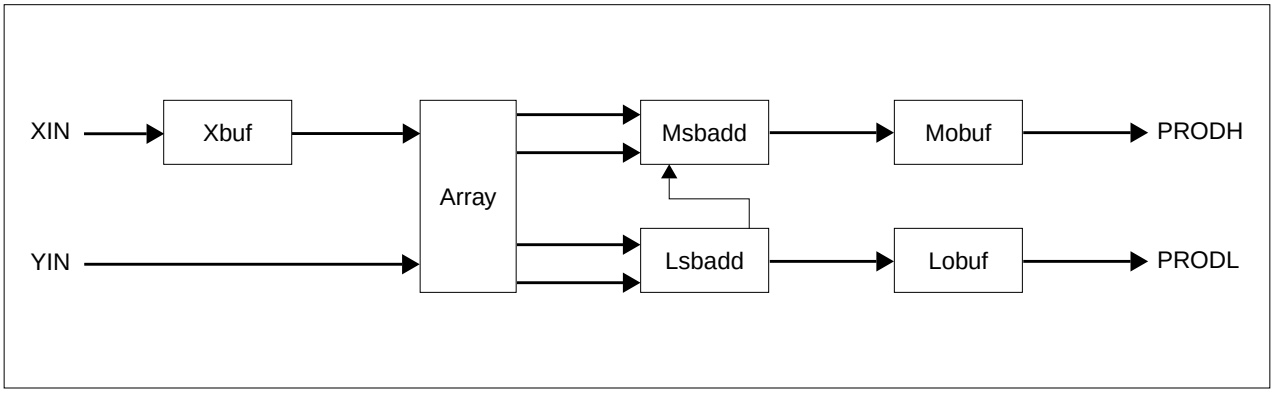
Pin Name	I/O	Description
XIN [x_width–1:0]	I	Data input – multiplicand
YIN [y_width–1:0]		Data input – multiplier
MCLK		Clock input to the latches (optional when pipes = 1 or accum ≥ 1)
RSTB		Input reset line for the latches. If the multiplier has an accumulator, the reset lines ensure that the contents of the accumulator is zero before the first set of XIN * YIN arrives to the accumulator (optional when pipes = 1 or accum ≥ 1).
PRODH [x_width+1:0]	O	Data output lines from the MSB adder. The values of these lines together with the prodL values give the output data (product).
PRODL [y_width–3:0]		Data output lines from the LSB adder

Pin Capacitance [Unit: pF]

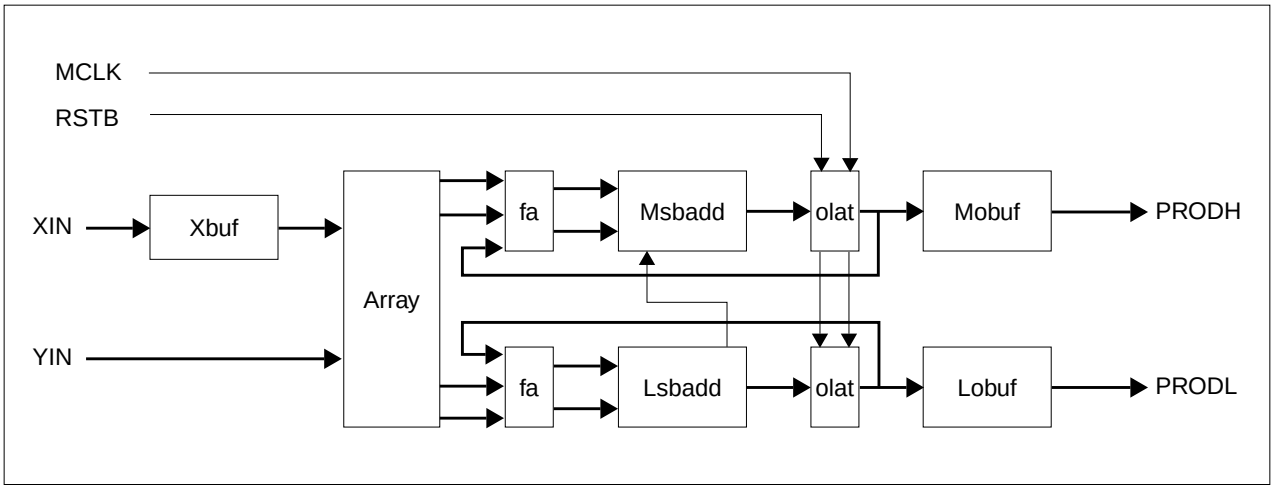
Name	Case	Value
XIN	all	0.044
YIN	all	0.046
MCLK	accum=1/2/3/4	0.045
	pipe=1	0.00532*x_width+0.00045*y_width+0.03364-0.00002*x_width*y_width
RSTB	accum=1/2/3/4	0.045
	pipe=1	0.00632*x_width+0.00052*y_width+0.03209 -0.00002*x_width*y_width

Block Diagram

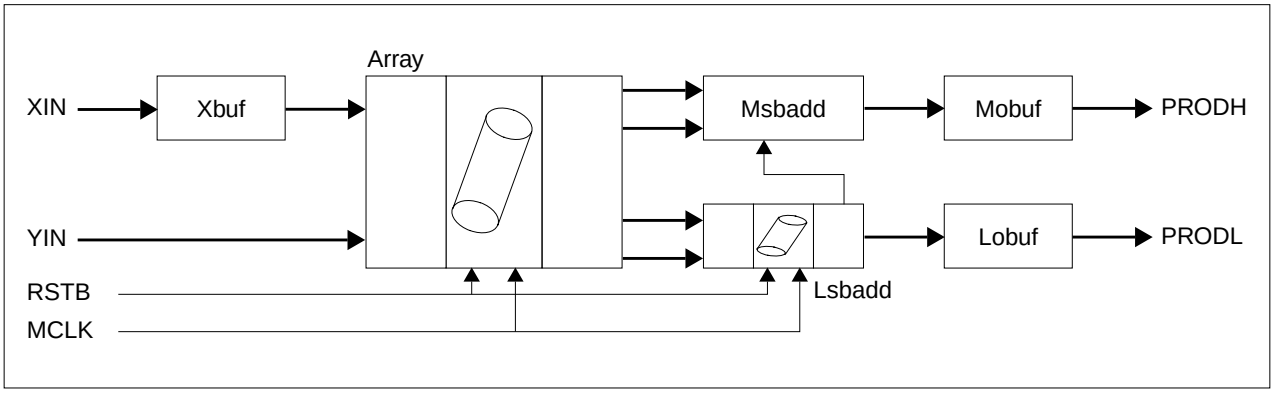
<pipe=0, accum=0>



<pipes=0, accum=1/2/3/4>

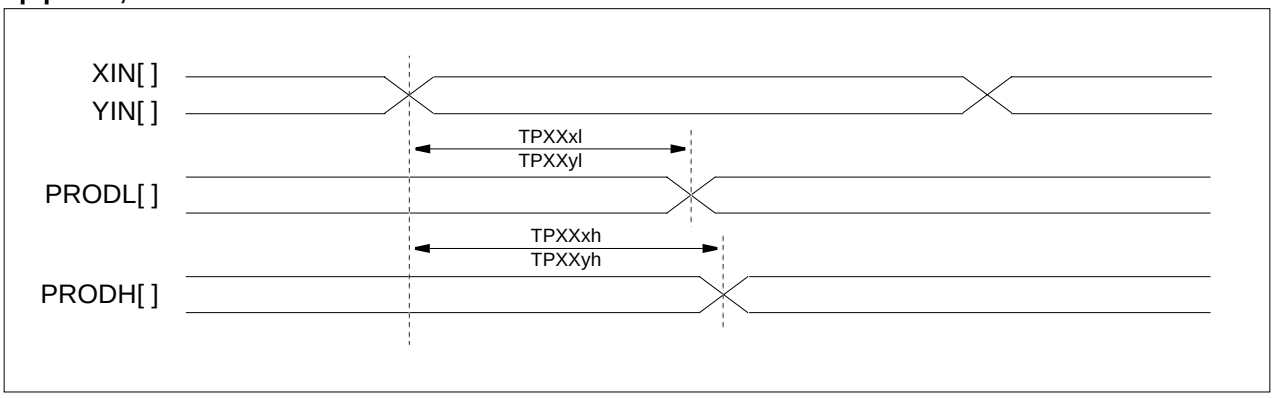


<pipes=1, accum=0>



Timing Diagram

<pipes=0, accum=0>

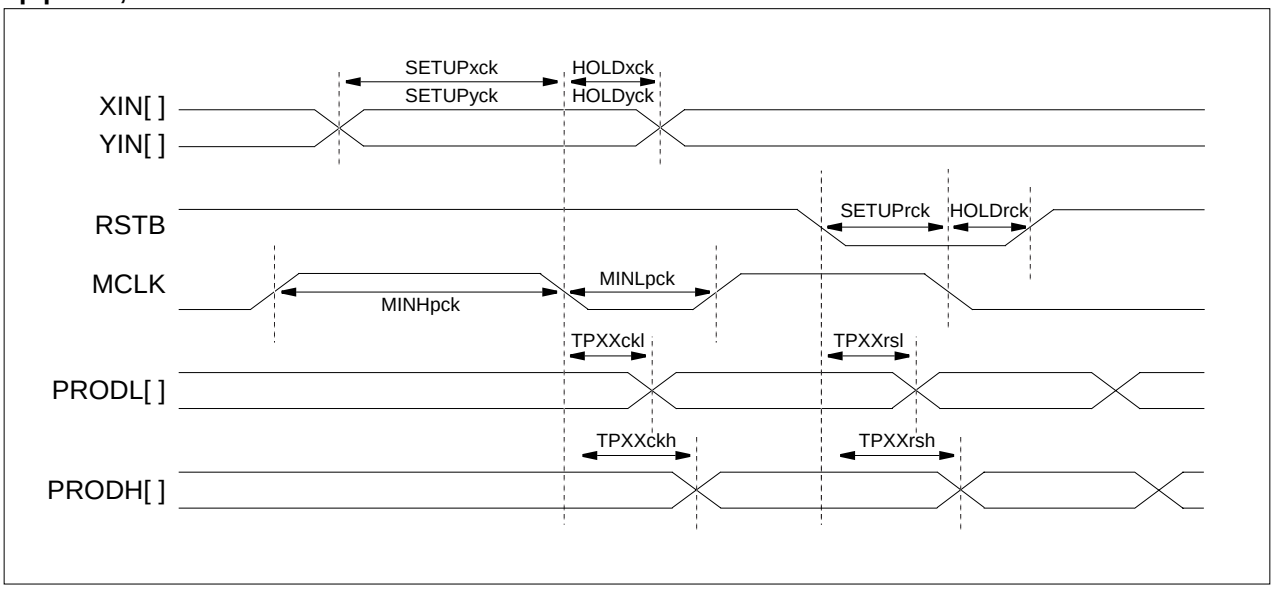


Timing Type Definition

Timing Type	Definition
TPXXxl	Propagation delay, TPLH/TPHL, from input XIN to output PRODL
TPXXyl	Propagation delay, TPLH/TPHL, from input YIN to output PRODL
TPXXxh	Propagation delay, TPLH/TPHL, from input XIN to output PRODH
TPXXyh	Propagation delay, TPLH/TPHL, from input YIN to output PRODH

Timing Diagram (Continued)

<pipes=0, accum=1/2/3/4>



Timing Type Definition

Timing Type	Definition
SETUPxck	Setup time for input XIN to MCLK
SETUPyck	Setup time for input YIN to MCLK
SETUPrck	Setup time for input RSTB to MCLK
HOLDxck	Hold time for input XIN to MCLK
HOLDyck	Hold time for input YIN to MCLK
HOLDrck	Hold time for inptu RSTB to MCLK
MINHpck	Minimum Pulse width for the HIGH state of MCLK
MINLpck	MInimum Pulse width for the LOW state of MCLK
TPXXckl	Propagation delay, TPLH/TPHL, from input MCLK to output PRODL
TPXXckh	Propagation delay, TPLH/TPHL, from input MCLK to output PRODH
TPXXrsl	Propagation delay, TPLH/TPHL, from input RSTB to output PRODL
TPXXrsh	Propagation delay, TPLH/TPHL, from input RSTB to output PRODH

<pipes=1, accum=0>

It should be the same as <pipes=0, accum=1/2/3/4>.
But, you may not concern the SETUPrck and HOLDrck for this type.

BMPY

Modified Booth Multiplier

Characteristic Reference Table

Symbol	Description	Unit	Symbol	Description	Unit
T	Junction temperature	°C	S	Input slope	ns
V_{DD}	Power supply voltage	V	SL	Standard load	-
C_L	Output load	SL	SA	Input switching activity	-

1) Timing Characteristics [Unit: ns]

(Typical process, T=25, V_{DD}=3.3, C_L=10, S=0.2, SA=0.5)

Type	8x8	24x24	36x36	48x48	64x64
Case: pipes=0,accum=0					
TPHLxh/TPLHxh	2.29 / 2.11	4.57 / 4.42	6.23 / 6.11	7.86 / 7.75	9.98 / 9.86
TPHLyh/TPLHyh	2.12 / 2.06	4.14 / 4.11	5.65 / 5.64	7.16 / 7.18	9.18 / 9.23
TPHLxl/TPLHxl	1.64 / 1.47	3.53 / 3.37	4.94 / 4.80	6.36 / 6.22	8.25 / 8.13
TPHLyl/TPLHyl	1.57 / 1.51	3.09 / 2.98	4.22 / 4.08	5.35 / 5.18	6.87 / 6.65
Case: pipes=0,accum=4					
HOLDrck	0.17	0.20	0.22	0.24	0.26
HOLDxck	0.17	0.20	0.22	0.24	0.26
HOLDyck	0.17	0.20	0.22	0.24	0.26
MINHpck	2.62	4.47	5.82	7.14	8.85
MINLpck	2.94	5.04	6.62	8.20	10.30
SETUPrck	0.39	0.47	0.54	0.59	0.67
SETUPxck	2.76	4.84	6.40	7.97	10.05
SETUPyck	2.43	4.20	5.53	6.85	8.62
TPHLckh/TPLHckh	0.81 / 0.75	0.85 / 0.78	0.88 / 0.81	0.90 / 0.84	0.94 / 0.87
TPHLrsh/TPLHrsh	0.82 / 0.00	0.91 / 0.00	0.98 / 0.00	1.05 / 0.00	1.14 / 0.00
TPHLckl/TPLHckl	0.78 / 0.72	0.82 / 0.76	0.85 / 0.79	0.89 / 0.82	0.93 / 0.87
TPHLrsl/TPLHrsl	0.76 / 0.00	0.86 / 0.00	0.94 / 0.00	1.01 / 0.00	1.09 / 0.00
Case: pipes=1,accum=0					
HOLDxck	0.10	0.10	0.10	0.10	0.10
HOLDyck	0.10	0.10	0.10	0.10	0.10
MINHpck	0.19	0.34	0.45	0.57	0.73
MINLpck	0.18	0.26	0.31	0.36	0.43
SETUPxck	1.40	2.20	2.95	3.83	5.19
SETUPyck	1.36	2.04	2.66	3.39	4.52
TPHLckh/TPLHckh	1.60 / 1.84	3.03 / 3.20	3.93 / 4.07	4.70 / 4.82	5.51 / 5.63
TPHLrsh/TPLHrsh	1.56 / 0.00	1.67 / 0.00	1.80 / 0.00	1.97 / 0.00	2.27 / 0.00
TPHLckl/TPLHckl	0.79 / 0.78	2.00 / 2.10	2.71 / 2.85	3.26 / 3.39	3.74 / 3.80
TPHLrsl/TPLHrsl	0.75 / 0.00	1.91 / 0.00	2.31 / 0.00	2.30 / 0.00	1.65 / 0.00

Characteristic Reference Table (Continued)

2) Power Characteristics [Unit: μW/MHz]

(Typical process, T=25, V_{DD}=3.3, C_L=10, S=0.2, SA=0.5)

Case	8x8	24x24	36x36	48x48	64x64
accum=0, pipes=0	149.72	1018.84	2427.96	4486.17	8240.17
accum=1, pipes=0	272.43	1341.26	3015.24	5436.97	9829.09
accum=2, pipes=0	280.45	1350.89	3022.89	5439.90	9821.48
accum=3, pipes=0	288.24	1353.59	3024.77	5443.53	9831.43
accum=4, pipes=0	290.47	1358.38	3029.50	5446.49	9829.40
accum=0, pipes=1	241.02	1167.63	2564.31	4562.45	8162.25

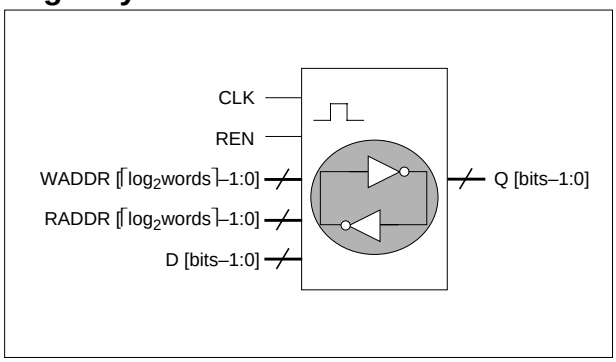
3) Size Variation [Unit: μm]

Type	Case	8x8	24x24	36x36	48x48	64x64
Width	pipes=0, accum=0	286.18	637.30	903.97	1173.50	1537.33
	pipes=0, accum=1	363.61	717.50	990.00	1268.56	1649.40
	pipes=0, accum=2	363.37	716.94	989.43	1268.18	1649.60
	pipes=0, accum=3	363.37	716.94	989.43	1268.18	1649.60
	pipes=0, accum=4	363.98	717.51	989.95	1268.64	1649.95
	pipes=1, accum=0	360.89	711.25	976.24	1243.14	1601.98
Height	pipes=0, accum=0	146.00	376.40	549.20	722.00	952.40
	pipes=0, accum=1	160.40	390.80	563.60	736.40	966.80
	pipes=0, accum=2	174.80	405.20	578.00	750.80	981.20
	pipes=0, accum=3	189.20	419.60	592.40	765.20	995.60
	pipes=0, accum=4	203.60	434.00	606.80	779.60	1010.00
	pipes=1, accum=0	160.40	390.80	563.60	736.40	966.80

REGF

Register File

Logic Symbol



Features

- *n*-bit (8 to 64) register file
- Functional model, schematic and layout generators
- Timing model with auto-characterization
- Configurable read/write ports for macro block (1-to-2 write and 1-to-4 Read ports)
- Synchronous operation in write mode
- Asynchronous operation in read mode
- Up to 8K bits capacity
- Up to 128 words
- Up to 64 bits

Function Description

The register file is built with one to four read ports and with one to two write ports.
All read and write ports are independent. The read ports always output data; data will be changed after the read address has been changed. The write ports are enabled by REN and data is latched into the memory location on the falling edge of the clock.

Parameter Description

Parameter Name	Description	Range
words	Number of words in the register file	8 to 128
bits	Number of bits per word	8 to 64
writes	Number of write ports	1/2
reads	Number of read ports	1/2/3/4

Pin Description

Pin Name	I/O	Description
CLK0 (writes ≥1) CLK1 (writes=2)	I	Clock signal for each write port. When the clock is high, data pass into the decoded memory location and is latched on the falling clock edge.
REN0 (writes ≥1) REN1 (writes=2)		Register enable signal for each write port. A high state prevents a write operation to the write port; a low state allows a write operation.
WADDR0 [⌈$\log_2$words⌉–1:0] (writes ≥1) WADDR1 [⌈$\log_2$words⌉–1:0] (writes=2)		Address input – Write address bus There is one address bus for each write port and there can be from 1 to 2 write ports.
RADDR0 [⌈$\log_2$words⌉–1:0] (reads ≥1) RADDR1 [⌈$\log_2$words⌉–1:0] (reads ≥2) RADDR2 [⌈$\log_2$words⌉–1:0] (reads ≥3) RADDR3 [⌈$\log_2$words⌉–1:0] (reads =4)		Address input – Read address bus There is one address bus for each read port and there can be from 1 to 4 read ports.
D0 [bits–2:0] (writes ≥1) D1 [bits–2:0] (writes =2)		Data Input – Word values written into the write port location during the write operation. There is one input bus for each write port.
Q0 [bits–2:0] (reads ≥1) Q1 [bits–2:0] (reads ≥2) Q2 [bits–2:0] (reads ≥3) Q3 [bits–2:0] (reads =4)	O	Output data previously written into the register file. Data are present at all times and its value depends on the read address. There is one output bus for each read port.

⌈ ⌉ ceilling (the smallest integer greater than of equal to value)

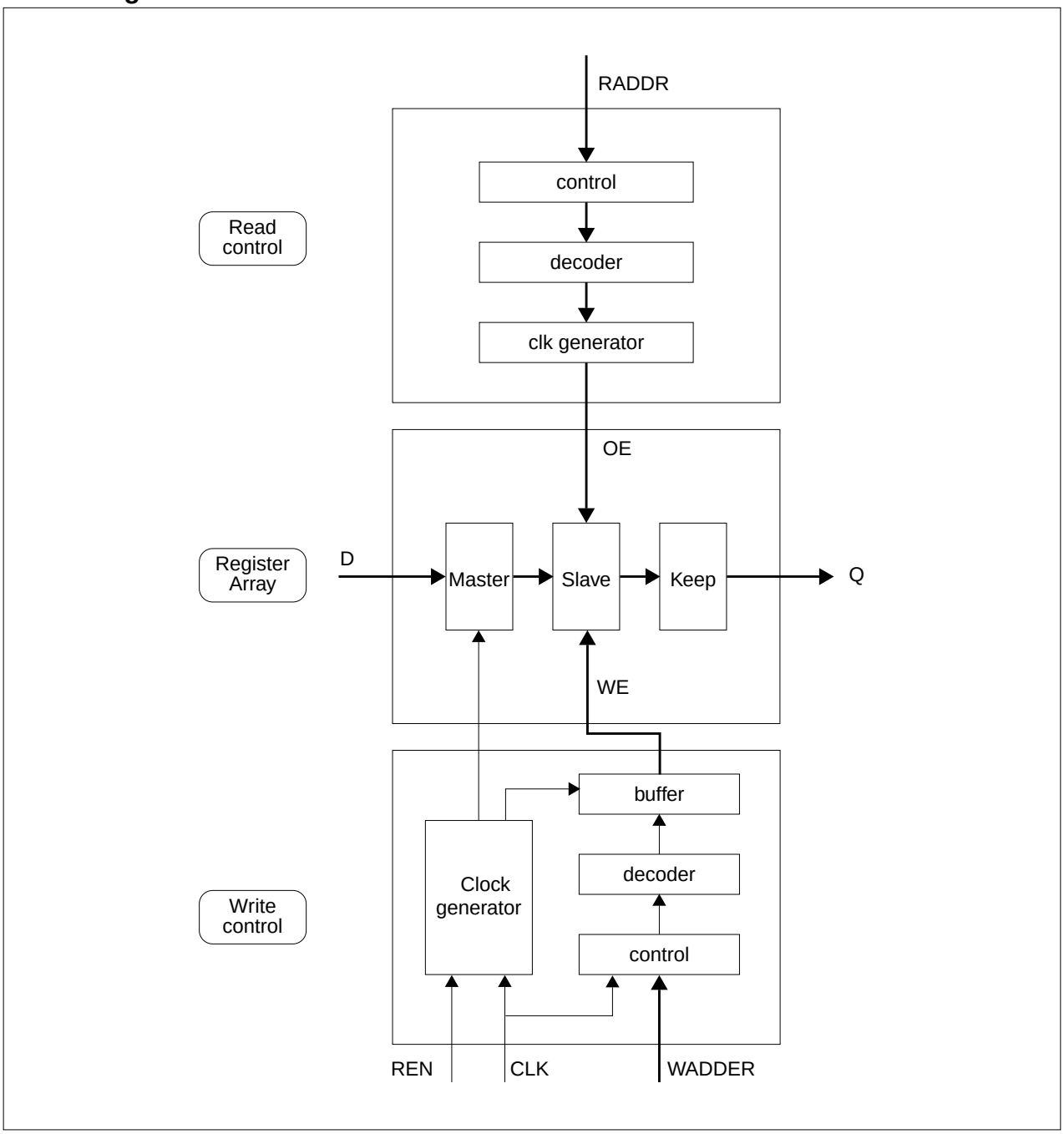
Pin Capacitance [Unit: pF]

Name	Case	Value
CLK0/1	writes=1/2	1.88e-06*bits+6.15e-03*words+9.07e-02-4.84e-08*bits*words
D0/1	writes=1/2	2.23e-10*bits+2.23e-10*words+2.30e-02-2.09e-11*bits*words
REN0/1	writes=1/2	5.43e-11*bits-1.27e-10*words+4.60e-02+1.64e-12*bits*words
WADDR0/1	writes=1/2	2.23e-10*bits+2.23e-10*words+2.30e-02-2.09e-11*bits*words
RADDR0/1/2/3	reads=1/2/3/4	5.36e-11*bits-1.29e-10*words+2.20e-02+5.17e-12*bits*words

REGF

Register File

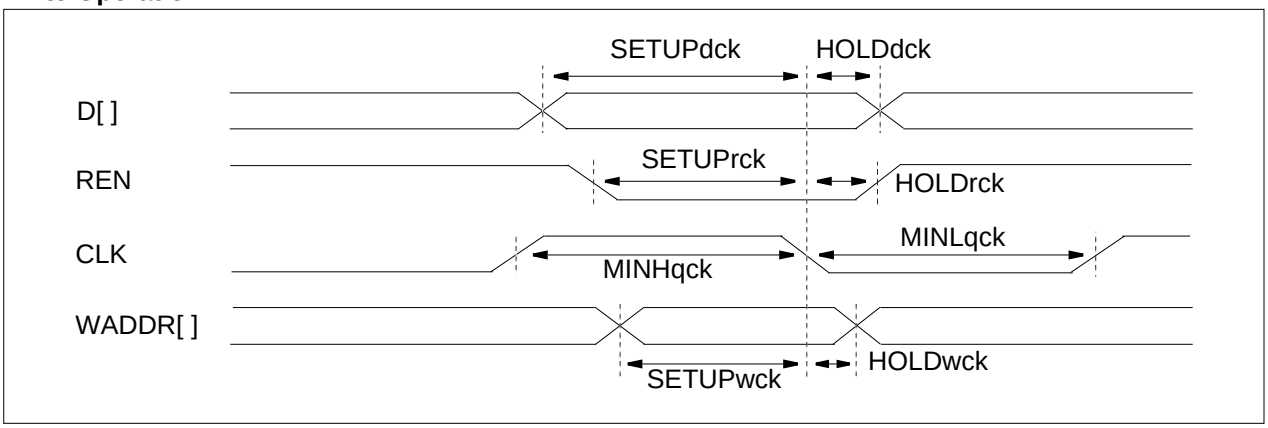
Block Diagram



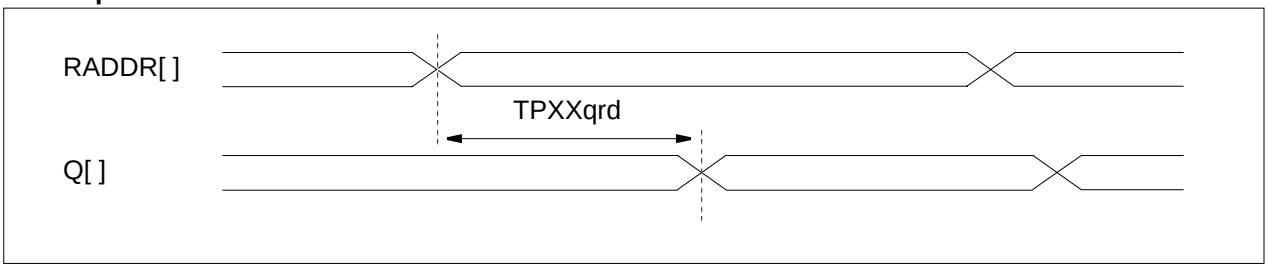
NOTE: The register file has two kind of layout structure. One is to place read and write control on the left side and right side of the register array. The other is to place them on the top and bottom of the register array block. The register file decides their position by bits and words size. When bits are greater than or equal to words, the read and write control block will be located on the top and bottom of the Array. On the other hand, the left and right side of the Array will be filled with them.

Timing Diagram

Write Operation



Read Operation



NOTE: Not allowed to read from and write to the same location at the same time.

Timing Type Definition

Timing Type	Definition
SETUPdck	Setup time for input D to CLK
SETUPrck	Setup time for input REN to CLK
SETUPwck	Setup time for input WADDER to CLK
HOLDdck	Hold time for input D to CLK
HOLDrck	Hold time for input REN to CLK
HOLDwck	Hold time for inptu WADDER to CLK
MINHqck	Minimum Pulse width for the HIGH state of CLK
MINLqck	MInimum Pulse width for the LOW state of CLK
TPXXqrd	Propagation delay, TPLH/TPHL, from input RADDR to output Q

REGF

Register File

Characteristic Reference Table

Symbol	Description	Unit	Symbol	Description	Unit
T	Junction temperature	°C	S	Input slope	ns
V_{DD}	Power supply voltage	V	SL	Standard load	-
C_L	Output load	SL	SA	Input switching activity	-

1) Timing Characteristics [Unit: ns]

(Typical process, T=25, V_{DD}=3.3, C_L=10, S=0.2, SA=0.5)

Type	8x8	24x24	36x36	48x48	64x64
HOLDdck	0.082	0.182	0.257	0.332	0.432
HOLDwck	-0.100	-0.100	-0.100	-0.100	-0.100
HOLDdrs	0.112	0.218	0.298	0.378	0.484
HOLDrck	-0.192	-0.543	-0.806	-1.069	-1.420
SETUPdck	0.251	0.162	0.096	0.030	-0.058
SETUPwck	0.600	0.600	0.600	0.600	0.600
SETUPdrs	0.204	0.110	0.039	-0.032	-0.126
SETUPrck	0.669	1.154	1.520	1.890	2.386
MINLqck	0.100	0.100	0.100	0.100	0.100
MINHqck	0.481	0.684	0.836	0.989	1.192
TPHLqck/TPLHqck	1.266/1.372	1.647/1.701	1.933/1.948	2.218/2.195	2.599/2.525
TPHLqrd/TPLHqrd	1.293/1.323	1.764/1.766	2.118/2.098	2.472/2.431	2.944/2.874

2) Power Characteristics [Unit: μW/MHz]

<Write mode / Read mode> (Typical process, T=25, V_{DD}=3.3, C_L=10, S=0.2, SA=0.5)

Case	8x8	24x24	36x36	48x48	64x64
read=1, write=1	38.87/23.67	111.74/53.86	181.87/96.83	247.59/136.06	344.72/209.05
read=1, write=2	79.48/34.92	209.41/74.89	312.93/112.12	456.89/159.32	622.59/231.76
read=2, write=1	40.79/38.07	113.38/64.36	182.01/109.98	247.24/152.71	346.92/232.01
read=2, write=2	76.01/48.78	215.74/108.05	331.75/133.30	488.43/267.97	667.49/406.62
read=3, write=1	43.40/51.03	126.03/99.64	203.49/170.93	276.24/267.31	409.01/423.65
read=3, write=2	82.57/61.16	226.48/147.11	350.41/196.45	531.31/379.85	741.17/587.98
read=4, write=1	44.54/66.50	124.02/110.22	202.72/177.31	272.27/273.57	391.41/419.65
read=4, write=2	79.42/76.16	229.66/185.51	367.89/217.59	557.06/478.36	780.43/753.44

3) Size Variation [Unit: μm]

Type	Case	8x8	24x24	36x36	48x48	64x64
Width	all	140.0	420.0	630.0	840.0	1120.0
Height	reads=1, writes=1	221.5	477.0	648.5	816.5	1040.5
	reads=2, writes=1	268.7	576.0	773.7	965.7	1221.7
	reads=3 writes=1	333.1	726.0	974.1	1214.1	1534.1
	reads=4 writes=1	414.7	927.0	1249.7	1561.7	1977.7
	reads=1 writes=2	309.3	617.5	815.3	1007.3	1263.3
	reads=2 writes=2	360.7	722.5	946.7	1162.7	1450.7
	reads=3 writes=2	429.3	878.5	1153.3	1417.3	1769.3
	reads=4 writes=2	515.1	1085.5	1435.1	1771.1	2219.1

PLL

6

Contents

General Description

The AL2007LX is a Phase-Locked Loop (PLL) frequency synthesizer constructed in CMOS on single monolithic structure.

The PLL macrofunctions provide frequency multiplication capabilities.

The output clock frequency is related to the input clock frequency Fin (XTALIN) by the following equation:

Fout = (m x Fin) / (p x s).

where

Fout is the output clock frequency.

Fin is the input clock frequency.

m, p and s are the values for programmable dividers.

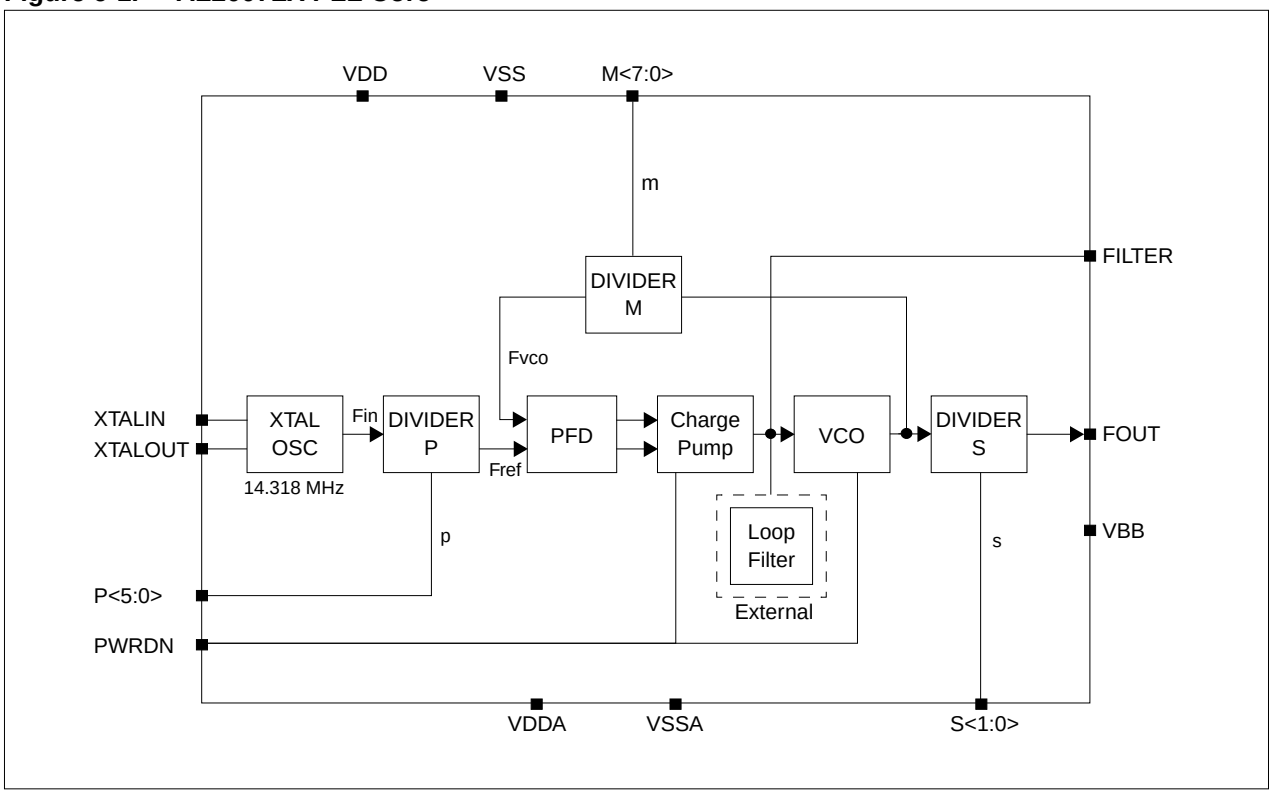
AL2007LX consists of a Phase/Frequency Detector (PFD), a Charge Pump, an external loop filter, a Voltage Controlled Oscillator (VCO), a 6-bit pre-divider, an 8-bit main divider and a 2-bit post scaler as shown in Figure 6-1.

Features

- 0.35μm CMOS device technology
- 3.3V single power supply
- Output frequency range: 20-170MHz
- Jitter: ±150ps
- Duty ratio: 40% to 60%
- Frequency changed by programmable dividers
- Provision for 14.318MHz crystal oscillator
- Power down mode

Block Diagram

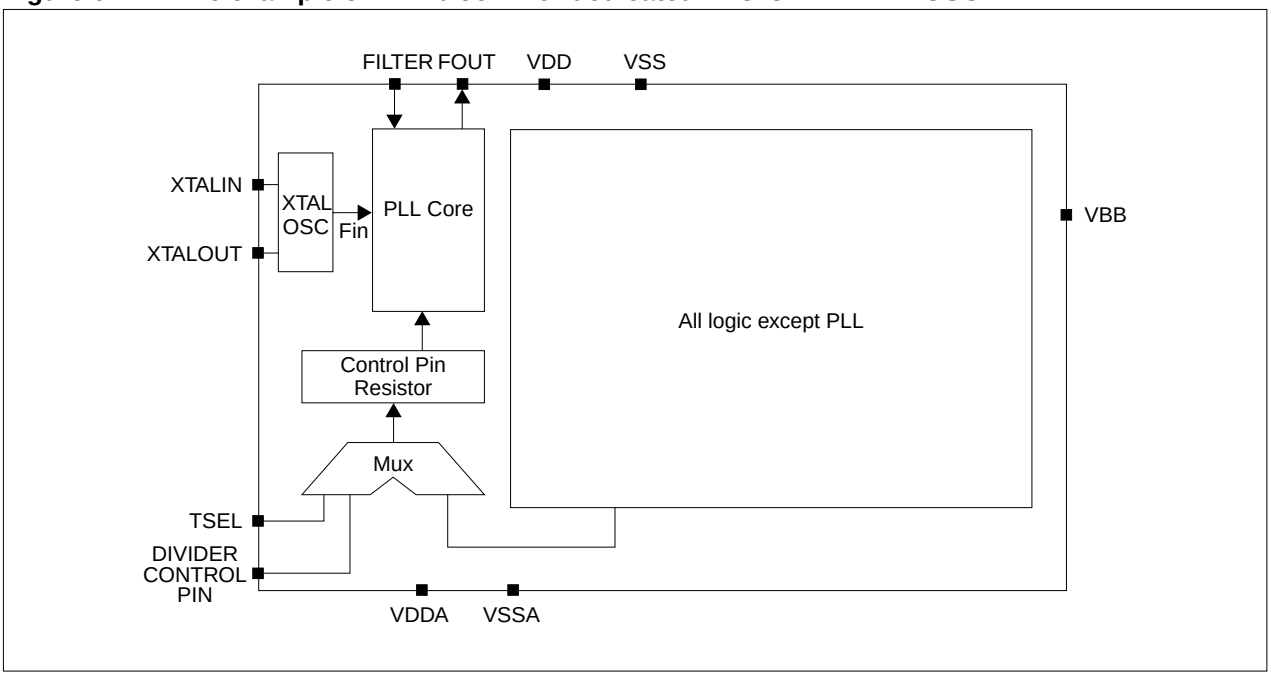
Figure 6-1. AL2007LX PLL Core



Pin Description

Pin Name	I/O	Description
VDD	P	Digital power supply for FSPLL
VSS	G	Digital ground for FSPLL
VDDA	P	Analog power supply for FSPLL
VSSA	G	Analog ground for FSPLL
VBB	G	Bulk ground
XTALIN	I	External clock input (14.318MHz) or crystal Input. If XTALIN isn't used, the XTALIN is FIN.
XTALOUT	O	External crystal output. If a crystal is used, it is connected across the I/O pins XTALIN and XTALOUT. If XTALOUT isn't used, it has to float the output.
FILTER	I	A capacitor is connected between the pin and analog ground.
FOUT	O	FSPLL clock output
PWRDN	I	FSPLL clock power down (active high)
P [5:0]	I	The values for 6-bit programmable divider
M [7:0]	I	The values for 8-bit programmable divider
S [1:0]	I	The values for 2-bit programmable divider

Figure 6-2. The example of PLL block with dedicated 14.318MHz XTAL-OSC



THE USAGE OF AL2007LX PLL CORE

— There are two crystal oscillator (XTAL-OSC) options for the AL2007LX PLL core.

1. With dedicated 14.318MHz XTAL-OSC:
   As shown in Figure 6-2., generally the crystal component of 14.318MHz is connected to the XTALIN and XTALOUT pins of dedicated 14.318MHz XTAL-OSC. If the crystal component is ignored, an external clock source is applied to the XTALIN pin with the XTALOUT pin being floated.
2. With SEC's 10MHz-40MHz programmable XTAL-OSC:
   If a wide range of crystal component is used instead of the component of a fixed 14.318MHz, it is recommended to use SEC's 10MHz-40MHz programmable XTAL-OSC cell (PSOSCM2) with a positive enable pin like Figure 6-3. A crystal component is located between the PADA pin and the PADB pin. The enable pin E must be HIGH in normal operation. The typical current consumption of PSOSCM2 is 10.93mA.

— When implementing an embedded PLL block, the following pins must be bypassed externally for testing the PLL locking function:
XTALIN, XTALOUT, FILTER, FOUT, VDDA, VSSA, VDD, VSS and VBB (According to the XTAL-OSC option, PADA, PADB and E)

— In case of self test logic, the divider control pins (P, M, S) and the TSEL pin must be bypassed externally for testing.

— The digital power (VDD, VSS), the analog power (VDDA, VSSA) and the bulk power must be dedicated to the PLL only and separated. If the dedicated VDD and VSS is not allowed, that of the least power consuming block are shared with the PLL as shown in Figure 6-3.

— The PIA_BB pad is used as a FILTER pad that contains only ESD protection diodes without any resisters and buffers.

— The FOUT and FILTER pins must be placed far from the internal signals in order to avoid overlapping the signal lines.

— The blocks having a large digital switching current must be located away from the PLL core.

— The PLL core must be shielded by guardring.

— If you do not use the PWRDN pin, connect it to VSS.

— For the FOUT pad, you can use a custom drive buffer or POT12_BB buffer considering the drive current.

Figure 6-3. The example of PLL block with SEC's XTAL-OSC (PSOSCM2)

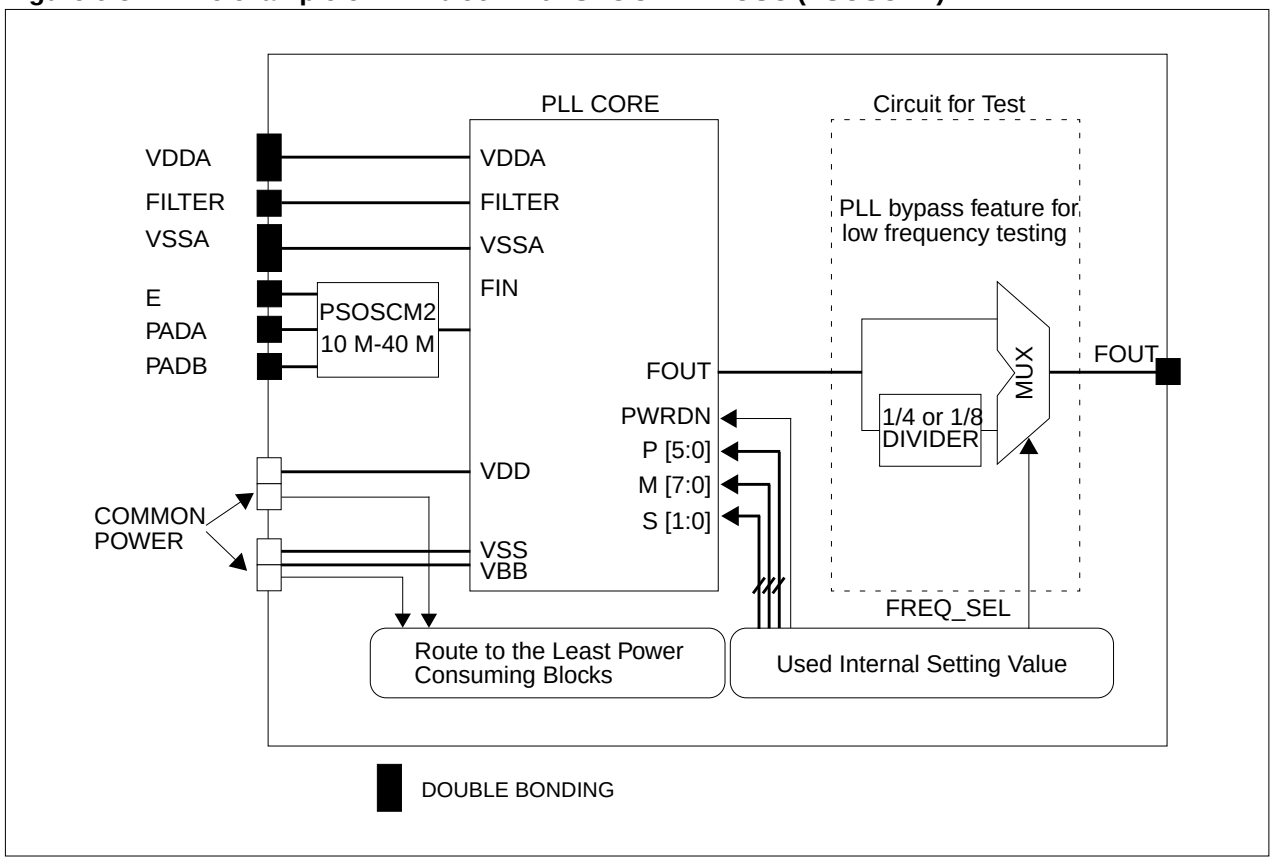
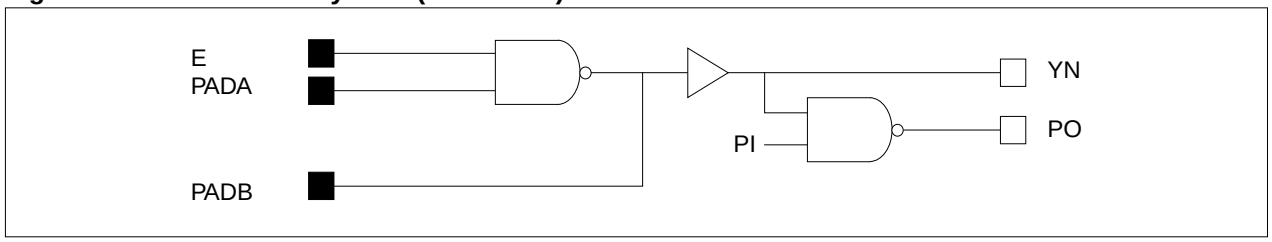


Figure 6-4. XTAL PAD Symbol (PSOSCM2)



— A special XTAL pad (PSOSCM2) for PLL is supported, refer chapter 4 for details.

— The XTAL must be located between PADA and PADB.
Enable pin (E) must be HIGH in normal operation.

— The operating frequency of PSOSCM2 is 10MHz-40MHz and the typical current consumption is 10.93mA

— PI pin must be connected to VDD, and the PO pin must be floated.

Test Chip

This 48 TSSOP package of the test chip has been fabricated for the PLL function test. Hence it is not provided to end-users as a discrete product.

No	Symbol	I/O	PAD NAME	Description
35-36	VDD	P	VDD	Digital power supply for FSPLL
33-34	VSS	G	VSS	Digital ground for FSPLL
13-14	VDDA	P	VDD	Analog power supply for FSPLL
11-12	VSSA	G	VSS	Analog ground for FSPLL
19-20	VBB	G	VSS	Bulk ground
15	XTALIN	I	PIA_BB	External clock input (14.3M) or crystal Input. If XTAL-OSC isn't used, the XTALIN is Fin.
16	XTALOUT	O	POA_BB	External crystal output. If a crystal is used, it is connected across the I/O pin XTALIN and XTALOUT. If XTAL-OSC isn't used the XTALOUT has to be floated.
17	FILTER	I	PIA_BB	A capacitor is connected between the pin and analog ground.
23	FOUT	O	POT12_BB	FSPLL clock output
18	PWRDN	I	PICC_BB	FSPLL clock power down (active high)
1-2, 45-48	P [5:0]	I	PICC_BB	The values for 6-bit programmable divider
37-44	M [7:0]	I	PICC_BB	The values for 8-bit programmable divider
31-32	S [1:0]	I	PICC_BB	The values for 2-bit programmable divider

Configuration

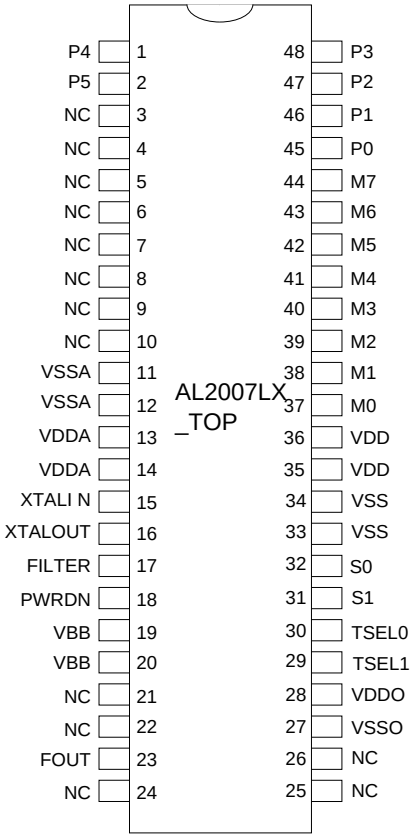


Figure 6-5. Pin Configurations

NOTES:

1. TSEL0, TSEL1, VDDO and VSSO pins are dummy, so they are not provided to the end-users.
2. NC is no connection pin.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	VDD, VDDA	3.15	3.3	3.45	V
Reference input frequency	XALIN (FIN), XTALOUT		14.318		MHz
External loop filter capacitance	FILTER		700		pF
Operating temperature	Top	0		70	°C

NOTE: It is strongly recommended that the supply pins (VDDA, VDD) be powered from the different sources.

Electrical DC Characteristics

(PLL Specifications: VDDA = VDD = 3.3V ± 5%, VSS = VSSA = VBB = 0V)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating voltage	VDD, VDDA	3.15	3.3	3.45	V
Dynamic current	Idd		12		mA
Power down current	Ipd		100		μA

Electrical AC Characteristics

(PLL Specifications: VDDA = VDD = 3.3V ± 5%, VSS = VSSA = VBB = 0V)

Characteristics	Symbol	Min	Typ	Max	Unit	Remarks
Output clock frequency	Fout	20		170	MHz	
Output clock duty	Rduty	40		60	%	
Settling time	Td		150		μs	
Cycle jitter	Tj		± 150		ps	

NOTE: All AC characteristics are simulation result data.

Functional Description

A PLL is the circuit synchronizing an output signal (generated by an VCO) with a reference or input signal in frequency as well as in phase.

In this application, it includes the following basic blocks.

— The voltage-controlled oscillator to generate the output frequency

— The divider P divides the input frequency by p

— The divider M divides the VCO output frequency by m

— The divider S divides the VCO output frequency by s

— The phase frequency detector detects the phase difference between the reference frequency and the output frequency (after division) and controls the charge pump voltage.

— The loop filter removes the high frequency components in charge pump voltage and gives smooth and clean control to VCO

The m, p, s values can be programmed by 16bit digital data from the external source. So the PLL can be locked in the desired frequency.

$$Fout = (m \times Fin) / (p \times s)$$

where

$Fin = 14.318MHz,\ m = M + 8,\ p = P + 2,\ s = 2^S$

Digital data format:

Main Divider	Pre Divider	Post Scaler
M7, M6, M5, M4, M3, M2, M1, M0	P5, P4, P3, P2, P1, P0	S1, S0

NOTES:

1. S1-S0: Output frequency scaler

2. M7-M0: VCO frequency divider

3. P5-P0: Input frequency divider

Frequency Synthesis

Frequency synthesis uses the system clock as a base frequency to generate higher/lower frequency clocks for internal logic.

For high speed applications in high-end designs, transmission line effects cause problems because of parasitics and impedance mismatch among various on-board components.

These problems can be eliminated by moving the high frequency to the chip level.

On-chip clocks that are faster than the external system clock can be synthesized by inserting a divider in the feedback path. The divider is placed after voltage controlled oscillator, as illustrated in Figure 6-1. The signal is running at M times the system clock frequency, so the PLL matches the divider signal output to the system clock. This configuration reduces the problem of interfacing to the system clock on the board, and it reduces the noise generated by the system clock oscillator and driver for all the components in the system.

Design Considerations

The following design considerations apply:

- Phase tolerance and jitter are independent of the PLL frequency.
- Jitter is affected by the noise frequency in the power (VDD/VSS, VDDA/VSSA, VBB). It increases when the noise level increases.
- A CMOS-level input reference clock is recommended for signal compatibility with the PLL circuit. Other levels such as TTL may degrade the tolerances.
- The used of two, or more PLLs requires special design considerations. Please consult your application engineer for more information.
- The following apply to the noise level, which can be minimized by using good analog power and ground isolation techniques in the system:
  - Use wide PCB traces for POWER (VDD/VSS, VDDA/VSSA) connections to the PLL core. Separate the traces from the chip's VDD/VSS, VDDA/VSSA supplies.
  - Use proper VDD/VSS, VDDA/VSSA de-coupling.
  - Use good power and ground sources on the board.
  - Use power VBB for minimize substrate noise
- The PLL core should be placed as close as possible to the dedicated loop filter and analog power and ground pins.
  - It is inadvisable to locate noise-generating signals, such as data buses and high-current outputs, near the PLL I/O cells.
- Other related I/O signals should be placed near the PLL I/O but do not have any pre-defined placement restriction.

General Description

The AL2007LA is a Phase-Locked Loop (PLL) frequency synthesizer constructed in CMOS on single monolithic structure.

The PLL macrofunctions provide frequency multiplication capabilities.

The output clock frequency is related to the input clock frequency Fin by the following equation:

Fout = (m x Fin) / (p x s).

where

Fout is the output clock frequency.
Fin is the input clock frequency.
m, p and s are the values for programmable dividers.

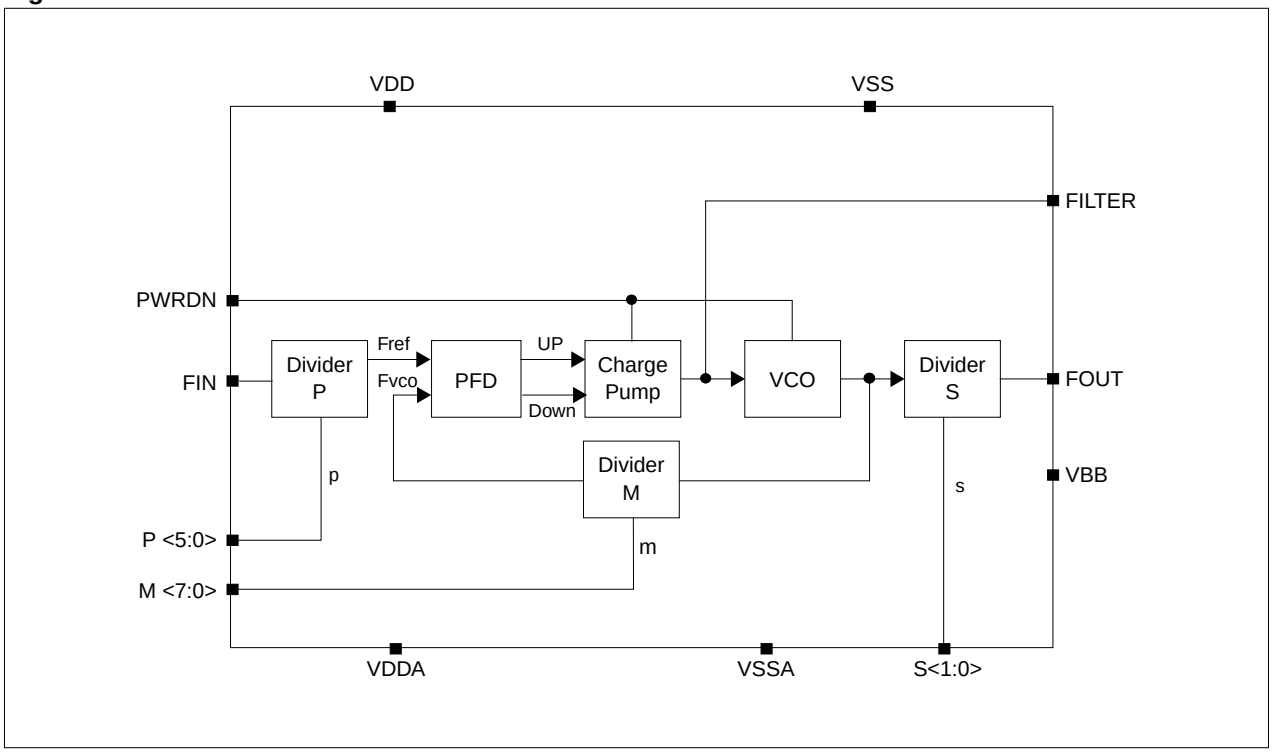
AL2007LA consists of a Phase/Frequency Detector (PFD), a Charge Pump, an External Loop Filter, a Voltage Controlled Oscillator (VCO), a 6-bit pre-divider, an 8-bit main divider and a 2-bit post scaler as shown in Figure 6-6.

Features

- 0.35μm CMOS device technology
- 3.3V single power supply
- Output frequency range: 20-170MHz
- Input frequency range: 10-40MHz
- Jitter: ±150ps
- Duty ratio: 40% to 60%
- Frequency changed by programmable dividers
- Power down mode

Block Diagram

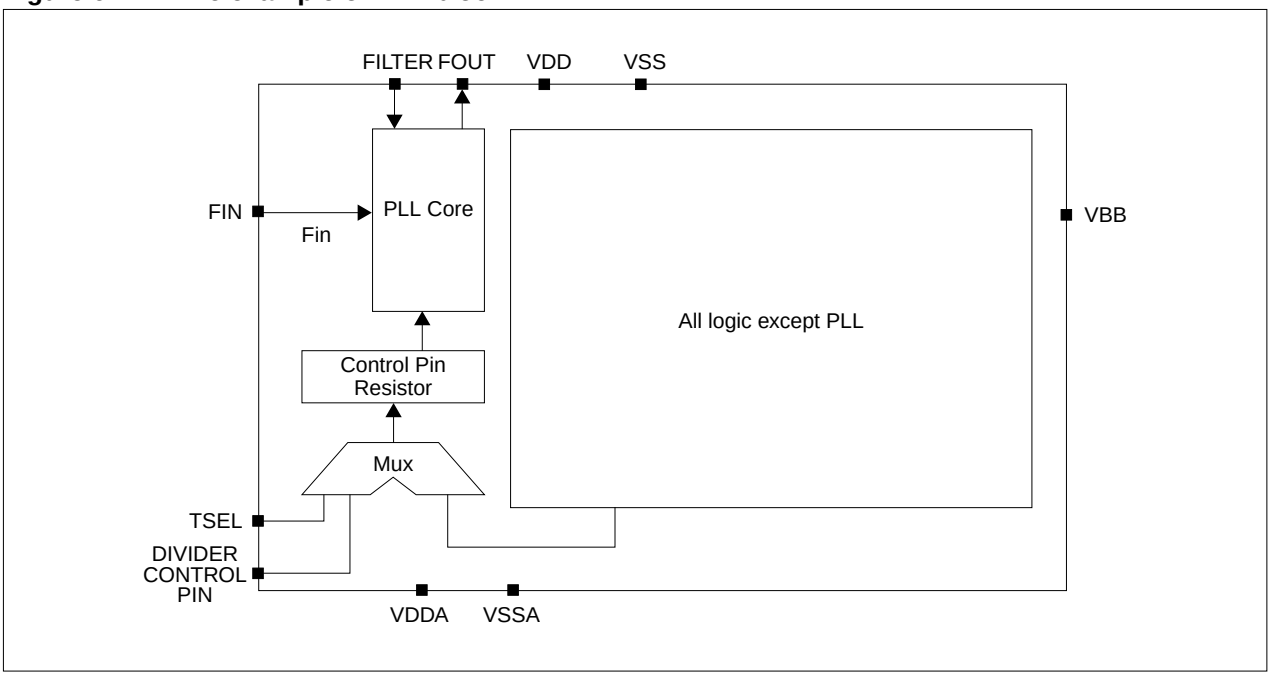
Figure 6-6. AL2007LA PLL Core



Pin Description

Pin Name	I/O	Description
VDD	P	Digital power supply for FSPLL
VSS	G	Digital ground for FSPLL
VDDA	P	Analog power supply for FSPLL
VSSA	G	Analog ground for FSPLL
VBB	G	Bulk ground
FIN	I	External clock input
FILTER	I	A capacitor is connected between the pin and analog ground.
FOUT	O	FSPLL clock output
PWRDN	I	FSPLL clock power down (active high)
P [5:0]	I	The values for 6-bit programmable divider
M [7:0]	I	The values for 8-bit programmable divider
S [1:0]	I	The values for 2-bit programmable divider

Figure 6-7. The example of PLL block



THE USAGE OF AL2007LA PLL CORE

— When implementing an embedded PLL block, the following pins must be bypassed externally for testing the PLL locking function:

  FIN, FILTER, FOUT, VDDA, VSSA, VDD, VSS and VBB

— In case of self test logic, the divider control pins (P, M, S) and the TSEL pin must be bypassed externally for testing.

— The digital power (VDD, VSS), the analog power (VDDA, VSSA) and the bulk power must be dedicated to the PLL only and separated. If the dedicated VDD and VSS is not allowed that of the least power consuming block are shared with the PLL as shown in Figure 6-8.

— The PIA_BB pad is used as a FILTER pad that contains only ESD protection diodes without any resisters and buffers.

— The FOUT and FILTER pins must be placed far from the internal signals in order to avoid overlapping the signal lines.

— The blocks having a large digital switching current must be located away from the PLL core.

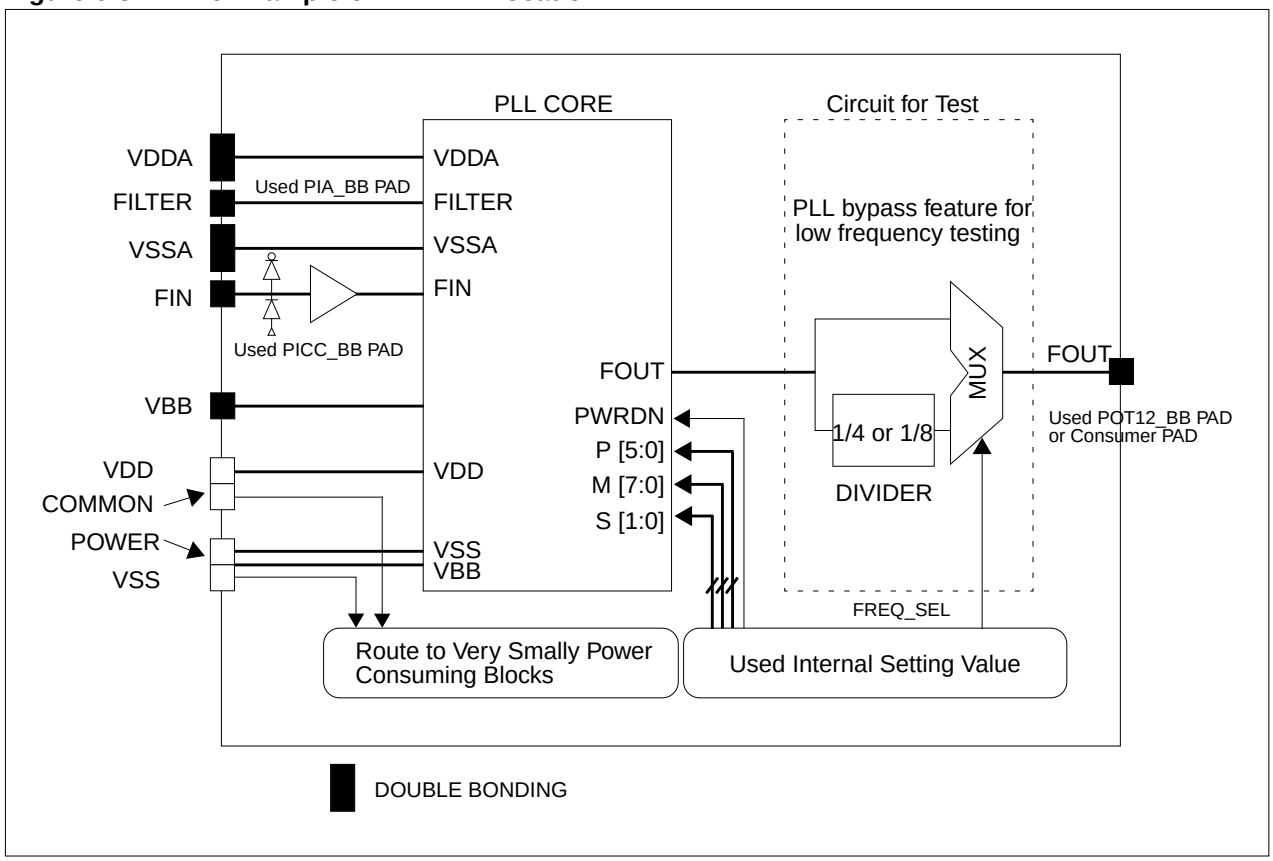
— An FIN input buffer with high slew rate is preferred because the smaller the buffer delay, the smaller the clock skew between the external source clock and PLL generated clock.

— The PLL core must be shielded by guardring.

— If you do not use the PWRDN pin, connect it to VSS.

— For FOUT pad you can use a custom drive buffer or POT12_BB buffer considering the drive current.

Figure 6-8. The Example of PLL Pin Location



Test Chip

This 48 TSSOP package of the test chip has been fabricated for the PLL function test. Hence it is not provided to end-users as a discrete product.

No	Symbol	I/O	PAD NAME	Description
35-36	VDD	P	VDD	Digital power supply for FSPLL
33-34	VSS	G	VSS	Digital ground for FSPLL
13-14	VDDA	P	VDD	Analog power supply for FSPLL
11-12	VSSA	G	VSS	Analog ground for FSPLL
19-20	VBB	G	VSS	Bulk ground
15	FIN	I	PICC_BB	FSPLL clock input
17	FILTER	I	PIA_BB	A capacitor is connected between the pin and analog ground.
23	FOUT	O	POT12_BB	FSPLL clock output
18	PWRDN	I	PICC_BB	FSPLL clock power down (active high)
1-2, 45-48	P [5:0]	I	PICC_BB	The values for 6-bit programmable divider
37-44	M [7:0]	I	PICC_BB	The values for 8-bit programmable divider
31-32	S [1:0]	I	PICC_BB	The values for 2-bit programmable divider

Configuration

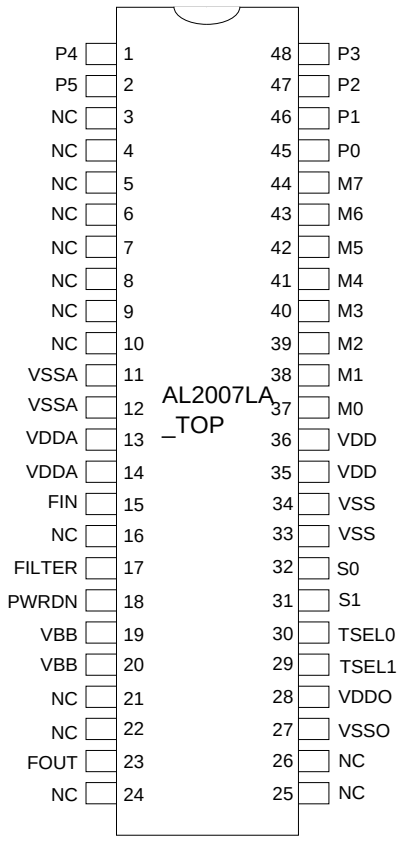


Figure 6-9. Pin Configurations

NOTES:

1. TSEL0, TSEL1, VDDO and VSSO pins are dummy, so they are not provided to the end-users.

2. NC is no connection pin.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	VDD, VDDA	3.15	3.3	3.45	V
Reference input frequency	XALIN (FIN), XTALOUT		14.318		MHz
External loop filter capacitance	FILTER		700		pF
Operating temperature	Top	0		70	°C

NOTE: It is strongly recommended that the supply pins (VDDA, VDD) be powered from the different sources.

Electrical DC Characteristics

(PLL Specifications: VDDA = VDD = 3.3V ± 5%, VSS = VSSA = VBB = 0V)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating voltage	VDD, VDDA	3.15	3.3	3.45	V
Dynamic current	Idd		5		mA
Power down current	Ipd		100		µA

Electrical AC Characteristics

(PLL Specifications: VDDA = VDD = 3.3V ± 5%, VSS = VSSA = VBB = 0V)

Characteristics	Symbol	Min	Typ	Max	Unit	Remarks
Output clock frequency	Fout	20		170	MHz	
Output clock duty	Rduty	40	50	60	%	
Settling time	Td		150		µs	
Cycle jitter	Tj		±150		ps	

NOTE: All AC characteristics are simulation result data.

Functional Description

A PLL is the circuit synchronizing an output signal (generated by an VCO) with a reference or input signal in frequency as well as in phase.

In this application, it includes the following basic blocks.

— The voltage-controlled oscillator to generate the output frequency

— The divider P divides the reference frequency by p

— The divider M divides the VCO output frequency by m

— The divider S divides the VCO output frequency by s

— The phase frequency detector detects the phase difference between the reference frequency and the output frequency (after division) and controls the charge pump voltage.

— The loop filter removes the high frequency components in charge pump voltage and gives smooth and clean control to VCO

The m, p, s values can be programmed by 16bit digital data from the external source. So the PLL can be locked in the desired frequency.

$$Fout = (m \times Fin) / (p \times s)$$

where

$Fin = 14.318MHz,\ m = M + 8,\ p = P + 2,\ s = 2^S$

Digital data format:

Main Divider	Pre Divider	Post Scaler
M7, M6, M5, M4, M3, M2, M1, M0	P5, P4, P3, P2, P1, P0	S1, S0

NOTES:

1. S1-S0: Output frequency scaler

2. M7-M0: VCO frequency divider

3. P5-P0: Input frequency divider

Frequency Synthesis

Frequency synthesis uses the system clock as a base frequency to generate higher/lower frequency clocks for internal logic.

For high speed applications in high-end designs, transmission line effects cause problems because of parasitics and impedance mismatch among various on-board components.

These problems can be eliminated by moving the high frequency to the chip level.

On-chip clocks that are faster than the external system clock can be synthesized by inserting a divider in the feedback path. The divider is placed after voltage controlled oscillator, as illustrated in Figure 6-6. The signal is running at M times the system clock frequency, so the PLL matches the divider signal output to the system clock. This configuration reduces the problem of interfacing to the system clock on the board, and it reduces the noise generated by the system clock oscillator and driver for all the components in the system.

Design Considerations

The following design considerations apply:

- Phase tolerance and jitter are independent of the PLL frequency.
- Jitter is affected by the noise frequency in the power (VDD/VSS, VDDA/VSSA, VBB). It increases when the noise level increases.
- A CMOS-level input reference clock is recommended for signal compatibility with the PLL circuit. Other levels such as TTL may degrade the tolerances.
- The used of two, or more PLLs requires special design considerations. Please consult your application engineer for more information.
- The following apply to the noise level, which can be minimized by using good analog power and ground isolation techniques in the system:
  - Use wide PCB traces for POWER (VDD/VSS, VDDA/VSSA) connections to the PLL core. Separate the traces from the chip's VDD/VSS, VDDA/VSSA supplies.
  - Use proper VDD/VSS, VDDA/VSSA de-coupling.
  - Use good power and ground sources on the board.
  - Use power VBB for minimize substrate noise
- The PLL core should be placed as close as possible to the dedicated loop filter and analog power and ground pins.
  - It is inadvisable to locate noise-generating signals, such as data buses and high-current outputs, near the PLL I/O cells.
- Other related I/O signals should be placed near the PLL I/O but do not have any pre-defined placement restriction.