The Next Chip Challenge: Effective Methods for Viable Mixed Technology SoCs

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Abstract

The next generation of computer chips will continue the trend for more complexity than their predecessors. Many of them will contain different chip technologies and are termed SoCs (System on a Chip). They present to the process community, the system and circuit communities, as well as to the design and test communities major new challenges. On the other hand they also offer at the same time also new opportunities!. For one, the desire to bring more functionality onto a single chip tends to require additional processing, which in turn results in various degrees of device compromises. The chips will also tend to become larger due to the added device content, and this generally will impact the yieldability of the final chip. And such chips will require potentially new approaches to validate the intended design performances. Chip sector reuse must also be brought into the discussion and wherever possible into practice. The net effect implies higher chip costs. Much of the industry's efforts are therefore focused in addressing these challenges; however, so far, not yet very successfully. The alternative has been to continue in the placement of chips onto substrate modules. Yet, this solution creates practical limits on achievable wiring densities and bandwidth, due to the spacing requirements of the C4 interconnection. Furthermore, every C4 joint is associated with a signal delay of about 50 psec. All of these handicaps would potentially benefit greatly from new SoC methods, starting with the fabrication methodology and extending it into the chip design and test areas.

Such a direction has been set in motion. The opportunity for a uniquely new chip fabrication method has emerged by combining a set of somewhat diverse processes. It is based on a judicious selection of process elements from the traditional chip area and combined with those of a somewhat more recent chip packaging process methodology. This approach results in overcoming simultaneously all of the key current process limitations as experienced with today's SoC chip designs, as well as eliminates certain chip packaging technology handicaps. Yet, it does not require the need for new process tooling. It relies on currently existing process tooling and process methodologies.

This new process direction has been found to be quite applicable to a number of desirable SoC device designs, and offers new opportunities for yet another expansion of the current semiconductor technology base over the next few years. However, effective SoC designs and fabrications require a much closer and earlier collaboration between the process, design and test communities.

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DAC 2002, June 10-14, 2002, New Orleans, Louisiana, USA.
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General Terms: Design

Key Words: SoCs (System on a Chip); Chip Fabrication methods; Chip/Packing integration; Chip Subsector concepts

Introduction

Electronic devices are continuing to become more and more complex with each new generation, while at the same time their respective device elements are becoming smaller and smaller. This environment of device crowding and complexity continues to generate major challenges – not only for the chip process community, but also for the packaging technologist. The latter is continuously being challenged for his ability to keep up with a pace that is commensurate with the rapidly changing advances of the chip sectors. The packaging sector has clearly been for a number of years the primary restraint for further maximizing the potential system speeds of many semiconductor chip technologies. Whereas the wiring density at the chip level is in the "micron" regime, the wiring density in the package remains in the "mils" regime. To minimize the impact as much as possible, current high performance package substrates consist of a combination of many inter-level metal and insulator layers. Yet, even these complex packages are not sufficient to effectively accommodate the needs for today's high performance chips, much less so future chips.

However, new challenges are also being confronted by the device technologist, due to the fact that there is a general desire by the system designers to have more and more device capabilities on a single chip. This implies at least two major directions: larger chips containing more content, while at the same time intermixing more diverse chip technologies. Both have a strong influence on the overall yields of such chips, and in turn, on the ultimate fabrication costs. Large chips do not yield very well, and complex multi-technology chips require much more processing, and thereby also influencing the potential chip yields. And in fact, some multi-technology chips are not possible to be fabricated with today's traditional chip process capabilities because of general incompatible material

properties. Furthermore, the need to test these types of mixed technology chips require new characterization methods and test procedures.

This general environment has therefore spawned a great deal of new thinking in terms of finding process alternatives to overcome some of these limitations. But the process remains somewhat sequential. That is, only after the process community has verified the ability to fabricate some of these new chips, the chip and system designers begin to consider them into their application space. And yet later, the test organizations scurry to find means for effective test methodologies.

Traditionally, the multi-layer ceramic (MLC) package has been used to package different type of technology chips on a common substrate. This allows for individual chip testing prior to packaging those chips. But the wiring density limitations of the C4 technology in such packages do create major barriers for advanced high performance devices. This environment would greatly benefit from new and innovative chip fabrication directions. One such recent direction has been a widening interest in stacked chips and 3D type chips. The latter is based on vertical interconnections through one chip in order to reach another. This work has been going on in several research laboratories for the past 5 - 7 years (1-3); yet, to date, no one has published definitive device results actually verifying the theoretical benefits. Such concepts have a number of major handicaps for which solutions have not been brought forward. One major hurdle is the inefficient removal of heat generated by any high performing set of chips stacked on top of each other. An alternative proposal is the concept of Si interposers serving as intermediates between the chip and the package. However, such interposer is not cheap to fabricate, since it requires extensive deep RIE etching for forming high aspect ratio vias, as well as subsequent filling of these deep vias. Furthermore, do they really serve as an effective solution, which could alternatively be achieved with simpler structures, such as thin film wiring? Again, the concept of interposers has been around for a number of years (4,5), but the actual use of them in any product seems to remain absent.

For the past few years, there has also been an increased interest in the creation of more innovative new packages to achieve closer chip-to-chip interconnection opportunities. GE's HDI (6-8) is one such example. The original concept is based on placing chips into substrate cavities, filling in the spaces surrounding the chips, and subsequently locating the positions of the chips and interconnecting them with some wiring technique. Quite a few process refinements have been made by GE's researchers over the years, but this initiative has not yet enjoyed any industry wide acceptance. More recently, slightly similar work was published by the research group at the Frauenhofer Institute in Berlin (9). Other approaches for more closely interconnecting chips to each other tend to be based on some version of C4 flip chip technology serving as the interconnect elements. However, the available C4 dimensions tend to place a practical limit on the possible wiring densities. Furthermore, each such C4 represents a signal delay of as much as 50 psec, so that every chip-to-chip interconnect will incur a total delay of about 100 psec. Since many advanced chip designs depend on about 30% of the total C4s for interconnections, the total delay budget for many chip designs, due to interconnects, can become significant.

As we therefore attempt to reach out into the future, what will the challenges and the potential solutions be which would further the impressive successes of the past? The evolutionary progress has been mapped out with some degree of certainty (i.e., the SIA roadmap). And it points to a number of roadblocks! However, looking back into the past, it becomes somewhat obvious that many of the technology breakthroughs are not the result of such evolutionary thinking, but rather relate to the introduction of more revolutionary approaches creating new process opportunities. The evolutionary forces are always active, and some level of progress will be made. On the other hand, revolutionary progress is less clearly defined in terms of a timetable or impact, but it will more than likely be elements of such innovations, which offer new directions and opportunities for further technology advances.

In the future, mobile systems are anticipated to predominate the semiconductor chip sector. This will bring additional pressures on improved chip packages; that is, lighter and smaller . Will entirely new packages be required, and can they be realized with simply evolutionary thinking? Or would this environment benefit for the chip sector to partner with the packaging sector by creating some level of technology marriage?

The T&J chip/package concept to create effective SoCs

The net chip content of many future chips seems to lie in the realm of SoCs, although there is some debate whether it may be SoPs (System-on-a-package). Viewing either version from the viewpoint of their respective traditional definitions, each of them has specific advantages and disadvantages. But by taking a new process approach - the concept of the T&J (Transfer & Joining) chip/package methodology – these respective handicaps are minimized, while maintaining and capitalizing on their respective collective advantages. Hence, it is possible to realize an effective SoC product, which does retain its inherent advantages; yet, incorporates the advantageous elements of an SoP structures. In essence, the T&J concepts migrates elements, traditionally done in the Thin Film sector of the Packaging house into the S/C house (Fig. 1).

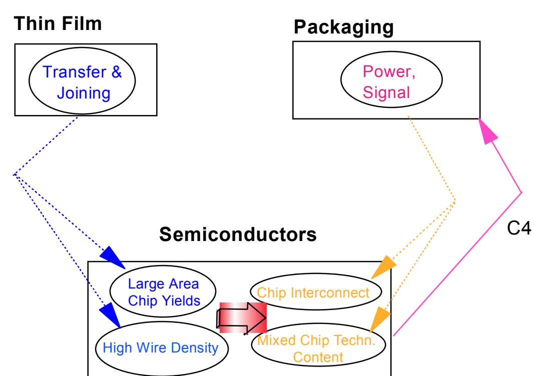

Figure 1. Technology Merging/Bridging

The T&J methodology relies on the initial fabrication of an interconnect wiring/insulator film structure on a glass wafer or plate; placing, attaching and bonding chips and/or full wafers to that metal interconnect structure; and subsequently removing the

glass wafer or plate. This process sequence leaves behind the interconnect wiring tying together the attached and bonded chips and/or wafer as is shown in Fig 2.

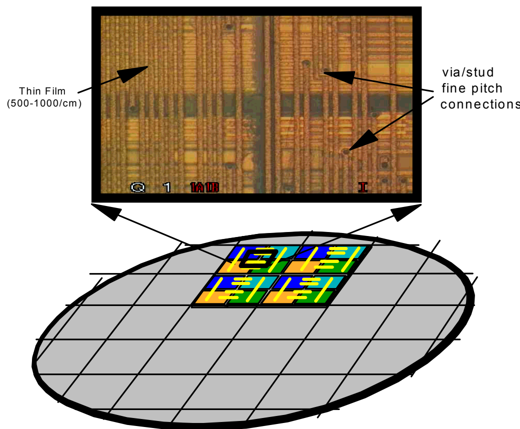

Figure 2. The S&T Generated SoC

In essence, the chip-to-chip interconnections, which previously relied on C4s, have been replaced by thin film wiring elements. The methodology allows for much higher wiring densities (up to a factor of 100) in comparison to C4s. This can have a major positive impact on the net device bandwidth. It also allows for chip-to-chip placements as close as about 25 - 60 um, as opposed to the typical 3 mm spacing of C4 based chip placements. Furthermore, the chip/wafer placement accuracies are well within1um. An additional major advantage of this fabrication methodology is the ability for parallel processing of all the parts and a minimal heat budget, the latter of which consists of only the bonding process itself. This alleviates the reliance on round wafers. In fact, it is preferable and desirable to utilize rectangular plate formats to minimize edge wafer losses.

The T&J concept also results in the ability to form large SoC chips from sub-sector (macros) parts, which (because of their respective processing) can also optimized. These will inherently be smaller chips and therefore offer much higher yields than a comparable monolith large chip. And of course the methodology allows for very diverse mixed chip content within an SoC chip.

Experimental

The T&J fabrication methodology can be done in existing manufacturing tools. Silicon chips were derived from 200 mm wafers. Chip placements were done on either 125 mm square glass plates or round 200 mm glass wafers. Most of the experimental data are based on the use of a single metal film on a silicon wafer added to the top of the normal BEOL (back end of the line) film structure, and a single metal film on the glass support plate and/or wafer, although this is not a limiting factor. Appropriate via and stud structures were generated to create the vertical interconnect bonding between the two metal film layers. A laser method was utilized for the removal of the glass plate and/or wafer from the metal interconnect structure. Different test vehicles were used to assess the various process elements.

Discussion

The T&J process is based on the attachment of chips to existing interconnect wiring separately fabricated on a supporting glass wafer (plate), which itself is only a temporary support for the interconnect wiring. The device chips are terminated with a appropriate insulating adhesive and patterns with via openings. In parallel, the interconnect wiring is built up on the glass wafer (plate), the number of layers being dictated by the specific device and SoC design requirements. The upper level of this interconnection wiring is terminated with an appropriate pattern of metal studs which mirror the via pattern on the device chips. Since the glass wafer serves as the receiver of the chips and/or full wafer, a single mask creating the stud pattern dictates all of the placement positioning for the vias on the chips. This allows for very precise chip positioning and chip-to-chip interconnections. After chip placement, the combined structure is heated to facilitate the full bonding of the chips to the interconnection studs. Chip positioning can be monitored through the glass wafer. See Fig. 3.

After proper bonding, the back sides of the attached chips are planarized and given a backside support with the use of a simple silicon wafer. After this, the glass wafer is removed with a laser ablation technique to leave behind the metal interconnect layers tightly bonded to the chips. The resulting metal interconnects and interconnected chip set structure is now ready to be appropriately diced and further processed for subsequent packaging needs However, it should be pointed out that in this instance the chip-to-chip interconnection already exist, leaving

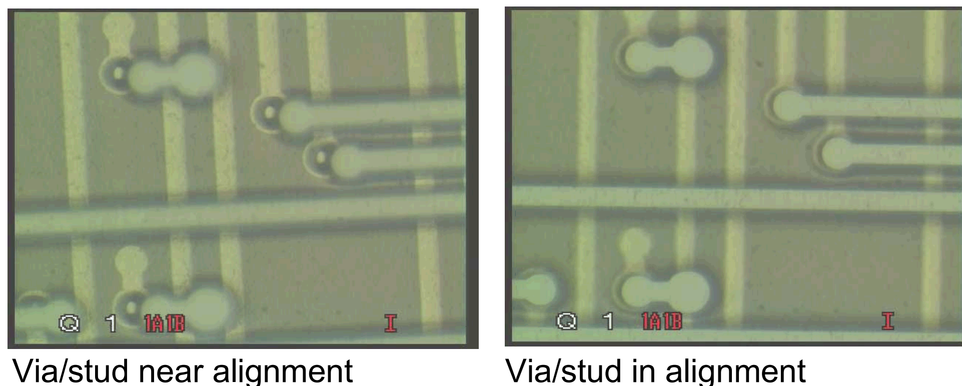

Figure 3. Via/Stud Alignment of Interconnect Wiring layers

only the need for power and signal from the package., and thus much fewer total C4s.

It should also be pointed out that with the T&J concept of fabricating the various chip macro sectors in parallel, the device and circuit design community must realize that the interconnect hierarchy needs to be carefully laid out. In today's large area SoCs, some of the interconnect wiring may be placed at some lower metal level because of either convenience or available space. However, for effective multi-technology chip content SoCs, this interconnect wiring should be brought up to a common set of metal layers. This allows for better testing and diagnostic capabilities, more efficient yield learning of the individual chip sub-sectors, and easier reuse of chip sectors for different designs.

Electrical data was generated for these types of via/stud interconnections to verify not only the ease of fabrication, but also the quality of the electrical interconnect structures. A key process element in the T&J process concept relates to the transferred wiring structure and its integrity when crossing the open gaps between chips which will exist between the attached chips. This is shown in Fig. 4 for different wiring dimensions and compared to similar control structures placed simultaneously on adjacent flat surfaces. No differences are evident. A spacing of 60 um does therefore not create any concerns and can be easily crossed.

Conclusion

The T&J process methodology is a very viable means for achieving true SoC chips without their traditional respective handicaps. That is, true SoCs allow for an effective mixturing of diverse technology chips into a single chip format. By appropriate and selective use of the available building blocks, which exist in both the Package (in this instance, within their Thin Film sector) and the S/C houses, it is possible to create multi-functional chips into a single SoC format. Alternatively, large SoC chips can be fabricated with this technique, and these need not be shackled by the typical yield handicaps associated with large area chips. However, it is important to point out, that it is not entirely feasible to simply take a large chip, section it into smaller ones, and then rebuild the chip back up into a large chip via the T&J method. Physically, this is possible; however, practically the breakage of already existing circuit design needs to be considered from the beginning, not as an afterthought or as a possible remedy for an existing chip yield crisis. In fact, as has often been pointed out in the recent literature, large area chips need the cooperative collaboration between the system, the circuit, the test, and the process engineer from the start of the device desig cycle. This collaboration should also be fostered for any mixed chip designs, since the overall result may be significantly improved, or may even be made much more viable, through such efforts.

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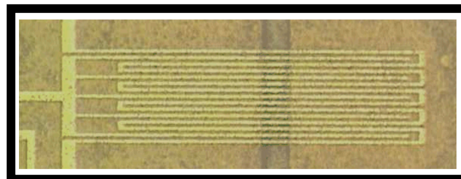

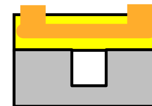

Gap crossing	25um	20um	15um	10um	5um
# of crossings	480	480	720	720	720
Yield	100%	100%	100%	100%	100%
Resistance (Ω)	4.254	3.725	3.977	5.328	10.47

Surface crossing	25um	20um	15um	10um	5um
# of crossings	240	240	360	360	360
yield	100%	100%	100%	100%	100%
Resistance (Ω)	4.314	3.323	4.566	5.580	10.37

Figure 4. Electrical Data for T&J Interconnect Wiring