Sequential Design Basics

Lecture 2 topics

- A review of devices that hold state
  - A review of Latches
  - A review of Flip-Flops

- Unit 11 of text
  - Set-Reset Latch/Flip-Flops/D latch/ Edge triggered D Flip-Flop

Latches and Flip-Flops

- What is the difference?
  - Flip-flops use a clock and are clock edge triggered
    - When the clock edge occurs the data on the data inputs determines the next state of the flip-flop
  - Latches are level sensitive
    - Use a clock, and when the clock (or enable) is active the output of the latch follows the data input.
    - Latches are very common in VLSI circuits. (Used as they require fewer transistors.)

The basis

- **How do you design logic that holds state**?
- Individual logic gates are feed forward devices who's output depends on the value of the inputs to that device.
- So how to create a device that holds a state?

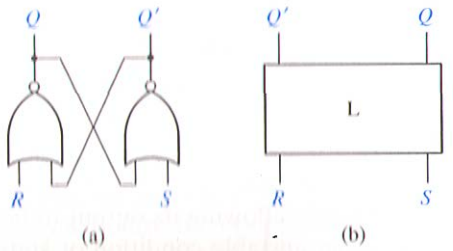
The basis

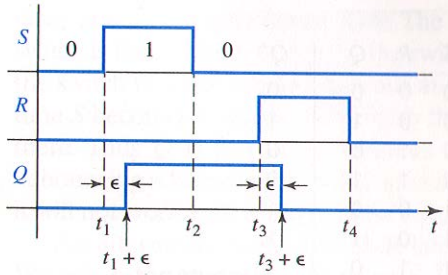
- **How do you design logic that holds state**?
- Individual logic gates are feed forward devices who's output depends on the value of the inputs to that device.
- So how to create a device that holds a state?
  - **FEEDBACK!!!**

The Set-Reset (SR) Latch

- The circuit has no memory
  - Output depends not only on present inputs and the state of the latch when the current inputs were applied.
- The state 1 1 on the inputs is not allowed. Why?

FIGURE 11-5
S-R Latch

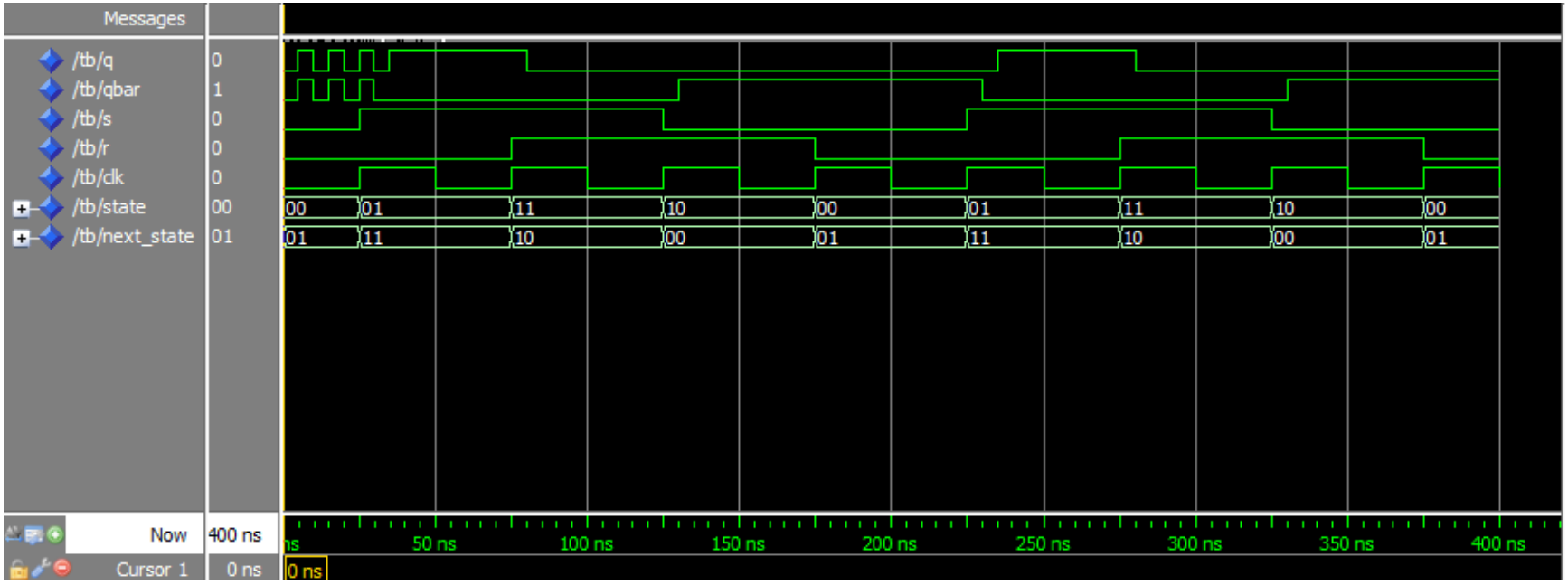




HDL code for SR Latch

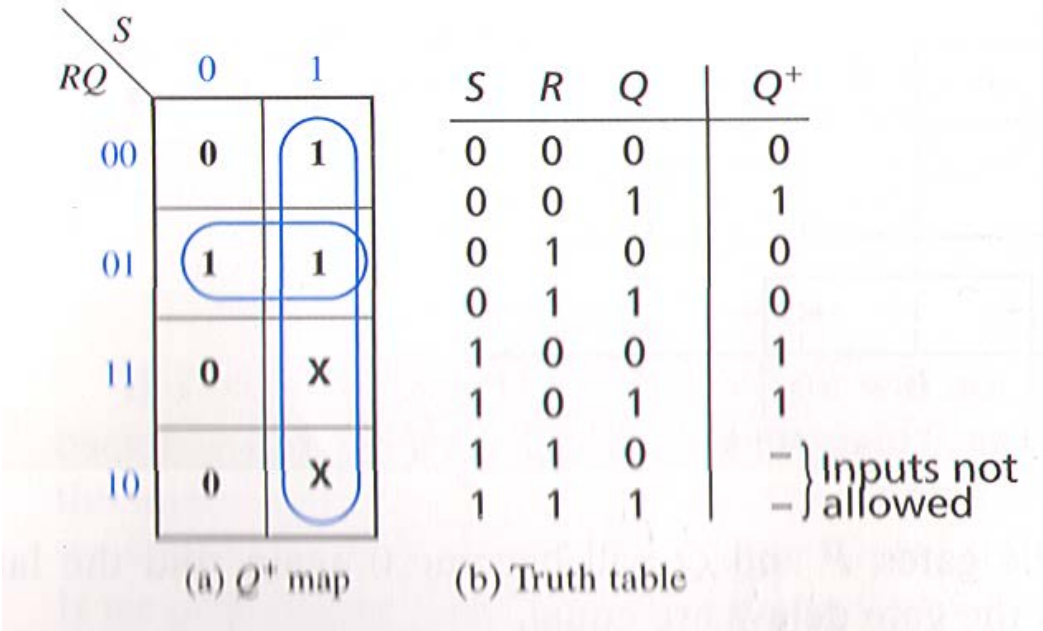
- The core of the model
  - --set up dataflow for SR latch
  - Q <= R NOR Qbar AFTER 5 ns;
  - Qbar <= S NOR Q AFTER 5 ns;
- Apply stimulus to S and R
  - What does simulation show

HDL simulation of SR latch



The next state

- The state 11 is not allowed
- S=1 Q to 1
- R=1 Q to 0
- S and R 00
  - Hold state



RQ \ S	0	1
00	0	1
01	1	1
11	0	X
10	0	X

(a) Q^+ map

S	R	Q	Q^+	
0	0	0	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	–	Inputs not allowed
1	1	1	–	

(b) Truth table

Next state truth table

- From the table you can get the next state equation
  - Here – $Q^+ = S + R'Q$

- An equation that expresses the state of a latch (or flip flop) in terms of its present state and inputs is referred to as the *characteristic equation.*

The D Latch

- The D Latch is the most common element in CMOS design.

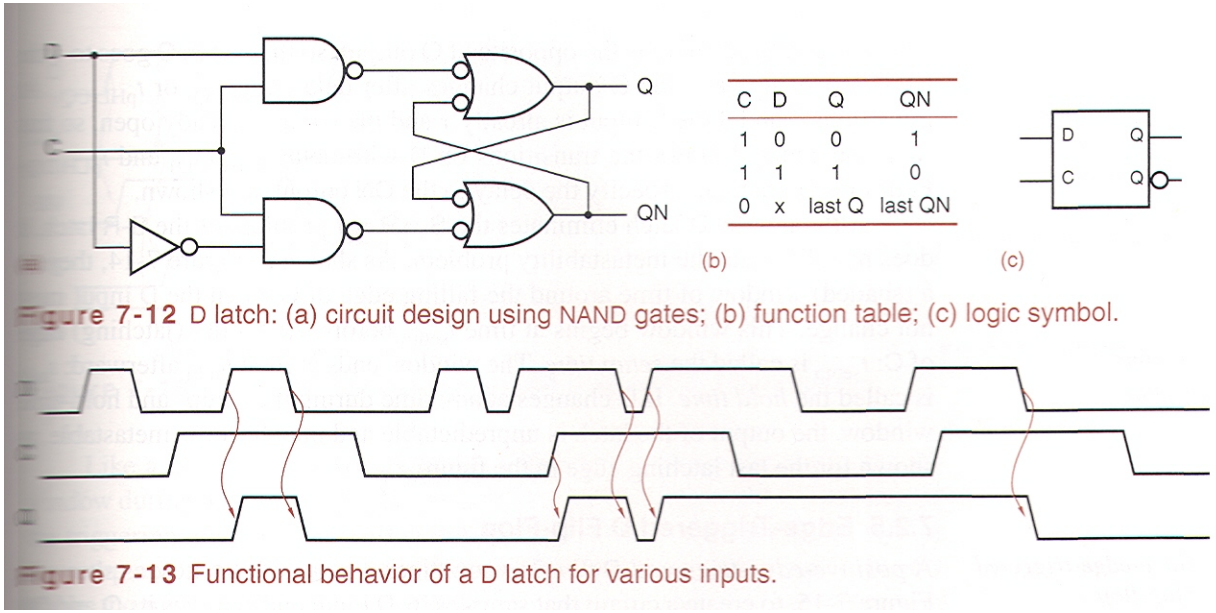
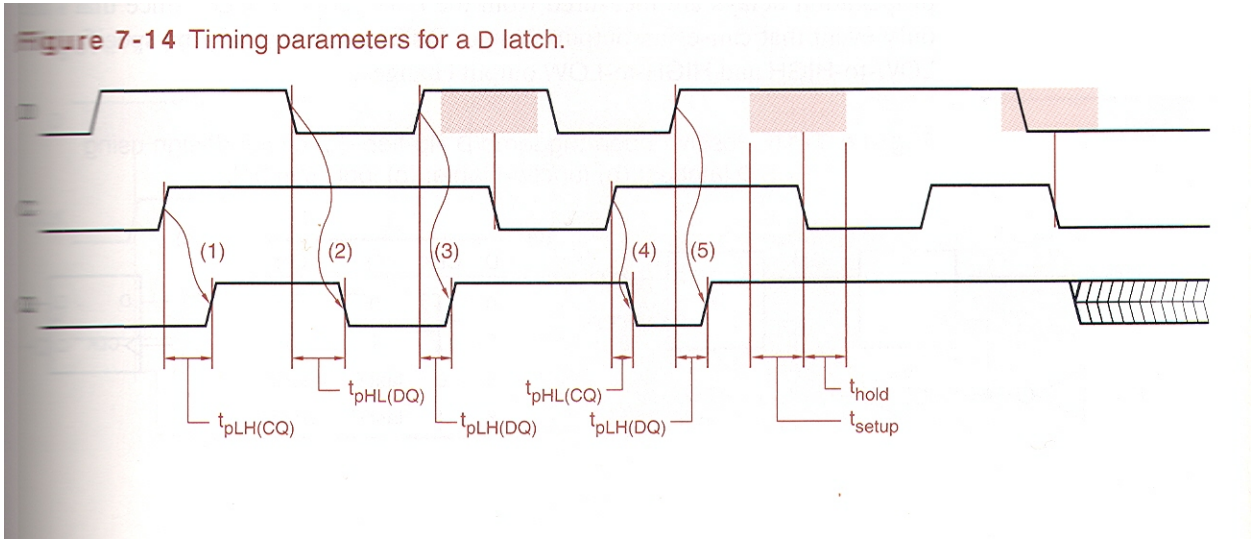


Figure 7-12 D latch: (a) circuit design using NAND gates; (b) function table; (c) logic symbol.

Figure 7-13 Functional behavior of a D latch for various inputs.

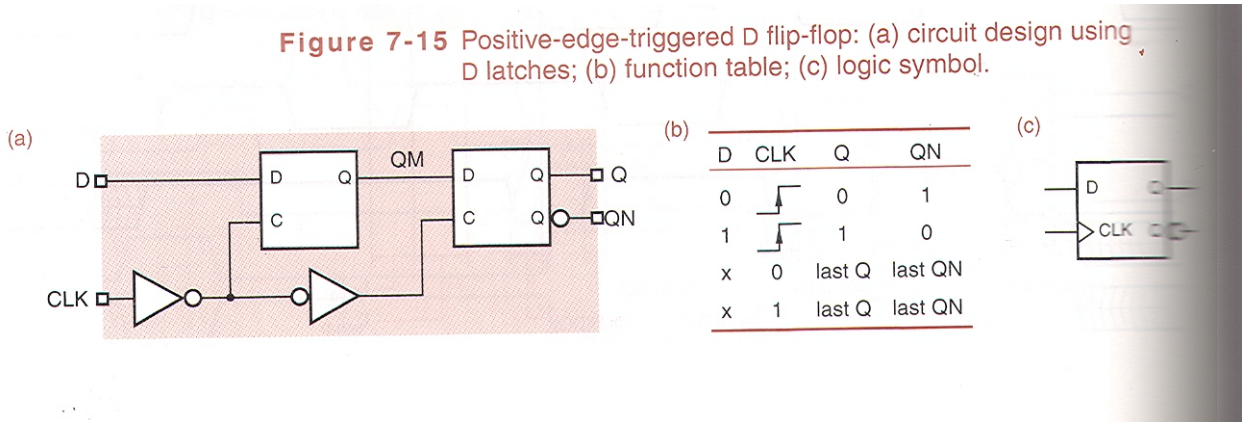
Timing diagram for a D Latch



The D F/F

- The D Flip-Flop has edge triggered operation
- Can be positive edge triggered (as here) or negative edge triggered

Figure 7-15 Positive-edge-triggered D flip-flop: (a) circuit design using D latches; (b) function table; (c) logic symbol.



D	CLK	Q	QN
0	↑	0	1
1	↑	1	0
x	0	last Q	last QN
x	1	last Q	last QN

Timing for a D Flip-Flop

- Important to note relationships

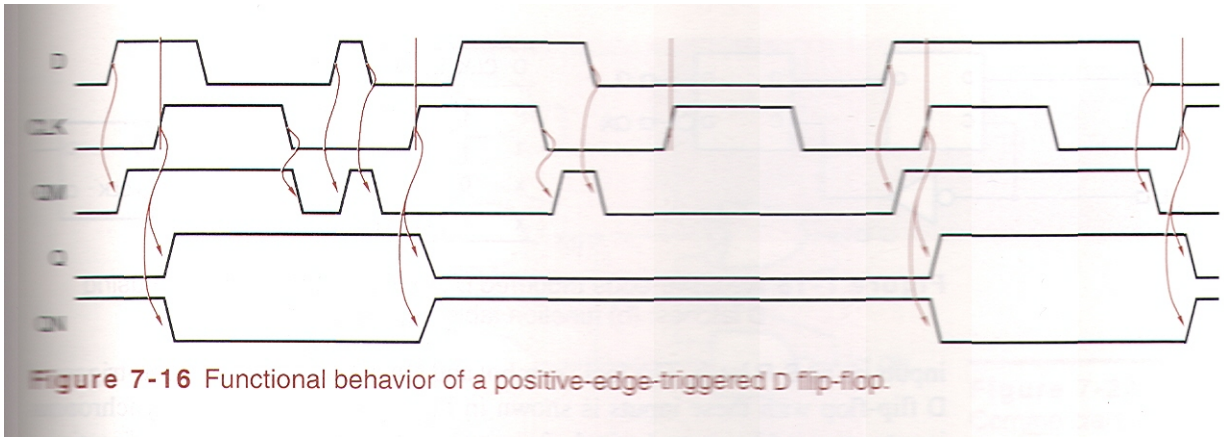
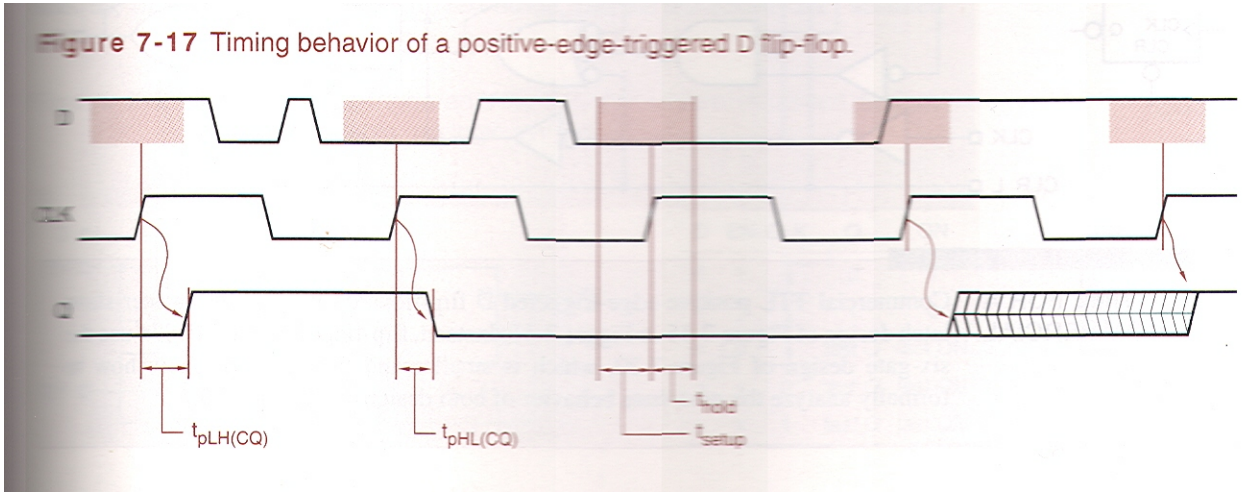


Figure 7-16 Functional behavior of a positive-edge-triggered D flip-flop.

D F/F Behavior

- Some important timing parameters
  - Clock to output
  - Setup and hold time



D F/F with Preset and Clear

- Can add preset and clear for easier circuit initialization.

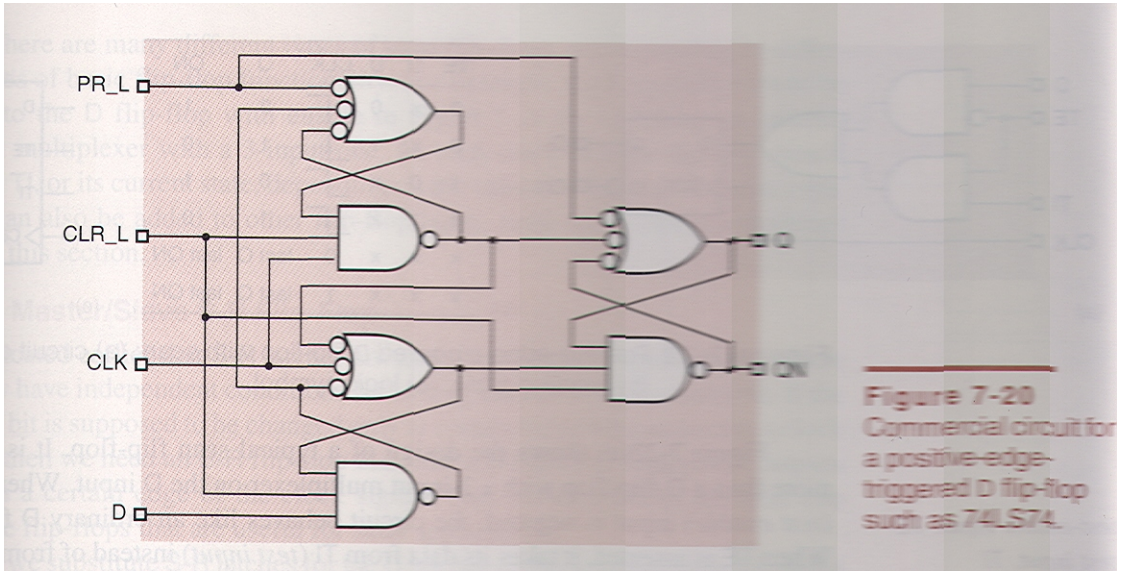


Figure 7-20
Commercial circuit for a positive-edge-triggered D flip-flop such as 74LS74.

Scan Chains

- D F/F is the F/F used in scan chains.

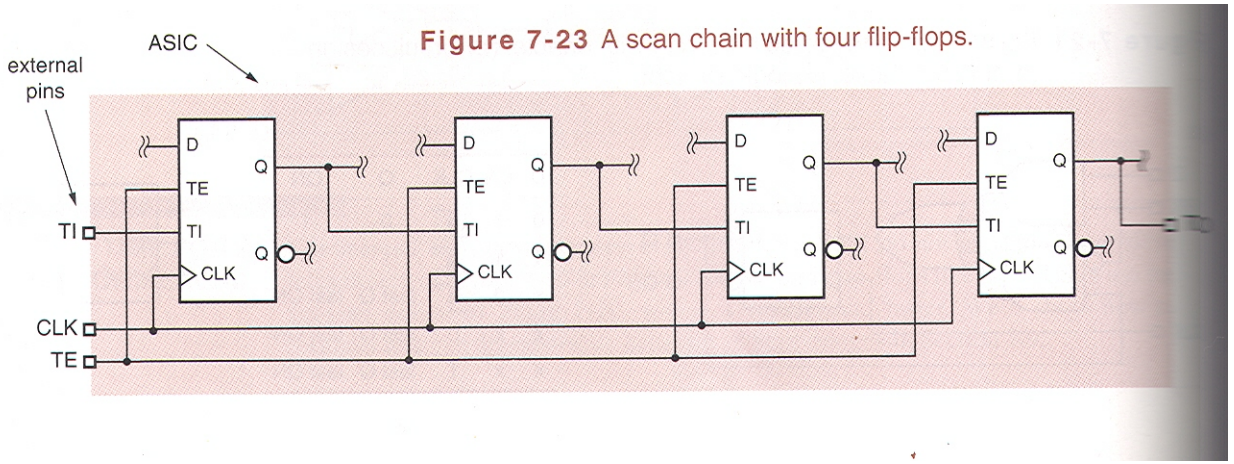
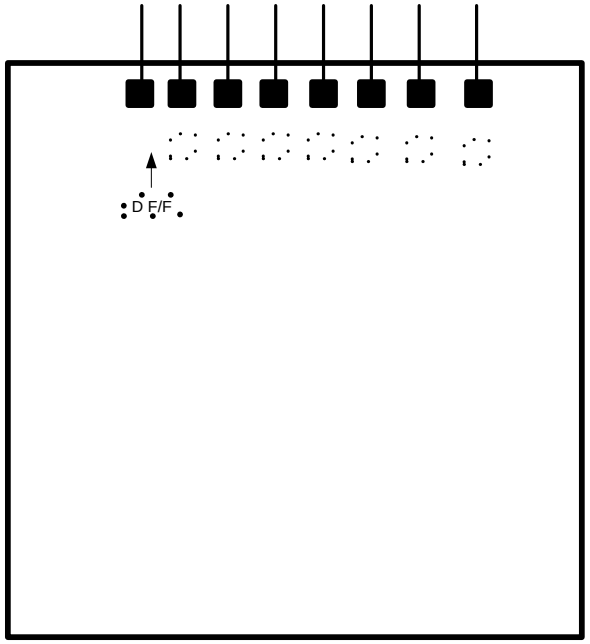


Figure 7-23 A scan chain with four flip-flops.

- What are scan chains?

Scan Chains

- Can use scan chains to inputs data or extract data



The T Flip Flop

- Toggle Flip Flop

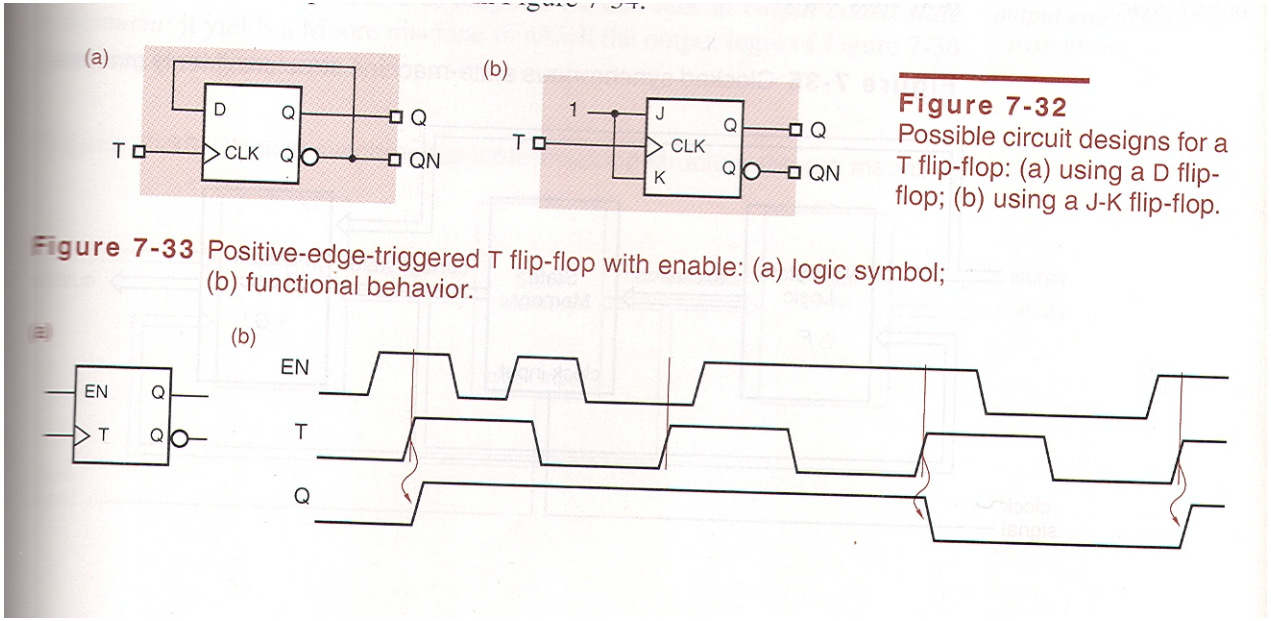
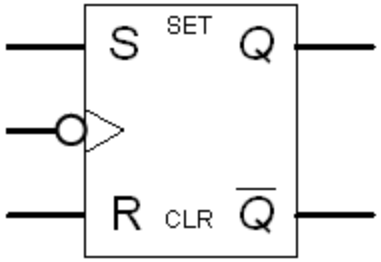


Figure 7-32
Possible circuit designs for a T flip-flop: (a) using a D flip-flop; (b) using a J-K flip-flop.

Figure 7-33 Positive-edge-triggered T flip-flop with enable: (a) logic symbol; (b) functional behavior.

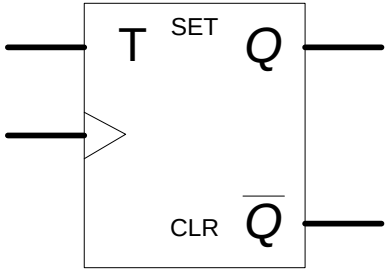
More on Basic Sequential Elements

- The S-R F/F
  - Q*=S+R'Q



S	R	CLK	Q
0	0	↓	Q
0	1	↓	0
1	0	↓	1
1	1	↓	Not allowed

- The Toggle F/F
  - Q*=Q'

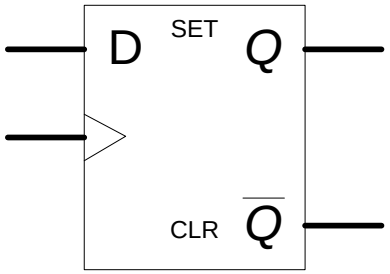


T	CLK	Q
0	↑	Q
1	↑	$\overline{Q}$

  - Q* is next value or next state

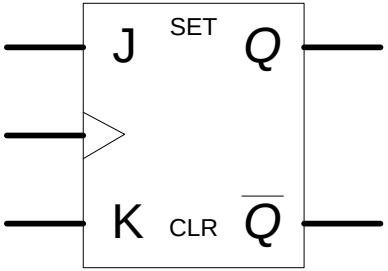
D F/F and J/K F/F

- D F/F
  - Q* = D



D	CLK	Q
0	↑	0
1	↑	1

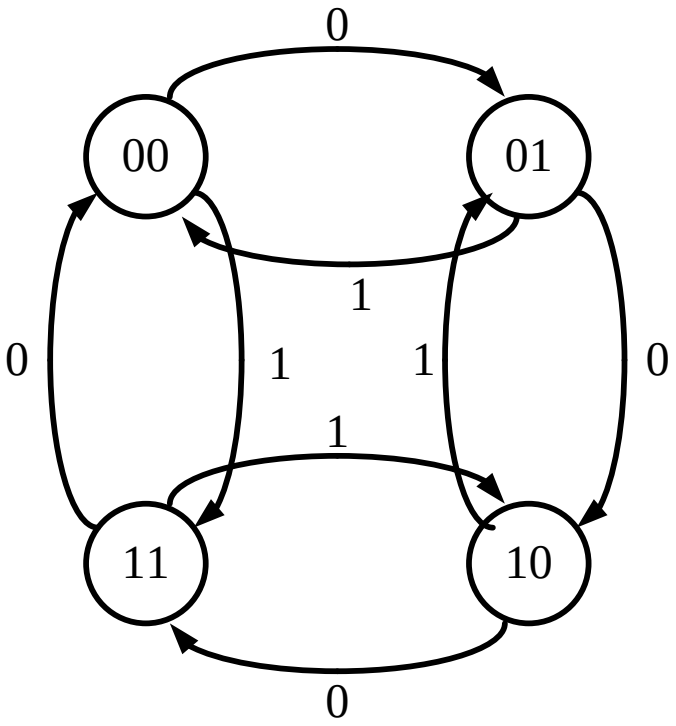
- J/K F/F
  - Q*=JQ'+K'Q



J	K	CLK	Q
0	0	↑	Q
0	1	↑	0
1	0	↑	1
1	1	↑	$\overline{Q}$

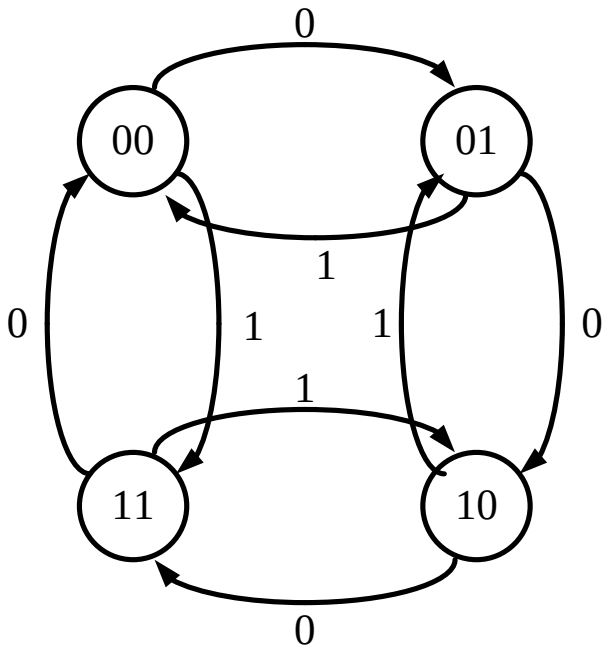
A simple up down counter

- Start with state diagram
- Control is x



Then add state table

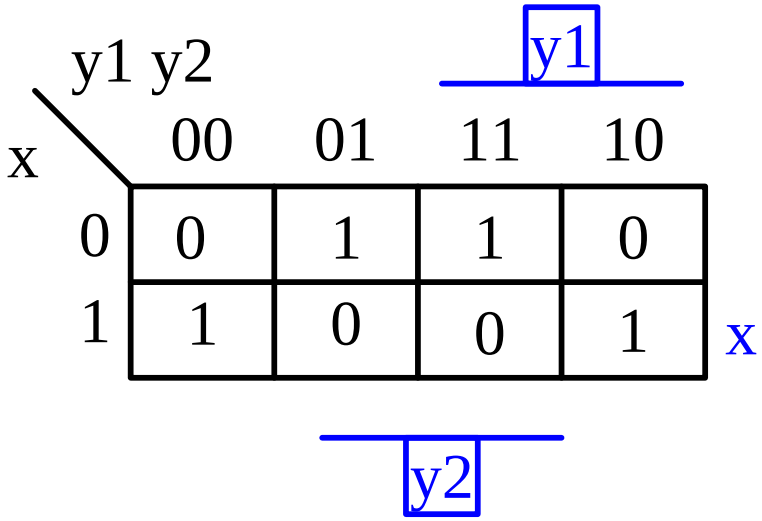
- Will use T F/Fs table reflect T F/Fs



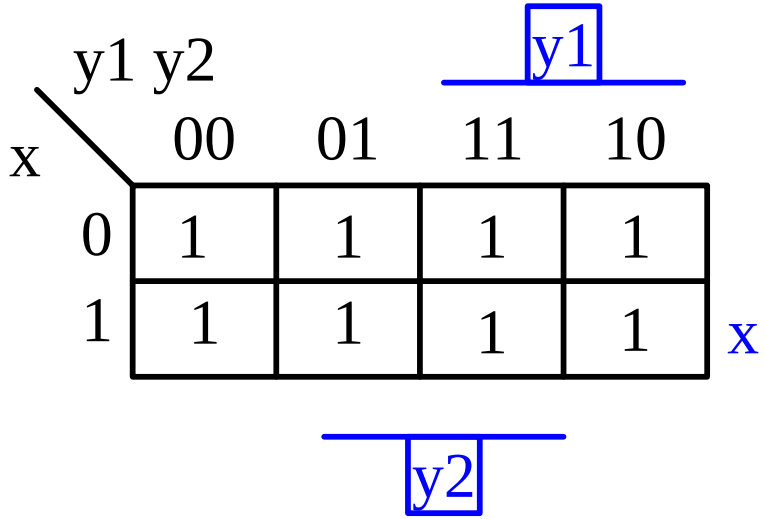
Pr St		Next State x=0		Next State x=1		T F/F inputs x=0		T F/F inputs x=1	
y1	y2	y1	y2	y1	y2	T1	T2	T1	T2
0	0	0	1	1	1	0	1	1	1
0	1	1	0	0	0	1	1	0	1
1	0	1	1	0	1	0	1	1	1
1	1	0	0	1	0	1	1	0	1

K Maps for the toggle F/Fs

T1



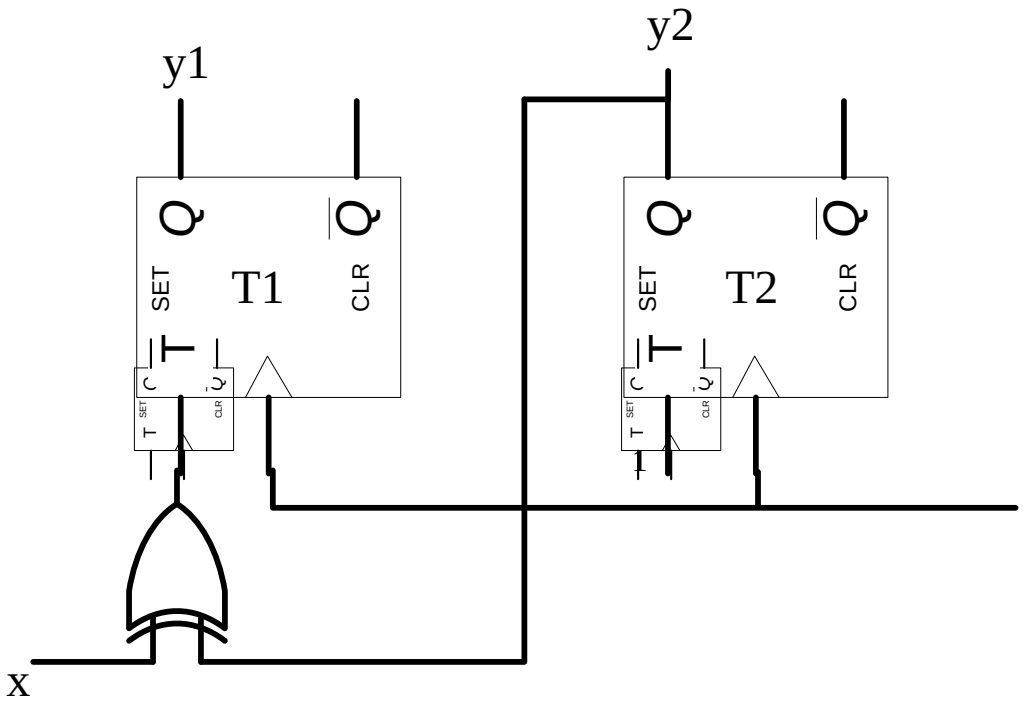
T2



T1 = x'y2 + x y2'

= x xor y2

Implementation



Some final notes

- Sequential elements (F/Fs) are bistable
- *Def*: Bistable – can be in one of two states

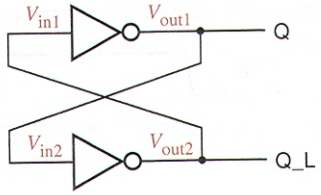


Figure 7-2
A pair of inverters forming a bistable element.

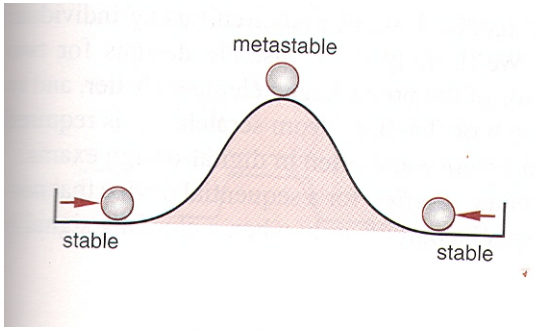


Figure 7-4
Ball and hill analogy for metastable behavior.

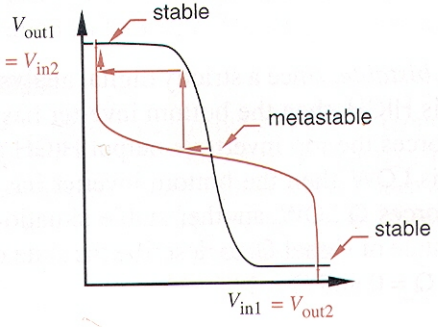


Figure 7-3
Transfer functions for inverters in a bistable feedback loop.

Transfer function:

$$V_{out1} = T(V_{in1})$$

$$V_{out2} = T(V_{in2})$$

Digital Circuit Types

- Combinational Logic Circuit – one whose outputs depend only on its current inputs.
  - A more descriptive term might be feedforward combinational logic circuits. These are circuits in which there is no feedback.
- Sequential Logic Circuit – one whose output depends not only on its current inputs, but also on the past sequence of inputs.

State changes

- A sequential circuit changes its state at times specified by a clock
- Clock frequency $C_f = 1 / T$
  - Where T is the Clock period

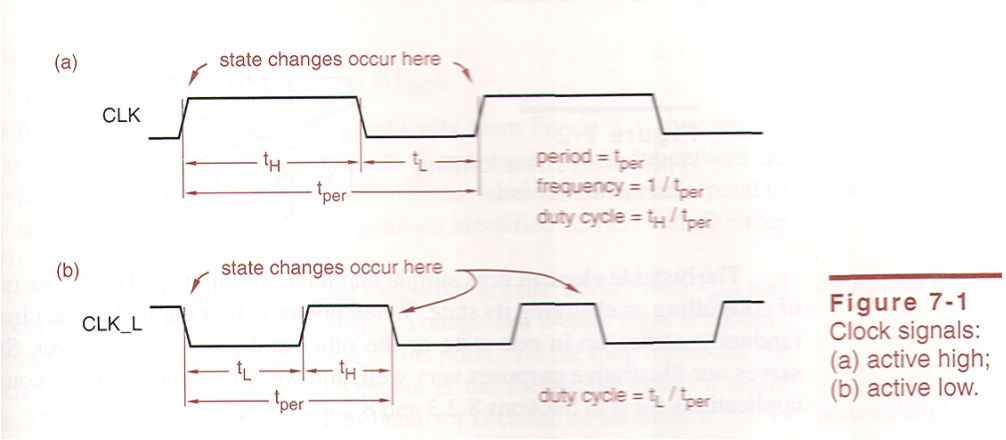


Figure 7-1
Clock signals:
(a) active high;
(b) active low.

9/25/2012 ECE 3561 Lect 2

Homework L2

- Read Unit 11
- Problem 11.1 – not for turn in – work for understanding – answer is in the text.
- (borrow a text or go to library)
- Go through the study guide of Unit 11