Homework Assignment #1 **DUE: Monday Jan 13th**

This assigment is intended as a run through the Quick VHDL system.
The commands relevant to this VHDL system are:

qhlib *library name* this command creates a library for the analyzed designs.
(you will need a library called "work")

qvhcom *design_file.vhdl* the VHDL compile command
qvhcom -source *design_file.vhdl* will print the source line and then the error message

qhdel *design_unit* deletes the design unit from the library

qhsim no arguments - starts up simulator - allows you to select library and design unit.

qhdir [-lib <library_name>] [<entity_name>] lists contents of a library

qhmap [<logical_name>] [<path>] defines a mapping between a logical library and a library directory

qhmap work ~/ee762/pr_step2_lib

STEP 1) Insure that you have a path set to access the mentor tools. Execute
>printenv | grep mentor

In response to this command you should get
PATH=/bin • • • with /usr/local/mentormaster/bin somewhere in the path
MGC_HOME=/usr/local/mentormaster
MGC_TMPDIR=/usr/local/mentormaster/tmp

If you do not get these (you may get more but that is ok), then add the following to your *.login* file (at a point after the "setenv PATH ...")

source /usr/local/mentormaster/SETUP

STEP 2) Create a directory for you work in this class and possibly even one for home-work and one for the project. Change directory to that directory and create a file with the following contents: (the remainder of this handout assumes you name the file, hw1.vhdl)

```
ENTITY  first_test  IS
END  first_test;
ARCHITECTURE  one  OF  first_test  IS
SIGNAL  phi1, phi2 :  BIT;
BEGIN
   PROCESS
   BEGIN
       WAIT FOR 10 NS;
       phi1 <=  '0';     phi2 <= '1';
       WAIT FOR 10 NS;
       phi1 <=  '1';     phi2 <= '0';
   END PROCESS;
END one;
```

STEP 3) In the directory for your work and contianing the file you just entered, you need to create a VHDL library. To do this execute

```
>qhlib    work
```

Then you can compile your design

```
>qvhcom  hw1.vhdl
```

STEP 4) Now we want to simulate the design for 200 ns. Execute the command

```
>qhsim
```

When the simulator starts, leave the resolution as "ns", and library work.
Click on the **entity** first_test and then click on the **Load** button.
The design will be loaded.

The VIEW pulldown in the main window is used to activate the other windows.
The available windows are Source, Structure, Variables, Processes, Signals, Wave, List
To see a waveform (or listing) for a signal, activate the Signals window and the wave window.

View --> Signals . . .
View --> Wave . . .

You can add all the signals to the waveform (or list) using the Wave and List pulldowns in the Signals window.

Wave --> Signals in region

You will see the names of the signals added to the wave display.
(Within the Wave and List windows you can explicitly add a signal using the "Prop" pulldown.)

STEP 5) You run the simulation using the RUN button or the Run pulldown. You can change the value for how long each press of RUN and the value shown in the Run pulldown using the options pulldown menu. You can also enter a command RUN *time* Press RUN twice to simulate for 200 ns. You should see the waveform generated in the Wave window.

STEP 6) Open a list window View --> List . . . in main window
Add the signals List --> Signals in region in Signals Window
Save the listing to a file File --> Write to File in List window

STEP 7) Save a copy of the waveform. In the Wave window under the File pulldown select "Write Postscript...". When the dialog box comes up your can use the default file name wave.ps or change it to another name. Then click OK.

STEP 8) Printouts. Print out the Listing file you created in step 6 using lp. Also printout the VHDL source that you entered in step 2 and prinout the waveform.

Turn in a copy of the VHDL source, the waveform, and the simulation listing file.