EE762 **Theory and Design of Digital Computers, II** **Winter 2003**

Instructor: Joanne DeGroat **Office:** 656 Dreese Lab 292-2439

Office Hours: to be announced

Texts: VHDL, Analysis and Modeling of Digital Systems, 2nd Edition, Zain Navabi, McGraw-Hill, 1998

Course Objectives: The objective of this course is to introduce the student to the detailed design of the major components of computer architectures using a modern HDL. After a brief review of the major components common to modern computer architectures, the student will be introduced to the design of components such as arithmetic logic units, floating point execution units, logic execution units, register design, controller design, instruction set design, cache design, and memory management unit design through HDL descriptions. At the conclusion of the course the student should be able to generate the specification for these units and complete the detailed design and writing of HDL descriptions of these components from these specifications.

Class	Subject	Text
1	Introduction and Course Overview	Ch 1,2, 3-3.1.3
2	VHDL Introduction	
3	Design and Modeling of ALU's (combinational design)	
4	Modeling and Simulation of a Generic Functional Unit	
5	Structural ALU Design and Description	
6	Behavioral Description	
7	Language Features - Survey of the Language	
8	"	
9	"	
10	"	
11	Timing and Concurrency - How HDL's Model Hardware	
12	Exam #1	
13	Exam Review and continue with new material	
14	Timing and Concurrency (continued)	
15	"	
16	Resolution Functions - Modeling and Simulation of Busses	
17	"	
18	"	
19	Design and Modeling of Floating Point Execution Unit's	
20	Behavioral Description	
21	Structural Description of Floating Point Unit	
22	"	
23	Design and Modeling of Cache Controllers	
24		
25	Exam #2	
26	Structural Description of Cache Controllers	
27	Behavioral Description of Cache Controllers	
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FINAL EXAM : Monday, March 17, 1:30PM-3:18PM

Grading Policy

Exams	60%
Homework and Computer Assignments	40%

Reference Texts:

VHDL, by Douglas L. Perry, McGraw Hill, 1991

A VHDL Primer, by Jayaram Bhasker, Prentice Hall, 1992

Chip Level Modeling with VHDL, by James Armstrong, Prentice Hall, 1988

IEEE Standard 1076-1987, VHSIC Hardware Description Language, IEEE Press, 1987

Computer Architecture, A Quantitative Approach, by John L. Hennessy and David A. Patterson, Morgan Kaufmann, 1990

Digital Systems, Hardware Organization and Design, 3rd Edition,
by Fredrick J. Hill and Gerald R. Peterson, John Wiley, 1987.

General Policies for this course:

1) Discussing homework and guided project step solutions with other students is permitted, however, the work you turn in must be yours! Electronic exchange of VHDL code is strictly prohibited, i.e., don’t do it!!!!

2) Homework and project step solutions must be turned in on time. Late submissions will be accepted on a case by case basis. Work submitted late will be subject to a late submission penalty of 2 points per day to a maximum of 50%. Homework and project step assignments will be handed out in class as the course progresses. They are due 2 classes after they are handed out, i.e., handed out on Monday - due Friday, handed out on Wednesday - due the following Monday, and handed out on Friday - due the following Wednesday.

3) Illness and extenuating circumstances are handled on a case by case basis. See me as soon as possible.

4) The intent is to post most course material on the web at
eewww.eng.ohio-state.edu/~degroat/